Content

List of figures:

List of tables:

List of equations:

Chapter 1.

1. Abstract.

The main objective in this project has been the design of a printed circuit board which name is *Bk1B111E11* and is part from a bigger system, ARAMIS CubeSat.

ARAMIS project is a low cost solution for any application of small size satellites. The principal element in *Bk1B111E11* are the solar cells, there are connected two in each side of the board (two on the bottom and two on the top), that is, four solar cells in total. Besides *Bk1B111E11* is part of a deployable structure, the arrangement consist in three tiles attached to CubeSat. The deployable structure is folded in the launch phase to avoid the vibration that can damage any component, then, once is stabilized, the satellite it will be deployed. The solution to keep attached the tiles is a thermal fuser. Each *Bk1B111E11* has eight holes, through each one passes a wire which keep join the three tiles, when the tiles should be deploy the thermal fuser works. Thermal fuser is composed by two resistors, one NTC100 and two MOSFETs, the resistors melt the tin (produced by Joule effect) allowing the deployment of the tiles, the NTC100 and the MOSFETs control the temperature so that no component is damaged.

For the final design of *Bk1B111E11* a series of necessary procedure have had to be follow to assure the correct work of the circuit. A database which have facilitate the design has been created. New components, as thermal fuser, has been created and simulated to verify their behaviour. And finally, all the components have been included in the board, and placed keeping all the restrictions and the rules required.

In conclusion, the board has been assembled and tested, and a microcontroller program has been written to control the temperature of the thermal fuser, since thermal fuser can damage any component if the temperature is no regulated, and therefore the mission could fail.

1.1. Introduction.

In this project the design of small size satellites CubeSat will be explained. Within this type of satellite we will focus in some electronics parts of ARAMIS. First of all, it is necessary to explain what the main features of CubeSat is, and why ARAMIS platform are a great solution for many satellite application.

CubeSat.

A CubeSat is a type of miniaturized satellite for space research, it is made up of multiples of 10×10×10 cm cubic units. CubeSat mass in not more than 1.33 kilograms per unit, and often use commercial off-the-shelf (COTS) components for their electronics and structure.

The CubeSat specification accomplishes several high-level goals. The CubeSat design specifically minimizes risk to the rest of the launch vehicle and payloads. The main reason for miniaturizing satellites is to reduce the cost of deployment: they are often suitable for launch in multiples, using the excess capacity of larger launch vehicles. Encapsulation of the launcher–payload interface takes away the amount of work that would previously be required for mating a piggyback satellite with its launcher. Unification among payloads and launchers enables quick exchanges of payloads and utilization of launch opportunities on short notice. [1]

ARAMIS platforms.

Is a solution for the creation of many kinds of satellite applications, its small size and its low cost structure is his principal advantage. ARAMIS is a new approach used in CubeSat. Its faces are PCBs that realize all basic features of the satellite. ARAMIS structure can be implemented for different format of CubeSat, 1U, 2U, 3U, (the structure project will be 1U) it is able to bring on board small telescopes, antennas. The main characteristic of the ARAMIS satellite of the project is the ability to deploy three tiles, in each tile there are four cells (two on each face), this design has been decided due to the faces of CubeSat are not large enough to mount a number of solar panels able to provide enough power to satellite subsystems.

To avoid vibration in the launch phase these deployable structures are closed. After the expulsion from the P-POD module, the solar panels' structure is deployed once in orbit and in this way the total surface of satellite exposed to the sun is increased, therefore also the power. The deployable solar panels are a solution that can be adapted to all CubeSat configurations.

It has payed particular attention at the connection that must be made to attach the structure to Bk1B6711 Test Board. Two spacers should be mounted in the opposite side to guarantee that the deployable structure does not touch the Test Board. It should handle the two power channels coming from two side of the deployable structure. Second of all, the concept of thermal fusers will be introduced, they are the deploying mechanism and therefore the main part of entire system.[2]

1.2. Current state of photovoltaic panels in satellites.

Solar energy in earth.

On planet Earth, the solar energy that reaches to the surface consists of direct and diffuse light. 20% of the radiation is reduced due to atmospherics conditions such as could be, pollution dust, etc. Due to the aforementioned only between 10-13% of the solar energy can be used. That means that average over a day is 0.1-0.2 kW/m². Therefore terrestrial and space photovoltaic solar panels have been designed different.

Space solar power.

The space solar energy is adhered out of the atmosphere Earth. Due at absence of gases in the space, the solar radiation is increased to 35% higher than that reached by the earth's surface. Therefore, in a photovoltaic solar panel in the geostationary Earth orbit (at an altitude of 36,000 km) eight time more light is received than in the Surface Earth, even it is closer to the Sun it number could be higher. An additional advantage is the fact that in the space there are no problems of weight or atmospheric corrosion.

Systems for the acquisition of space solar energy must be located at a distance from Earth above low Earth orbit since the nearest orbits are impractical due to the attractive force of the Earth. Due to the different characteristics between photovoltaic cells used in the space and in the Earth, the space photovoltaic cells are usually more expensive. Because of the high transport costs to space, a very important factor is the specific energy (that is, the energy generated divided by the unit of mass).[3]

Photovoltaics module in the International Space Station.

The cells used for the International Space Station are silicon covered by a thin glass that prevents degradation to radiation. The International Space Station is composed by 16 photovoltaic solar panels provide energy equivalent in area of football field. The system that integrates the International Space Station is the largest installed outside the earth.

The most efficient cells used in space are Gallium Arsenide called multi-junction cells, the materials with which are composed take better advantage of the sun's energy and are more robust to inhospitable conditions. Multi-junction cells have proven efficiency of 34%, are called multi-junction by the number of layers that make up the cell, can be three, four and up to six layers.

1.3. Background of the project.

The principal goals in the previous project (Development and testing of a deploying mechanism for the solar panel structure in ARAMIS satellite platform) about ARAMIS satellite was the designing of the deploying mechanism and the realization of a test board able to release the deployable solar panels' structure. Since the size of the satellite other target was the space reduction, making possible to integrate into the board other functions easily was an objective. In addition it had payed particular attention in electrical part, which was made following particular rules such as avoiding detachment of small parts in orbit and too high temperature due to the thermal fusers.

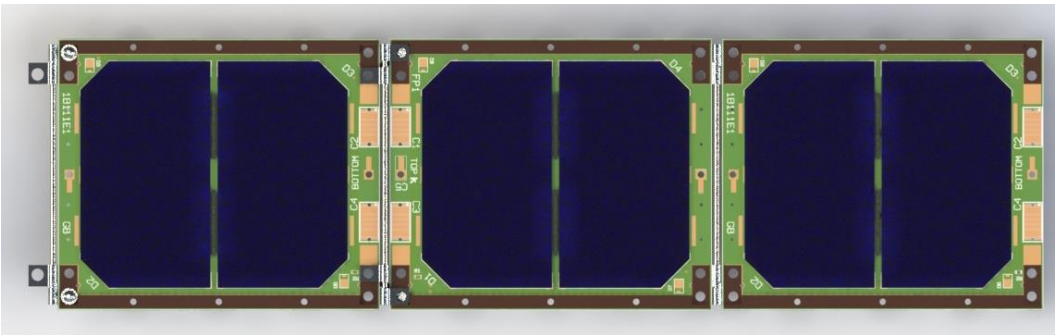


Figure 1. Design of the deployable panel system.

The solution for the objectives was to develop a deploying mechanism and the test board able to deploy the solar panels' structure. The structure was consisted in eight thermal fusers that have been used to detach the wire that keeps the deployable structure closed. The test board was made using components easily findable on market. Mechanical springs were employed to mount the structure in charge. The test board Bk1B6711 used to test the deploying mechanism was made following functional, electric and mechanical specifications required to be compatible with standard panels of the CubeSat and finally the elements were distributed on the board to guarantee the correct behaviour of the entire structure.

Figure 1 show the final design of test board *Bk1B6711*.

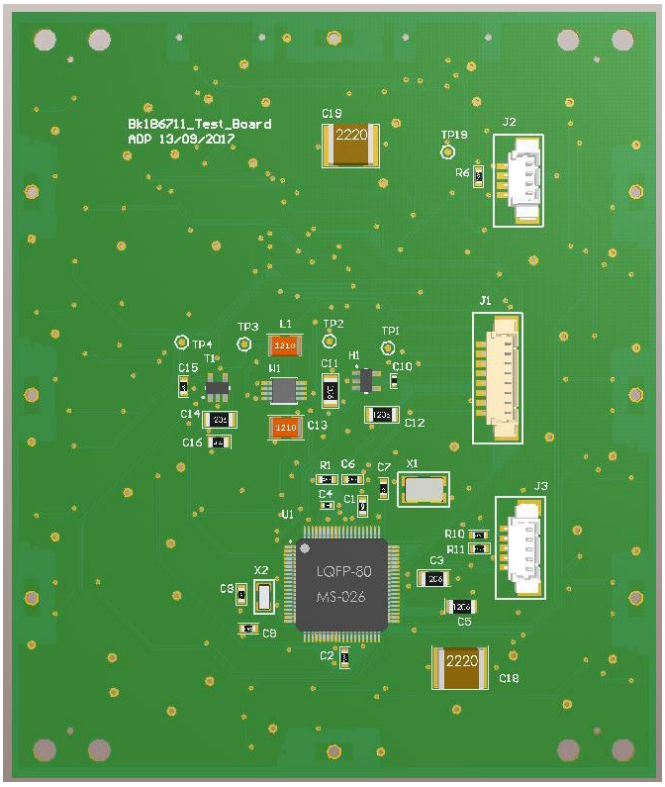


Figure 2. Test board Bk1B6711 design.

1.4. Proposed solution.

The target of this project is the continuation of Aramis satellite design, which is developed in four parts:

1. Design or modify of the PCB components, in this part of the project we have adapted the different components of the printed circuit in order to achieve the Aramis´s main goal, a small size and low cost. A component libreries has been created in order to unify all components and its features. Due it importance a simulation of different model of thermal fuser has been made. The program used to get all mentioned, has been ALTIUM.

2. Design of the PCB, the designed component has been placed in the correct position where has been kept in mind all design rules (the distances between each component, the order of placed, etc.). Once the board meet all the objective, a model 3D and a GERBER has been generated. In this point also, an explanation of features and requirements has been developed in order to de design of the circuit.

3. Test of the PCB, once the printed circuit board design is materialized, has been assembled all components in the laboratory by a process which will be explain in future chapters. A test of the board has been made to assure the correct functioning of the entire system.

4. Control the thermal fuser, the main of this part is to assure the correct functioning of the entire thermal fuser system, driving the thermal fuser temperature. In case that the temperature increase some elements can be damaged. The way to drive it is by a microcontroller (MSP430F543), and with the information of the NTC100 of thermal fuser. The microcontroller will receive information of the NTC100, one code will be executed and will decide the operation, and if the temperature is high the thermal fuser will be disabled.

1.5. Programs used.

Altium, Access, WordPad, and iAR are the programs that have been used to develop this project. The first, Altium has been used for the design of the PCB, in order to unite the different parts of a components (footprint, simulation, symbol, etc.) has been used Access, WordPad has been used for the writing of the code of the components simulation, and iAR is the program used to control the Texas Instrument Microcontroller which allow drive the thermal fusers.

1.5.1. Altium.

Altium Designer is a PCB and electronic design automation software package for printed circuit boards.

Schematics.

Altium Designer maintains a two-way connection between schematics and the PCB, providing a unified interface and data model throughout the design process to improve productivity. The schematic editor allows flat, hierarchical and mixed topology designs, design reuse, and numerous productivity accelerators.

Component Management.

The Unified Component Model employed by Altium Designer means each component has the symbols, variants, footprints, 3D mechanical and simulation models needed.

PCB Design.

The board provide mechanical mounting for the components and connected the appropriate pins together, implementing the logical design defined on the schematic.

3D PCB Design.

It can be easily toggle between the 2D and 3D display modes. Component models can be created in the PCB library editor from a set of simple 3D shapes, or 3D models can be imported, in a variety of formats, including STEP.

As well as importing component models, it can also import the product case, and 3D clearance checking can be performed.

Simulation.

With Altium Designer the XSPICE mixed analog and digital simulation and waveform editors are built in, allowing AC, transient, operating point, parameter sweep, monte-Carlo analyses and more.[4]

Definitely Altium in the project has been used to design the different footprint, symbols and simulation of the printed circuit board components. Footprint for the PCB, symbols for the schematics and simulation to assure the correct work of the circuit.

1.5.2. Access, WordPad and IAR.

Microsoft Access.

Is a database management system (DBMS) from Microsoft that combines the relational Microsoft Jet Database Engine with a graphical user interface and software-development tools.

Users can create tables, queries, forms and reports, and connect them together with macros. Advanced users can use Visual Basic for Applications (VBA) to write rich solutions with advanced data manipulation and user control. Access also has report creation features that can work with any data source that Access can access.[5]

This program has been used in order to a database creation which will unify the different component information (footprint, symbol, store…).The information is save by two different ways, a name or code and the direction of the fill.

Is important to classify the different components in order to facilitate design and the assembly. The following libraries are for the first Database, which is called AraMiS_Altium_Lib:

Actuators.	OP-AMP
Capacitors.	Processors.
Connectors.	Regulator-References.
Crystals-Oscillators.	Resistors.
Digital.	RF.
Diodes.	Sensors.
Drivers.	Switches
Inductors.	Transistors.

Table 1. Libraries of AraMiS_Altium_Lib component

And another Database has been made for the non-commercial components, it name is AraMiS_Altium_Lib_Extra.

There we have components like Photo Cell, the Thermal Fuser, or some PAD. This material have been specifically designed for the printed circuit.

ID	Part Number	Part Name	Library Ref	Library Path	Component Type
564	CELL_CESI_TJ_68.96X39.55	CELL_CESI_TJ_69X40	CELL_CESI_TJ_68.96X39.55	Symbols\Miscellanea.SchLib	Standard
571	CubeSat_1U_Frame	CubeSat_1U_Frame	CubeSat_1U_Frame	Symbols\Miscellanea.SchLib	Standard
572	Pad1x2R	Pad1x2R	Pad1x2R	Symbols\Miscellanea.SchLib	Standard
573	1B213RW-FIXING	1B213RW-FIXING	1B213RW-FIXING	Symbols\Miscellanea.SchLib	Standard
575	1B213RW-SOLAR-THROUGH-PINS	1B213RW-SOLAR-THROUGH-	1B213RW-SOLAR-THROUGH-	Symbols\Miscellanea.SchLib	Standard
576	CubeSat_1U_Embedded_Coil	CubeSat_1U_Embedded_Coi	CubeSat_1U_Embedded_Co	Symbols\Miscellanea.SchLib	Standard
577	Bk1B11E_Fuser_Serie	Bk1B11E_Fuser_Serie	Bk1B11E_Fuser_Serie	Symbols\Miscellanea.SchLib	Standard
578	Bk1B11E_Fuser_Serie_MOS	Bk1B11E_Fuser_Serie_MOS	Bk1B11E_Fuser_Serie_MOS	Symbols\Miscellanea.SchLib	Standard
579	Bk1B11E_Fuser_Parallel	Bk1B11E_Fuser_Parallel	Bk1B11E_Fuser_Parallel	Symbols\Miscellanea.SchLib	Standard
580	Bk1B11E_Fuser_Parallel_MOS	Bk1B11E_Fuser_Parallel_MO	Bk1B11E_Fuser_Parallel_MC	Symbols\Miscellanea.SchLib	Standard
581	CubeSat_1U_Frame_1B111E1	CubeSat_1U_Frame_1B111E	CubeSat_1U_Frame_1B111E	Symbols\Miscellanea.SchLib	Standard
582	PAD_FUSER	PAD_FUSER	PAD_FUSER	Symbols\Miscellanea.SchLib	Standard

Figure 3. AraMiS_Altium_Lib_Extra, example

Thus, each component has this features:

Name	Description
ID	Number of component.
Simulation.	Name of the model simulation.
Value.	Value of the component.
Footprint.	Name of the footprint component.
Note.	-
Package Footprint Ref.	Name of the footprint component.
Latest Revision Date.	-
Sim File.	Location of the model simulation.
Sim Model Name.	Reference to unify each file of the component.
Sim Prefix.	-
Supplier Part Number 1.	Code of supplier store.
Supplier 2.	Name of the store
Supplier Part Number 2.	Code of supplier store.
Part Name.	Name of the component.
Part Label.	Name of the component.
Tolerance.	Kind of simulation
Sim Kind.	-
Library Path.	Location of the symbol component.
Footprint Path.	Location of the footprint.
Sim Sub Kind.	Sub-kind of simulation
Temperature Coefficient.	-
Operating temperature.	-
Sim Port Map.	-
Supplier 1.	Name of the store.
Document.	-
Package Reference.	Name of the footprint component.
Pin Count.	Number of pins.
Publisher.	Database editor.
Datasheet Document.	-
Component Type.	-
Publisher.	-
Signal Integrity.	-
Part Number.	Name of the footprint component.
Library Ref.	Name of the component.

Table 2. Classification of AraMiS_Altium_Lib feature

ID	Part Number	Part Name	Library Ref	Library Path	Component	Datash	Part Label
167	RS_693-5527	J_14_FEMALE_IDC	J_14_FEMALE_SMT_IDC	Symbols\Connectors.SchLib	Standard		J_14_FEMALE_SMT_IDC_091851478
168	DK_WM5587CT-ND	J_UMC_FEMALE_50Ohm	J_UMC_FEMALE_3mmx4mm_SMT	Symbols\Connectors.SchLib	Standard		J_UMC_FEMALE_3mmx4mm_SMTM
169	DK_WM1722-ND	J_4_FEMALE_PicoBlade	J_4_FEMALE_SMT_PicoBlade	Symbols\Connectors.SchLib	Standard		J_4_FEMALE_SMT_PicoBlade_1A
170	DK_WM7608-ND	J_4_MALE_PicoBlade	J_4_MALE_SMT_PicoBlade	Symbols\Connectors.SchLib	Standard		J_4_MALE_SMT_PicoBlade_1A
171	DK_WM1724-ND	J_6_FEMALE_PicoBlade	J_6_FEMALE_SMT_PicoBlade	Symbols\Connectors.SchLib	Standard		J_6_FEMALE_SMT_PicoBlade_1A
172	DK_WM7610CT-ND	J_6_MALE_PicoBlade	J_6_MALE_SMT_PicoBlade	Symbols\Connectors.SchLib	Standard		J_6_MALE_SMT_PicoBlade_1A
173	DK_WM1726-ND	J_8_FEMALE_PicoBlade	J_8_FEMALE_SMT_PicoBlade	Symbols\Connectors.SchLib	Standard		J_8_FEMALE_SMT_PicoBlade_1A
174	DK_WM7612CT-ND	J_8_MALE_PicoBlade	J_8_MALE_SMT_PicoBlade	Symbols\Connectors.SchLib	Standard		J_8_MALE_SMT_PicoBlade_1A
175	DK_H11809CT-ND	J_SMTM_FEMALE_50Ohm	J_SMTM_FEMALE_3mmx4mm_SM	Symbols\Connectors.SchLib	Standard		J_SMTM_FEMALE_3mmx4mm_SMT
176	DK_WM1721-ND	J_3_FEMALE_PicoBlade	J_3_FEMALE_SMT_PicoBlade	Symbols\Connectors.SchLib	Standard		J_3_FEMALE_SMT_PicoBlade_1A
177	DK_WM7621CT-ND	J_3_MALE_PicoBlade	J_3_MALE_SMT_PicoBlade	Symbols\Connectors.SchLib	Standard		J_3_MALE_SMT_PicoBlade_1A
178	DK_WM7619CT-ND	J_15_MALE_PicoBlade	J_15_MALE_SMT_PicoBlade	Symbols\Connectors.SchLib	Standard		J_15_MALE_SMT_PicoBlade_1A
179	DK_WM7609CT-ND	J_5_MALE_PicoBlade	J_5_MALE_SMT_PicoBlade	Symbols\Connectors.SchLib	Standard		J_5_MALE_SMT_PicoBlade
180	DK_609-3487-1-ND	J_6_MALE_2.54mm	J_6_MALE_SMD-2.54_Berg	Symbols\Connectors.SchLib	Standard		J_6_MALE_SMD-2.54_Berg_X
181	DK_WM5409CT-ND	J_3_MALE_EzMATE	J_3_MALE_SMD_EzMATE	Symbols\Connectors.SchLib	Standard		J_3_MALE_SMD_EzMATE_X
182	DK_J501-ND	J_SMA_FEMALE_50Ohm	J_SMA_FEMALE_TH_SMA	Symbols\Connectors.SchLib	Standard		J_SMA_FEMALE_TH_SMA_50Ohm
183	RS_670-4203	J_PIN-CRIMP_FEMALE_PicoBlade	J_1_FEMALE_PIN-CRIMP_PicoBlad	Symbols\Connectors.SchLib	Standard		J_1_FEMALE_PIN-CRIMP_PicoBlade_
184	DK_WM17002-NF	J_15_FEMALE_PicoBlade	J_15_FEMALE_SMT_PicoBlade	Symbols\Connectors.SchLib	Standard		J_15_FEMALE_SMT_PicoBlade_1A
185	DK_WM1723-ND	J_5_FEMALE_PicoBlade	J_5_FEMALE_SMT_PicoBlade	Symbols\Connectors.SchLib	Standard		J_5_FEMALE_SMT_PicoBlade_1A
186	DK_WM3564	J_3_FEMALE_EzMATE	J_3_FEMALE_SMT_EzMATE	Symbols\Connectors.SchLib	Standard		J_3_FEMALE_SMT_EzMATE_1.5A
187	RS_700-1025	J_4_PLUG_EzMATE	J_4_PLUG_XX_EzMATE	Symbols\Connectors.SchLib	Standard		J_4_PLUG_XX_EzMATE_X
188	RS_700-0833	J_4_MALE_EzMATE	J_4_MALE_SMT_EzMATE	Symbols\Connectors.SchLib	Standard		J_4_MALE_SMT_EzMATE_1.5A
189	RS_700-1022	J_3_PLUG_EzMATE	J_3_PLUG_XX_EzMATE	Symbols\Connectors.SchLib	Standard		J_3_PLUG_XX_EzMATE_X
190	FR_112-5274	J_WIRE_PicoBlade	J_1_WIRE_AWG28_PicoBlade	Symbols\Connectors.SchLib	Standard		J_1_WIRE_AWG28_PicoBlade_X
191	DK_S9134-ND	J_20_MALE_1.27mm	J_20_MALE_SMT-1.27mm_SHROU	Symbols\Connectors.SchLib	Standard		J_20_MALE_SMT-1.27mm_SHROUD

Figure 4. AraMiS_Altium_Lib, example.

WordPad.

WordPad is a basic word processor, included with almost all versions of Microsoft Windows. The simulations codes have been developed within this program. The simulation is an important part of the components that will be explain in future chapters.

IAR.

IAR Embedded Workbench is a program that allow to create code for MSP430 devices, in the project a microcontroller MSP430F543 will be program, in order to drive the thermal fuser. In IAR a code and simulation can be make.

Chapter 2:

2. Components.

To assemble the board the different components have been designed correctly beforehand, (thermal fuser, resistors, photovoltaics cells, diodes…). It is important to know its measures and characteristics to achieve correct operation, and simplify the assembly of the board for future works. The process to get the design of this components has been described in this point.

The design of a printed circuit board is the goal of this project, but it is made up of different devices that give a function to the board. The models of the components have been described in this paragraph.

2.1. Thermal fusers.

One of the goals of the Aramis satellite is to avoid the vibration that can be produced when CubeSat is allocated into the P-POD module, in the launch phase. This vibration can damage the three *Bk1B111E* PCBs. In order to solve this problem eight wires which will keep the system together have been introduced.

Thermal fusers are devices specifically designed to keep the deployable structure stable and not subject to vibrations in the launch phase, once there were not any danger, can be deployed. Each fuser is formed by one hole, the holes have been used to pass the wire through the three PCBs its mission is to keep together all of them. The location of them in the board are: six holes in the lateral support, one in the top and one in the bottom.

The way of functioning is using eight wires that pass through the PCBs keeping them together. Thus, thanks to the Joule effect produced by thermal fusers, the tin solder in the holes is dissolved, allows the deployment of entire structure, thanks to the mechanical springs.

To achieve the Joule effect a current passes through a resistance in order to produce the heat needed to weld the tin where the wire is soldered.

It is important that detachment system verify some strict requirements:

- Any component of the satellite should not be damaged, in case it happened, a short circuit could be occur and the mission could fail. For that reason the detachment system must guarantee not to detach any components from the satellite transforming themselves into dangerous space debris.
- In order to withstand the high acceleration on the launch phase, the tensile strength of the wires should be enough.
- Another requirement is to control the power consumption of the thermal fusers during its activity, the thermal fusers should not have high power consumption, and they should not reach too high temperatures. In order to solve this problem, a microcontroller program which will control the thermal fuser depending of the temperature has been created.
- The space occupation and weight are an important feature to consider.

To understand better the architecture of the thermal fuser the figures below have been included:

In figure X the feedback of the thermal fuser is shown, NTC100 of the thermal fuser send information to the Microcontroller, which depending of the temperature value will enable or disable the thermal fuser.

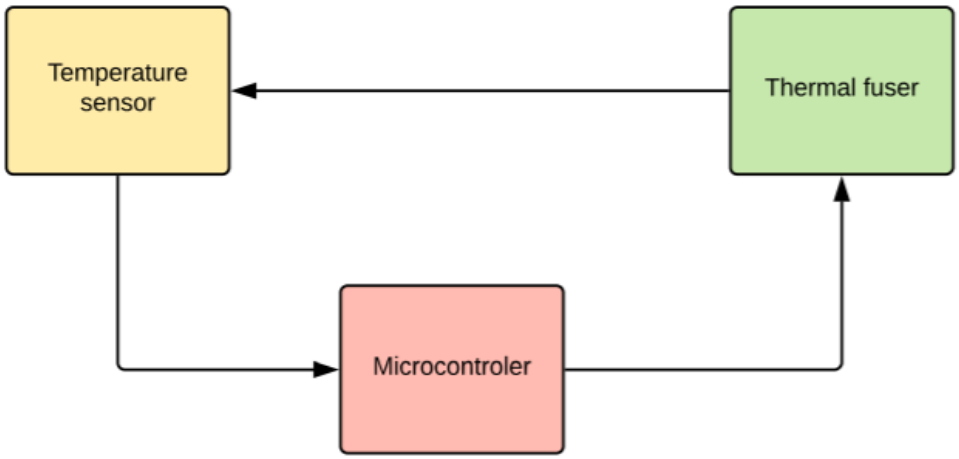
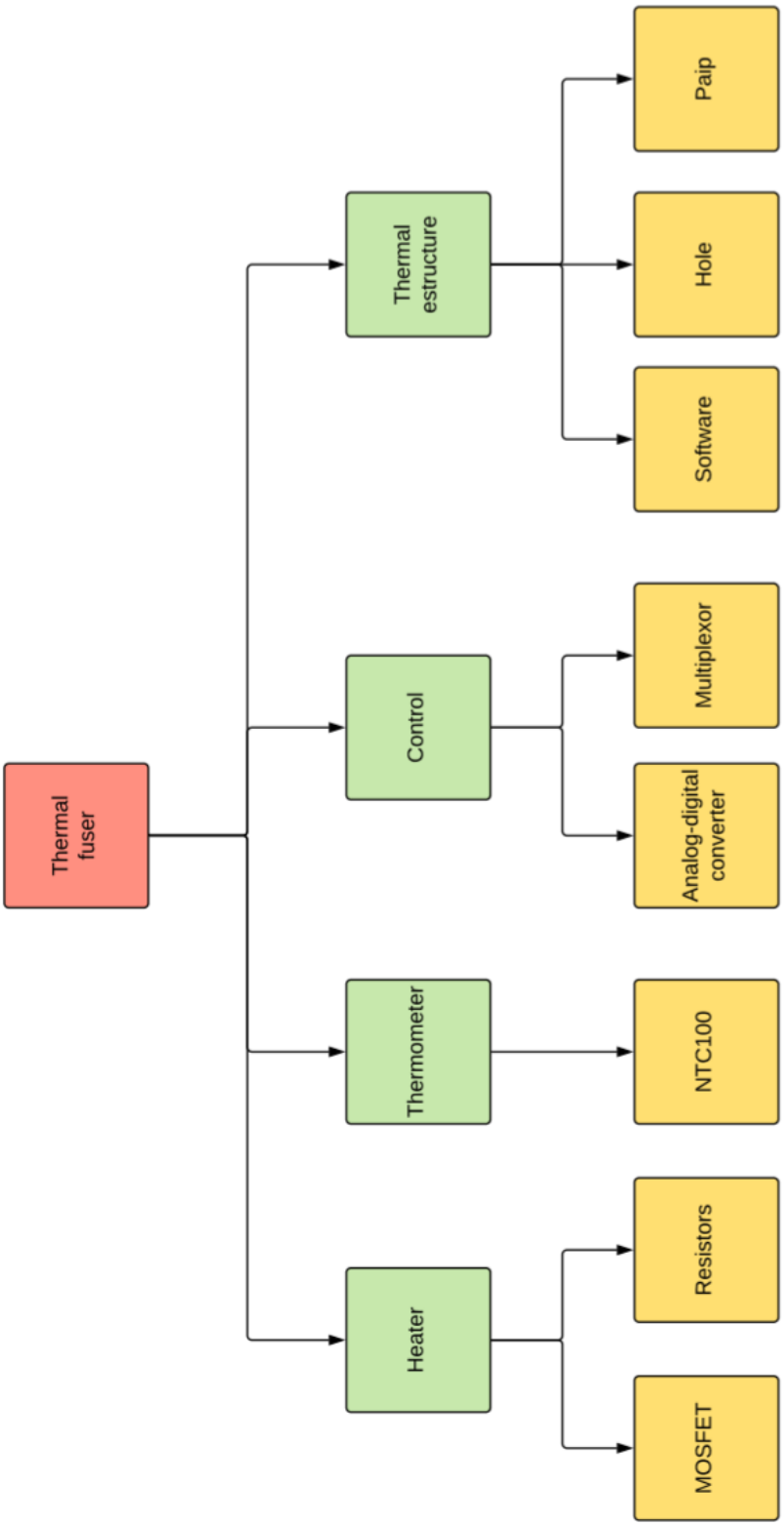


Figure 5. Feedback of thermal fuser.

On the other hand, the figure below shows the architecture of the fuser. The fuser is compose of four main blocks:

1. Heater: it purpose is the melt of the wire in the hole, form by the resistor and MOSFETs.
2. Thermometer: it main function is the measure of the temperature in the fuser, formed by a NTC100.
3. Thermal structure: the place where the tin will be melted and the wire through the system.
4. Control: system that will control the melting of the wire, and therefore the opening of the deployable system.


Thermal fuser
Thermal estructure
Paip
Hole
Software
Control
Multiplexor
Analog-digital converter
Thermometer
NTC100
Heater
Resistors
MOSFET

The thermal fusers are formed by two resistance, one NTC, and two MOSFET, the conversion of electric energy in heat by Joule effect is the form of the deployment mechanism as mentioned above.

To produce Joule effect, and deploy the *Bk1B111E* solar panels' structure, is necessary to get a power enough that can melt the tin. The power depends on which material the wires are composed of. The wire in ARAMIS satellite is composed by CuBe. Therefore the power necessary to melt the tin where the wires are soldered is 1.5W. The circuit is designed considering the high voltage bus of 14V, according to ARAMIS specifications.

Resistors. The two resistance have to be very close to the pad of the soldered wire, this is because the heat of the resistance which have to melt the tin in this area. In order to obtain the necessary power the value of the resistors has been calculates, due to different connections (series or parallel), the resistors have different values.

The value of the resistors was calculated in the previous project (Development and testing of a deploying mechanism for the solar panel structure in ARAMIS satellite platform).

First, knowing the power consumption and the voltage, the current that passes through the wire (I_{min}) has been calculated:

$$Power = V \cdot I_{min}$$

Equation 1. Power consumption.

$$I_{min} = \frac{Power}{V} = \frac{1.5W}{14V} = 107mA$$

Equation 2. Minimal current.

Then, it has been calculated the equivalent resistor.

$$R_{eq} = \frac{V}{I_{min}} = \frac{14V}{107mA} = 131\Omega$$

Equation 3. Equivalent resistor.

And finally, keeping in mind the two different configuration, series and parallel, have been calculated the value for each case:

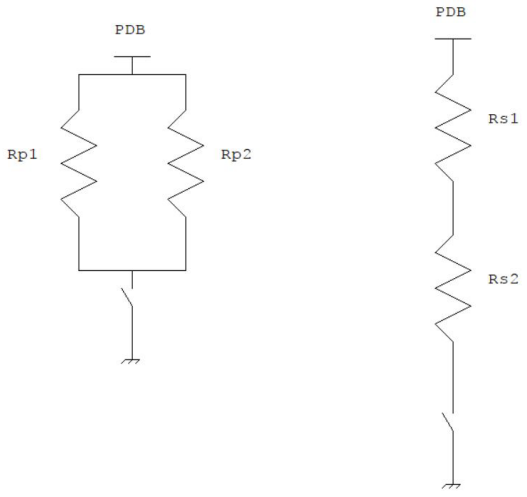


Figure 6. Resistors of thermal fuser configuration

$$R_{s1} = R_{s2}$$

$$R_{eq} = R_{s1} + R_{s2} = 2R_{s1}$$

$$R_{s1} = \frac{R_{eq}}{2} = \frac{131}{2} = 65.5\Omega$$

Equation 4. Series resistance calculation.

For the parallel configuration:

$$R_{p1} = R_{p2}$$

$$R_{eq} = \frac{R_{p1} \cdot R_{p2}}{R_{p1} + R_{p2}} = \frac{R_{p1}^2}{2R_{p1}} = \frac{R_{p1}}{2}$$

$$R_{p1} = 2 \cdot R_{eq} = 262\Omega$$

Equation 5. Parallel resistance calculation

NTC. The NTC is positioned close to the resistors the NTC function is to control the temperature of the resistance. The technique used is as follows, NTC read the temperature change in the resistor, then by a voltage differential the information arrives to the microcontroller and then the microcontroller will decide if the temperature is too high and if were needed it would disable the thermal fuser. The chosen NTC has been *NTCS0603E3104FXT*.

MOSFETs. Drive by the microcontroller, to avoid short circuit between the power supply and the ground has been included a driving circuit of the thermal fusers. The drive circuit consists of two transistors and two resistors of a few ohms connected to the gates. Its function is very easy; when the satellite is ejected from the P-POD module, the two MOSFETs can enable the fuser and can disable it in the event of malfunction also if the temperature reached by the thermal fusers is too high. The chosen MOSFT has been *IRLHS6376TRPBF*.

Table below resume the main characteristic of the thermal fusers.

Thermal Fuser	MOSFET	Resistance
Bk1B671A	-	Series
Bk1B671B	✓	Series
Bk1B671C	-	Parallel
Bk1B671D	✓	Parallel

Table 3. Thermal fuser resume.

The design of the thermal fuser were done in the thesis *Development and testing of a deploying mechanism for the solar panel structure in ARAMIS satellite platform,* although in this project some changes in the symbol as the position of the resistance have been made.

Four models of thermal fusers have been design:

1. *Bk1B671A_Thermal_Fuser_Series.*

Two resistance connected in series and the MOSFETs not included in the component symbol are the main difference between this model and the others.

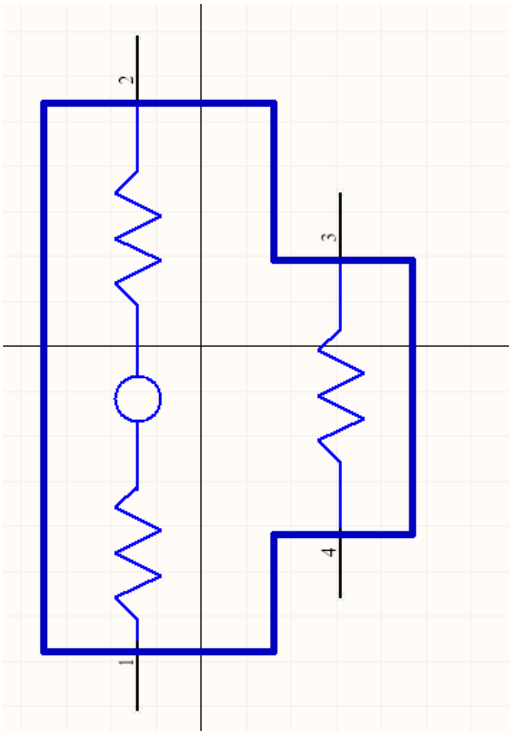


Figure 7. Symbol of Bk1B671A_Thermal_Fuser_Series.

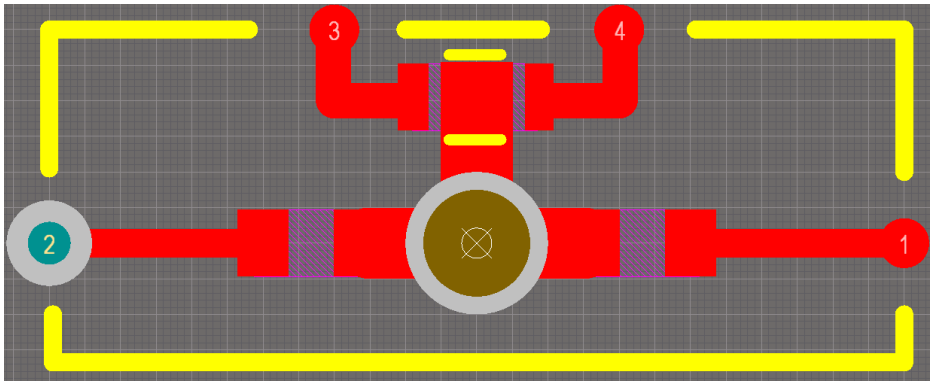


Figure 8. Footprint of Bk1B671A_Thermal_Fuser_Series.

2. *Bk1B671B_Thermal_Fuser_Series_MOS.*

This model has included the MOSFETs in the symbol, in difference with the last thermal fuser, it also has the resistance in series and the hole between the two resistors. As in the last component (*Bk1B671B_Thermal_Fuser_Series)*, this model has the inconvenience that if one resistor is damaged, it could produce a short circuit.

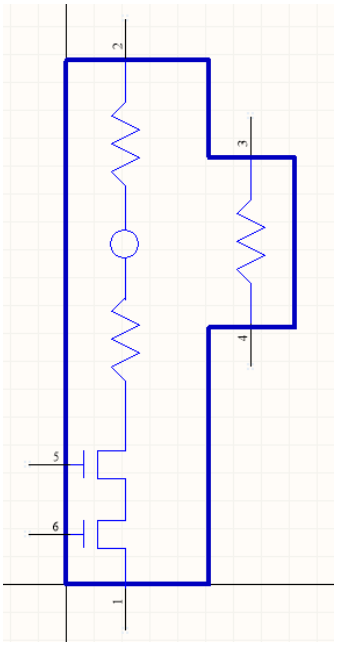


Figure 9. Symbol of Bk1B671B_Thermal_Fuser_Series_MOS.

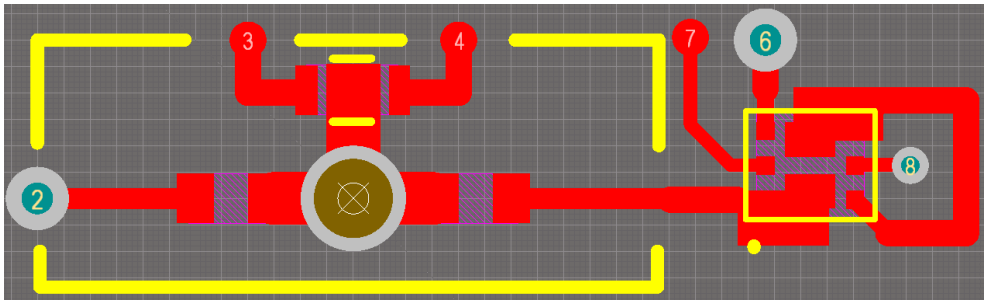


Figure 10. Footprint of Bk1B671B_Thermal_Fuser_Series_MOS

3. *Bk1B671C_Thermal_Fuser_Parallel.*

In this case the thermal fuser has the resistance connected in parallel, this configuration has the advantage that, if one of the resistance is damage, any short circuit will be produce. In this model there are not any MOSFETs included in the symbol.

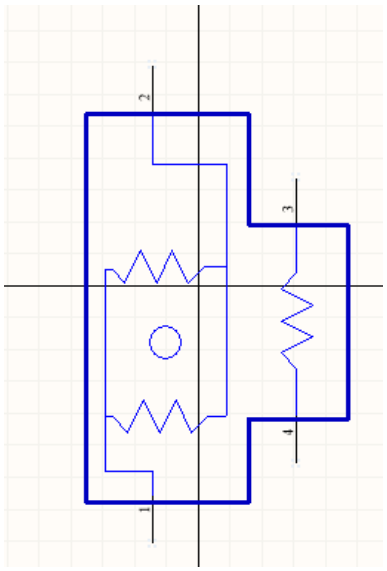


Figure 11. Symbol of Bk1B671C_Thermal_Fuser_Parallel.

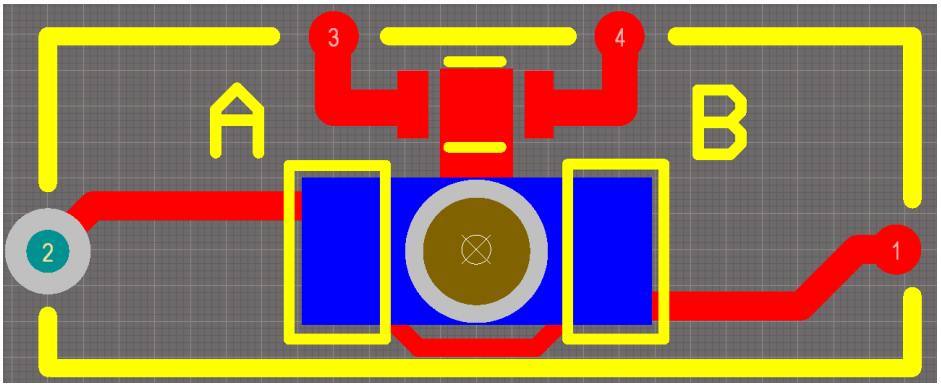


Figure 12. Footprint of Bk1B671C_Thermal_Fuser_Parallel.

4. *Bk1B671D_Thermal_Fuser_Parallel_MOS.*

This thermal fuser has also two parallel resistors therefore it has the advantage that, if one of the resistance is damage, any short circuit will be produce. The MOSFETs are included in the symbol as *Bk1B671B_Thermal_Fuser_Series_MOS.*

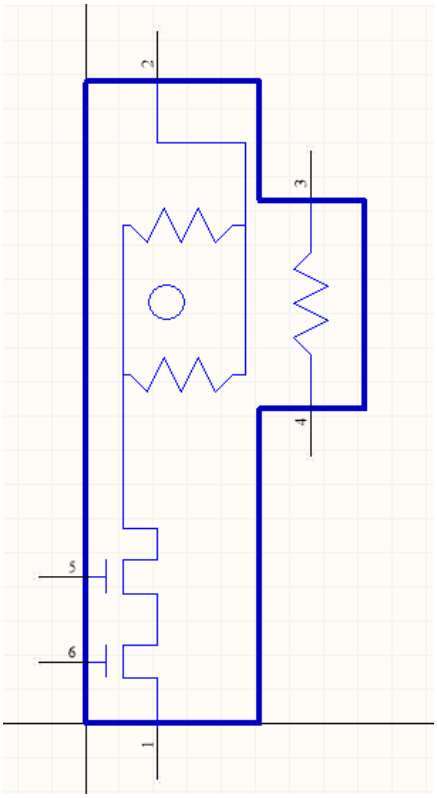
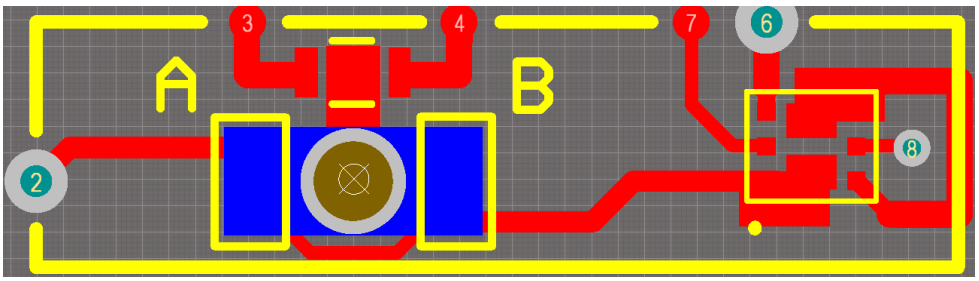


Figure 13. Symbol of Bk1B671D_Thermal_Fuser_Parallel_MOS



Bk1B671E_Pad_Fuser.

Finally, in the design of *Bk1B111E* has been needed to consider the footprint PAD of the thermal fuser. Since thermal fuser will contain it board. *Bk1B111E* has eight holes where the wire pass through.

Therefore a footprint and a symbol of this important component has been design.

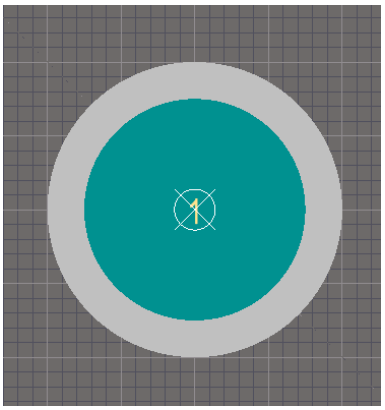


Figure 14. Footprint of Bk1B671E_Pad_Fuser.

Hole size	1.5mm
Diameter	2mm

Table 4. Measures of Bk1B671E_Pad_Fuser

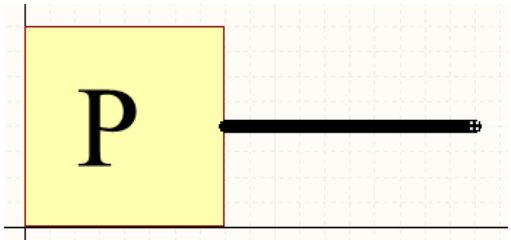


Figure 15. Symbol of Bk1B671E_Pad_Fuser.

2.1.1. Solar Cells.

The board *Bk1B111E* will be constituted by four solar cells, two in the top side and another two in the bottom side. Thus, when the satellite is in orbit will receive solar arrays always.

The model chosen has been *CESI-Cell-TJ-68.96x39.55* their efficiency is 29.5% and it can generate approximately 2.3V, so if it is connected in series the output voltage will be about 4.6V. In order to protect them, a bypass diode has been connected in parallel to each solar cell to assure the correct work of the *CESI-Cell-TJ-68.96x39.55*, even one of them is damaged.

This model has been develop by CESI and can resist temperatures from -250°C to 300°C, has a high radiation resistance and a good mechanical strength. [6]

Table 4 show the solar cell average electrical output parameters when temperature is 25°C.

Area (cm^2)	I_{SC} (mA)	V_{OC}(V)	I_m (Ma)	V_m(V)
26.5	473	2.6	455	2.32
30.15	538	2.61	517	2.33

Table 5. Performance data of CESI-Cell-TJ-68.96x39.55

Figure X represent the Current-Voltage characteristic of the solar cell (blue) when the temperature is 25°C.

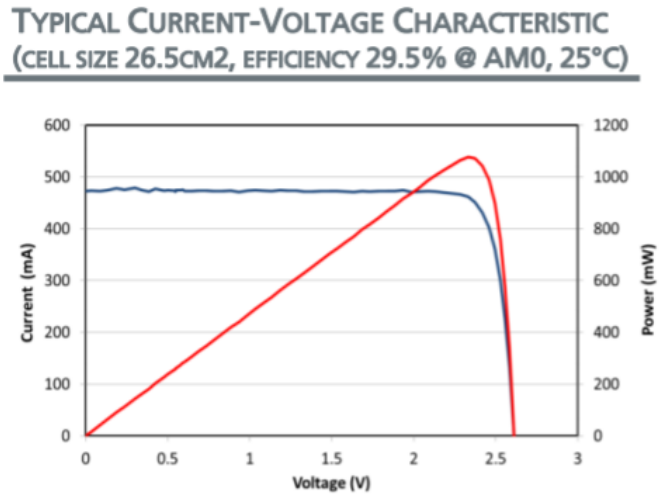


Figure 16. Typical current-voltage characteristic of CESI-Cell-TJ-68.96x39.55

2.1.2. Diode.

As were mentioned in the last point the solar cells need to have a bypass diode connected, because otherwise, if one side of Bk1B111E were damaged or obscured by the shadow cast (due to the movement of ARAMIS Satellite) the space mission could fail.

The chosen diode is *DK_UPR10E3CT-ND*, this diodes compliant and offers optimized forward voltage characteristic with reverse blocking capabilities up to 150V, in addition the diode include a full metallic bottom that eliminates possibility of solder flux entrapment during assembly and a unique locking tab acts as an efficient heat path form die to mounting plane for external heat sinking with very low thermal resistance junction to case.[7]

Its nominal voltage is 100V and the maximum current is 2.5A.

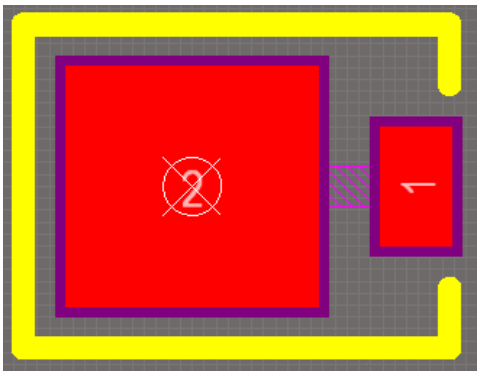


Figure 17. Footprint of DK_UPR10E3CT-ND.

2.1.3. Connectors.

The deployed structure is composed by three *Bk1B111E* boards therefore to be connected between them is necessary consider some restrictions.

One important restriction is to keep the connection of one of the face with face which is also received the solar lighting, in the other tile, since if one connection is not kept, then there would produce a short circuit.

The chosen connector is *J_8_CABLE_FFC*, it has 6 connectors, two for the ground and four for the components.

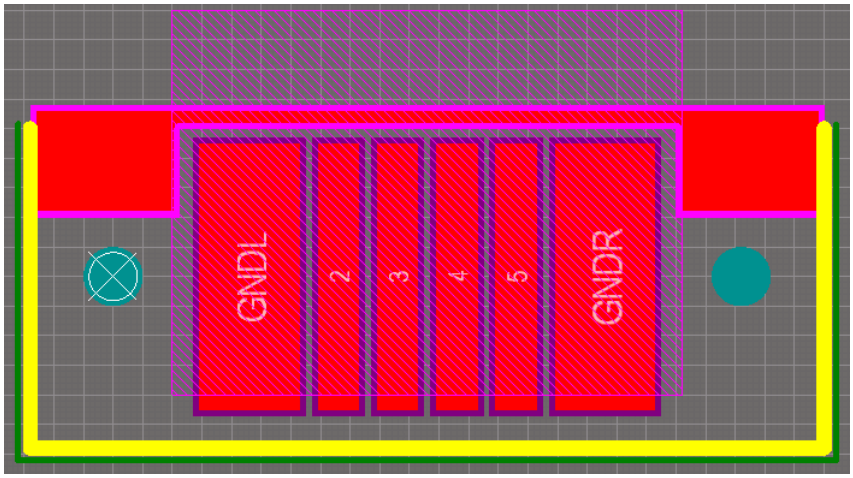


Figure 18. Footprint of J_8_CABLE_FFC.

2.2. Methodology.

The methodology to create the project could be resume in four steps:

1. Unify database, since not all components belonged to the same database (AraMiS_Altium_Lib), for this step was necessary to make new components.
2. Simulate the components, in order to prove their correct functioning.
3. Make the circuit schematic, this part is making with the symbols of the components.
4. Make the printed circuit board, once compiled the schematic, it has been created a PCB in Altium with the footprints of the components.

2.2.1. Component creation.

To create a component in the data base it has been started verify each component of the system *Bk1B6711* and *Bk1B111E* in order to make sure that it belonged to the same library (or AraMiS_Altium_Lib_Extra), if any element was not included in that library, it was changed and created again.

The components not included were:

- LTC3631EMS8E-5#PBF-ND (regulator): has been included in AraMiS_Altium_Lib (regulator group).
- DK_587-1628-1-ND (coil): has been included in AraMiS_Altium_Lib (inductor group).
- J_8_CABLE_FFC (cable): its pins has been modified and has been included in AraMiS_Altium_Lib (connector group).
- J5_SMD_PicoBlade (pico blade): has been included in AraMiS_Altium_Lib (connector group).
- IRLHS56376HbF (MOSFET): has been included in AraMiS_Altium_Lib (transistor group).
- Bk1B671A_Thermal_Fuser_Series (series thermal fuser): a simulation has been created and has been included in AraMiS_Altium_Lib_Extra.
- Bk1B671B_Thermal_Fuser_Series_MOS (series MOSFET fusor): a simulation has been created and has been included in AraMiS_Altium_Lib_Extra.

However, not all of them were not previously made, the following components have been made from the beginning:

- Bk1B671C_Thermal_Fuser_Parallel (parallel thermal fuser): a new symbol, new simulation, footprint has been created in this component, also has been included in AraMiS_Altium_Lib_Extra.
- Bk1B671D_Thermal_Fuser_Parallel_MOS (parallel MOSFET thermal fuser): a new symbol and new simulation, footprint has been created in this component, also has been included in AraMiS_Altium_Lib_Extra.
- CubeSat_1U_Frame_1B111E1 (the board frame): a new symbol and footprint has been created in this component, also has been included in AraMiS_Altium_Lib_Extra.
- Bk1B671E_Pad_Fuser (pad fuser): a new symbol and footprint has been created in this component, also has been included in AraMiS_Altium_Lib_Extra.

2.2.2. Footprint.

For the proposed of facilitate the explanation about how the different components were made, a single element has been chosen and explained step by step.

In this case, DK_587-1628-1-ND, the coil, has been chosen, which database is AraMiS_Altium_Lib.

The program used for a component creation is Altium, as previously stated, it can be beginning by symbol design or footprint design. At the moment it will start for the footprint. First, it has been searched the component in the home store (Digi-key), in order to take it datasheet.

Once datasheet is obtain, the code has been searched so as to obtain it features, measures, tolerance, inductance, etc., these characteristics are necessary to be able design the footprint that must be stored in the database.

Induttanza (µH)	Tolleranza (±)	Resistenza in c.c. max (Ω)	Corrente aumento temp. (mA)	N. di articolo Digi-Key	Prezzo su nastro pre-tagliato 1	10	100	Nastrati in bobina‡ Q.tà	Prezzi	N. di articolo Taiyo Yuden
Tipo CBC3225										
1.0	20%	715	1,440	587-1622-1-ND†§	.51	4.05	24.42	1,000	92.89	CBC3225T1R0MR
2.2	20%	104	1,130	587-1623-1-ND†§	.51	4.05	24.42	1,000	92.89	CBC3225T2R2MR
4.7	20%	130	1,010	587-1624-1-ND†§	.51	4.05	24.42	1,000	92.89	CBC3225T4R7MR
10	20%	172.9	900	587-1625-1-ND†§	.51	4.05	24.42	1,000	92.89	CBC3225T100MR
22	20%	351	780	587-1626-1-ND†§	.51	4.05	24.42	1,000	92.89	CBC3225T220MR
47	20%	871	480	587-1627-1-ND†§	.51	4.05	24.42	1,000	92.89	CBC3225T470MR
100	20%	1,820	340	587-1628-1-ND†§	.51	4.05	24.42	1,000	92.89	CBC3225T101MR

Figure 19. Extract of datasheet.

Therefore, the design of the footprint can be done, the next step is to take the item number to be able know the size of the footprint.

Tipo	Dimensioni – in. (mm) L	W	T	E
CBC3225	0.126 ±0.008 (3.2 ±0.2)	0.098 ±0.008 (2.5 ±0.2)	0.098 ±0.008 (2.5 ±0.2)	0.024 ±0.012 (0.6 ±0.3)
CB2518, CBC2518	0.098 ±0.008 (2.5 ±0.2)	0.071 ±0.008 (1.8 ±0.2)	0.071 ±0.008 (1.8 ±0.2)	0.020 ±0.008 (0.5 ±0.2)
CB2016, CBC2016	0.079 ±0.008 (2.0 ±0.2)	0.063 ±0.008 (1.6 ±0.2)	0.063 ±0.008 (1.6 ±0.2)	0.020 ±0.008 (0.5 ±0.2)
CB2012, CBC2012	0.079 ±0.008 (2.0 ±0.2)	0.049 ±0.008 (1.25 ±0.2)	0.049 ±0.008 (1.25 ±0.2)	0.020 ±0.008 (0.5 ±0.2)
CBL2012	0.079 ±0.008 (2.0 ±0.2)	0.049 ±0.008 (1.25 ±0.2)	0.035 ±0.004 (0.9 ±0.1)	0.020 ±0.008 (0.5 ±0.2)
CBMF1608	0.063 ±0.2 (1.6 ±0.2)	0.031 ±0.008 (0.8 ±0.2)	0.031 ±0.008 (0.8 ±0.2)	0.015 ±0.006 (0.4 ±0.15)

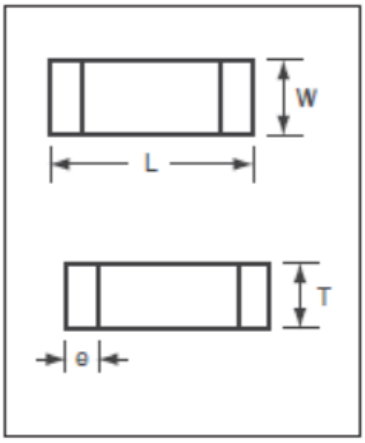


Figure 20. Size of footprint coil

Back to Altium, the footprint has been made, it has been selected the type of component, inductive, and it has been created a new element within this group (in this case SMD) where will be included.

Paying attention in each layer, the measure of datasheet has been followed and finally it has been obtained the footprint.

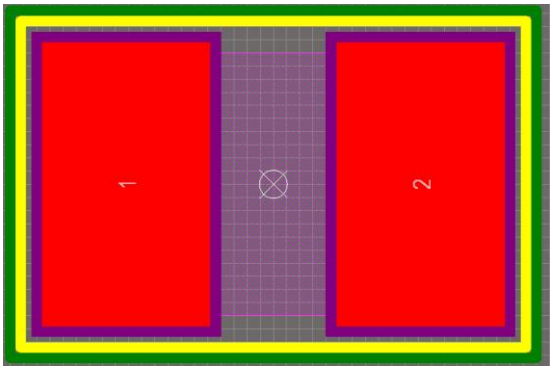


Figure 21. DK_587-1628-1-ND - Footprint coil design

The footprint is named in order to be stored in the database and to be able to unify with the symbol and the simulation, in this case it has been named *1210*.

2.2.3. Symbol.

Next, it has been created the symbol, since this case is a coil, the symbol which has been created is generic. Therefore it has been created this symbol with it name. The symbol also needs to be named.

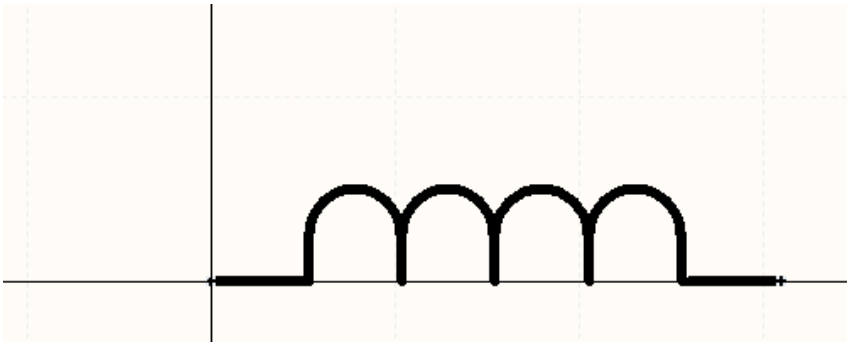


Figure 22. DK_587-1628-1-ND - Symbol coil design.

The addition of the component in the database is the following step. The databases have different features to be classified, the most important to be highlighted are:

- Part Name: It is the name of the component.
- Part Number: It's the number of the component.
- Library Ref: reference code of the symbol in Altium.
- Library Path: localization file of the symbol.
- Part Label: reference code of the symbol in Access.
- Footprint: name of the footprint in the Access.
- Package Reference
- Footprint Path: localization file of the footprint.
- Footprint Ref: footprint name in Altium
- Sim File: localization file of the simulation.
- Sim Model Name: Name of the simulation.

The method of component creation was applied in the same way for the others elements, it could not had simulation or belong to the other library (AraMiS_Altium_Lib_Extra). Others components like thermal fuser has had been design with no previous reference from any datasheet.

Chapter 3

3. Thermal fuser models.

The models of the thermal fuser have not been designed by any manufacturer, this means that their simulation cannot be able obtained from any website. It have been simulated in order to check the correct operation.

The simulate elements are:

- Bk1B671A_Thermal_Fuser_Series.
- Bk1B671B_Thermal_Fuser_Series_MOS.
- Bk1B671C_Thermal_Fuser_Parallel.
- Bk1B671D_Thermal_Fuser_Parallel_MOS.

3.1. Develop of the code model.

WordPad has been the program to develop the simulation code. As in the last section, in order to simplify the explanation a model has been chosen, the most important in the project is Bk1B671C_Thermal_Fuser_Parallel_MOS (point 2.3.1 explain why).

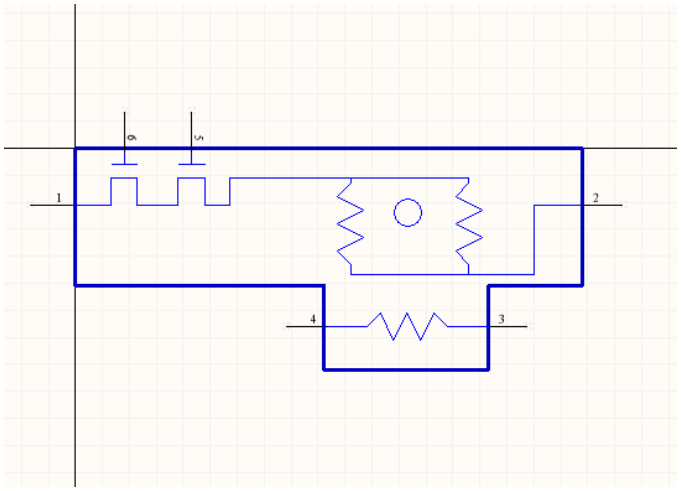


Figure 23. Bk1B671D_Thermal_Fuser_Parallel_MOS - symbol.

A code has been created in WordPad, the fuser is composed by different elements model, a NTC100, two resistors in parallel and a MOSFET, for this reason the code is differentiated in several parts.

Part 1.

```
.SUBCKT Bk1B671D_Thermal_Fuser_Parallel_MOS 1 2 3 4 5 6
R1 10 2 240
R2 10 2 240
X1 3 4 NTC100K
X2 11 5 11 1 6 10 irlhs6376pbf
```

In this part the pins have been declared with their components as in figure X, the value of the resistors and the nodes between each components have also been declared, where *X1* and *X2* are a designator, and *irlhs6376pbf* is the MOSFET.

Part 2.

The first lines of the code declare the connection of the NTC in the component and the value of it parameters.

```
.SUBCKT NTC100K 1 2
+ PARAMS: TOL=0
+ B0=-14.5737389
+ B1=4734.87
+ B2=-99567.95
+ B3=-5091275.72
+ B4=40082796.5
+ R25=100000
+ CTH=0.012 GTH0=0.00246 GTH1=0 TK=273.15
*
Gthem 1 2
Value={V(1,2)/(R25*(1+TOL/100)*(exp((((B4/(V(3)+TK+TEMP)+B3)/(V(3)+TK+TE
MP)+B2)/(V(3)+TK+TEMP)+B1)/(V(3)+TK+TEMP)+B0)))}
*
RP 1 2 1T
*
Gtmp1 0 3
Value={V(1,2)*V(1,2)/(R25*(1+TOL/100)*(exp((((B4/(V(3)+TK+TEMP)+B3)/(V(3
)+TK+TEMP)+B2)/(V(3)+TK+TEMP)+B1)/(V(3)+TK+TEMP)+B0)))}
C_par 3 0 {CTH}
R_par 3 0 1T
Gpar  3 0 Value={V(3)*(GTH0+(GTH1*(V(3)+TEMP)))}
*
.ends
```

Part 2 shows the model simulation of the NTC, which will calculate the value of the temperature in function of the voltage. This code has been extract from the datasheet of the NTC.

Part 3.

The code start with the declaration of the connection of the MOSFETs in the component.

```
.SUBCKT irlhs6376pbf 1 2 3 4 5 6
X1 6 2 1 irlhs6376pbf-SINGLE
X2 3 5 4 irlhs6376pbf-SINGLE
.SUBCKT irlhs6376pbf-SINGLE 1 2 3
* SPICE3 MODEL WITH THERMAL RC NETWORK
**************************************
*      Model Generated by MODPEX     *
*Copyright(c) Symmetry Design Systems*
*         All Rights Reserved        *
*    UNPUBLISHED LICENSED SOFTWARE   *
*   Contains Proprietary Information *
*      Which is The Property of      *
*     SYMMETRY OR ITS LICENSORS      *
*Commercial Use or Resale Restricted *
*   by Symmetry License Agreement    *
**************************************
* Model generated on Nov 21, 11
* MODEL FORMAT: SPICE3
* Symmetry POWER MOS Model (Version 1.0)
* External Node Designations
* Node 1 -> Drain
* Node 2 -> Gate
* Node 3 -> Source
M1 9 7 8 8 MM L=100u W=100u
.MODEL MM NMOS LEVEL=1 IS=1e-32
+VTO=1.31248 LAMBDA=0.0497001 KP=29.3563
+CGSO=2.59003e-06 CGDO=1.45749e-07
RS 8 3 0.0338159
D1 3 1 MD
.MODEL MD D IS=1e-17 RS=0.0437879 N=0.617647 BV=30
+IBV=0.00025 EG=1.2 XTI=1 TT=1e-07
+CJO=4.69616e-11 VJ=4.99996 M=0.841611 FC=0.5
RDS 3 1 5e+07
RD 9 1 0.0001
RG 2 7 16.8802
D2 4 5 MD1
* Default values used in MD1:
*   RS=0 EG=1.11 XTI=3.0 TT=0
*   BV=infinite IBV=1mA
.MODEL MD1 D IS=1e-32 N=50
+CJO=1.75007e-10 VJ=0.539795 M=0.845354 FC=1e-08
D3 0 5 MD2
* Default values used in MD2:
*   EG=1.11 XTI=3.0 TT=0 CJO=0
*   BV=infinite IBV=1mA
.MODEL MD2 D IS=1e-10 N=0.458926 RS=3e-06
RL 5 10 1
FI2 7 9 VFI2 -1
VFI2 4 0 0
EV16 10 0 9 7 1
CAP 11 10 2.33591e-10
FI1 7 9 VFI1 -1
VFI1 11 6 0
RCAP 6 10 1
D4 0 6 MD3
* Default values used in MD3:
*   EG=1.11 XTI=3.0 TT=0 CJO=0
*   RS=0 BV=infinite IBV=1mA
.MODEL MD3 D IS=1e-10 N=0.458926
.ENDS irlhs6376pbf

*SPICE Thermal Model Subcircuit
.SUBCKT irlhs6376pbft 3 0
```

```
R_RTHERM1          3 2  7.406833675
R_RTHERM2          2 1  9.689893537
R_RTHERM3          1 0  1.887219931
C_CTHERM1          3 2  0.000335895
C_CTHERM2          2 1  0.001687426
C_CTHERM3          1 0  6.07579e-05

.ENDS irlhs6376pbft-SINGLE
.ENDS

.ENDS
```

Part three shows the simulation of the MOSFETs as in part 2, this code has been provide by the manufacture.

3.2. TEST_Bk1B6712_Fuser_System_X_X.

Once the code has been made, the next step is to design a project simulation in Altium.

In this case, a project named *Bk1B6712_Fuser_System_Parallel_MOS* has been generated for the simulation, in the schematic, four inputs and one output have been connected to the thermal fuser.

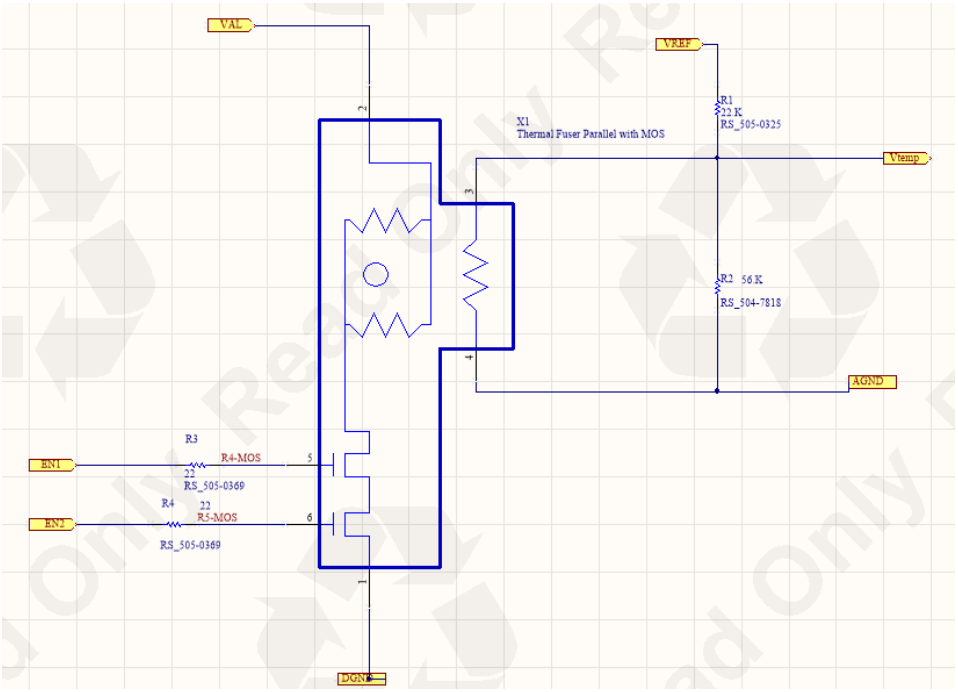


Figure 24. Bk1B6712_Fuser_System_Parallel_MOS.

Then, a test bench has been created for the simulation, which has been named *TEST_Bk1B6712_Fuser_System_Parallel_MOS*, it project is composed by two schematics, *Bk1B6712_Fuser_System_Parallel_MOS* and other called *TEST_Bk1B6712_Fuser_System_Parallel_MOS.*

The schematic sheet *TEST_Bk1B6712_Fuser_System_Parallel_MOS* contain a device sheet symbol of thermal fuser.

Two voltage source and two pulse voltage source have been connected to the device sheet symbol.

The voltage source 1 (V1_VSRC) is connected to the parallel resistors (VREF) the value of this source is 3V, this supply is the voltage reference used to measure the temperature in NTC100.

The voltage source 2 (V2_VSRC) is connected to the MOSFET (VAL), its value is 14V, according to the Aramis specifications. The function of this supply is to provide the resistors in order to produce the Joule effect.

The two Voltage Pulse Sources are connected to the MOSFET (EN1 and EN2), its goals is to drive the current of the resistors, thus control the Joule effect.

Finally the temperature will be shown by the NTC100 of the thermal fuser which is connected to the output Vtemp, the connection is indicated in the figure X.

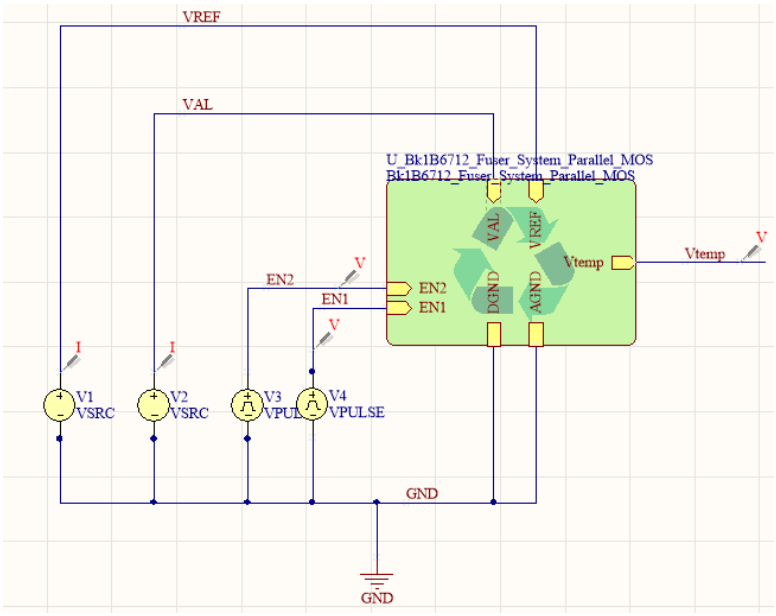


Figure 25. TEST_Bk1B6712_Fuser_System_Parallel_MOS

The value for the sources are shown in the table X.

	Value	AC Magnitude	AC Phase
V1 Voltage source	3V	-	-
V2 Voltage source	14V	-	-

Table 6. VSRC, parameters

	DC Magnitude	AC Magnitude	AC Phase	Initial Value	Pulsed Value	Time Delay	Rise Time	Fall Time	Pulse Width	Period
V3 Pulse Voltage source	0	1	0	0	3.3V	1m	1u	1u	4m	10m
V4 Pulse Voltage source	0	1	0	0	3.3V	2m	1u	1u	4m	10m

Table 7. VPULSE, parameters.

The project has been compiled and has been generated a 'Mixed Sim' netlist to detail information about the simulation process.

```
TEST_Bk1B6713_Fuser_System_Parallel
*SPICE Netlist generated by Advanced Sim server on 18/07/2018 11:31:13

*Schematic Netlist:
R2 Vtemp VREF 22.K
R3 0 Vtemp 56.K
R4 EN1 NetR4_2 22.
R5 EN2 NetR5_2 22.
XU2 NetU2_1 NetR4_2 NetU2_1 0 NetR5_2 NetU2_6 irlhs6376pbf
V1 VREF 0 3
V2 VAL 0 14
V3 EN2 0 DC 0 PULSE(0 3.3 1m 1u 1u 4m 10m) AC 1 0
V4 EN1 0 DC 0 PULSE(0 3.3 2m 1u 1u 4m 10m) AC 1 0
X1 NetU2_6 VAL Vtemp 0 Bk1B671C_Thermal_Fuser_Parallel
```

This part of netlist it can verify the connection of the components and the sources are correct.

Last, the simulation has been executed.

In the same way, the simulation of the others thermal fuser have been done, therefore, the representations of the simulations are shown next. Two kinds of simulations have been done for the thermal fusers: Transient analysis and DC sweep analysis.

3.2.1. Transient analysis

This analysis is useful to know behaviour of the MOSFETs in the thermal fuser, whose function in the component is to enable the pass of the current to the resistors and thus produce the melt in the wire of the thermal fuser.

The first graph show the behaviour of the MOSFETs, that is when works each one. In the simulation two MOSFETs has been simulated with a time delay of 2ms, therefore the current can only reach the resistance when both are working, in that case it will produced a voltage of 3.3V.

On the other hand the second graph shows the behaviour of the current that pass to the resistors as a function of time. When both MOSFTs are working the current that passes reaches a value next to 107mA necessary to produce the Joule effect in the resistances.

Depending of the resistance configuration (series or parallel) the current reaches can be: 103mA, for the fuser system series or 117mA for the fuser system parallel.

1. *TEST_Bk1B6713_Fuser_System_Parallel_MOS Simulation*.

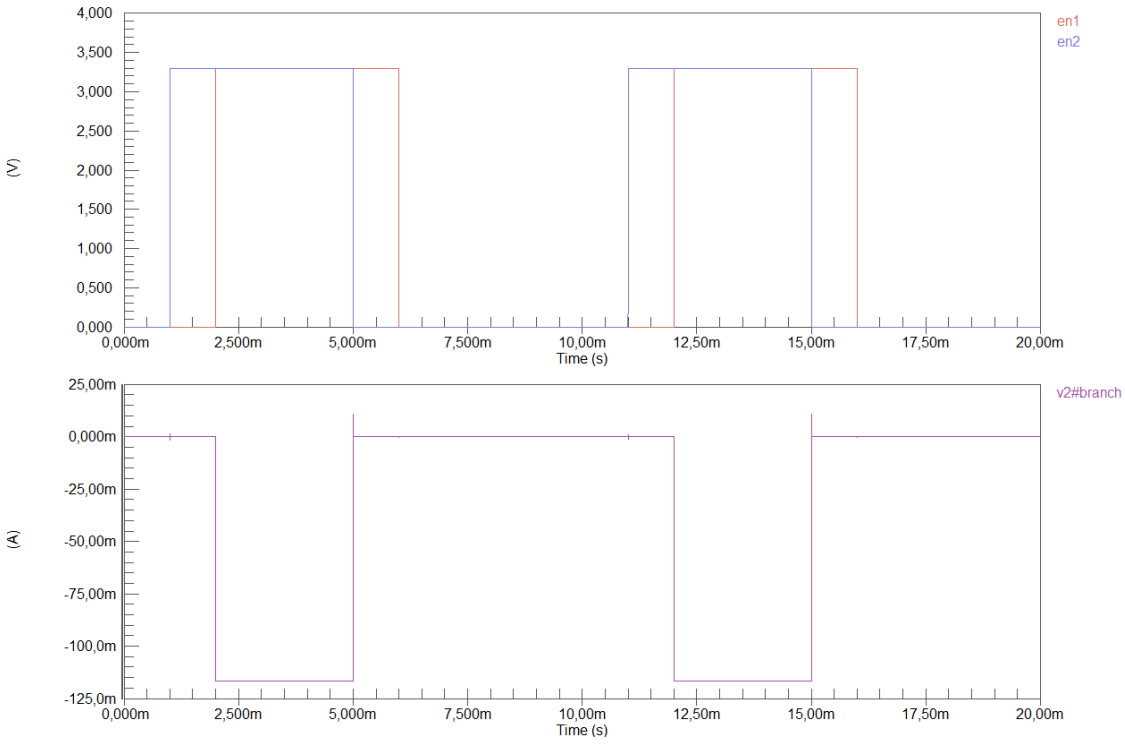


Figure 26. TEST_Bk1B6713_Fuser_System_Parallel_MOS Simulation (Transient analysis).

2. *TEST_Bk1B6713_Fuser_System_Parallel Simulation.*

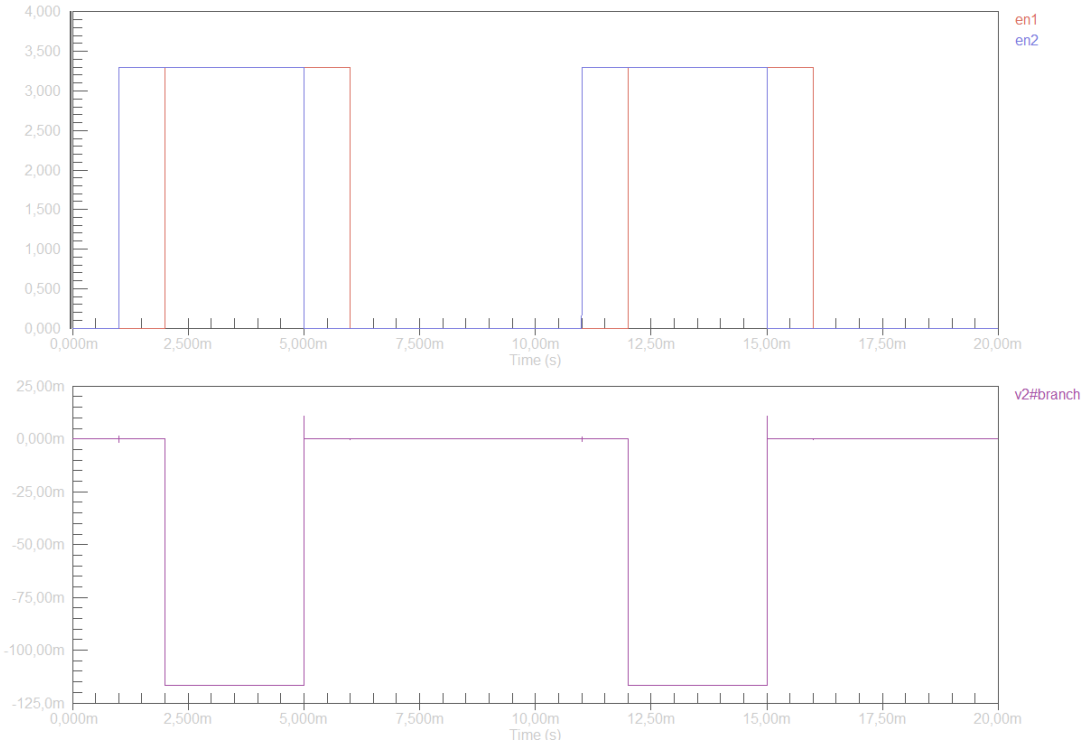


Figure 27. TEST_Bk1B6713_Fuser_System_Parallel Simulation (Transient analysis).

3. *TEST_Bk1B6713_Fuser_System_Series Simulation.*

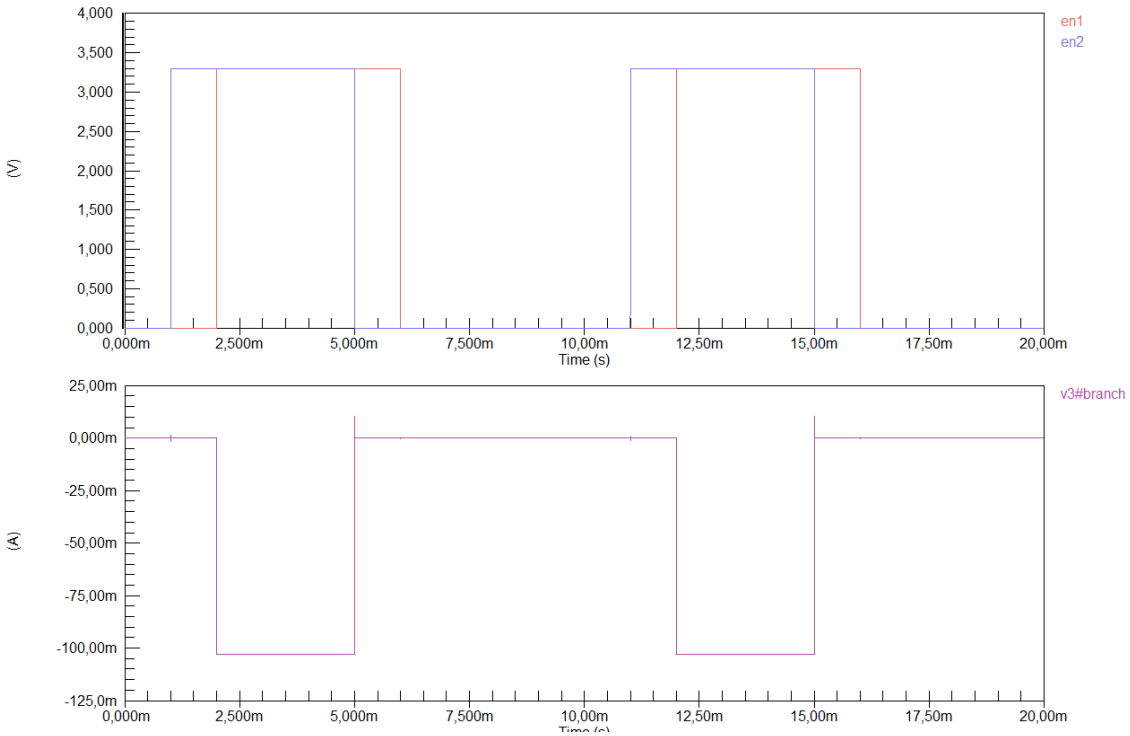


Figure 28. TEST_Bk1B6713_Fuser_System_Series Simulation (Transient analysis).

4. *TEST_Bk1B6713_Fuser_System_Series_MOS Simulation.*

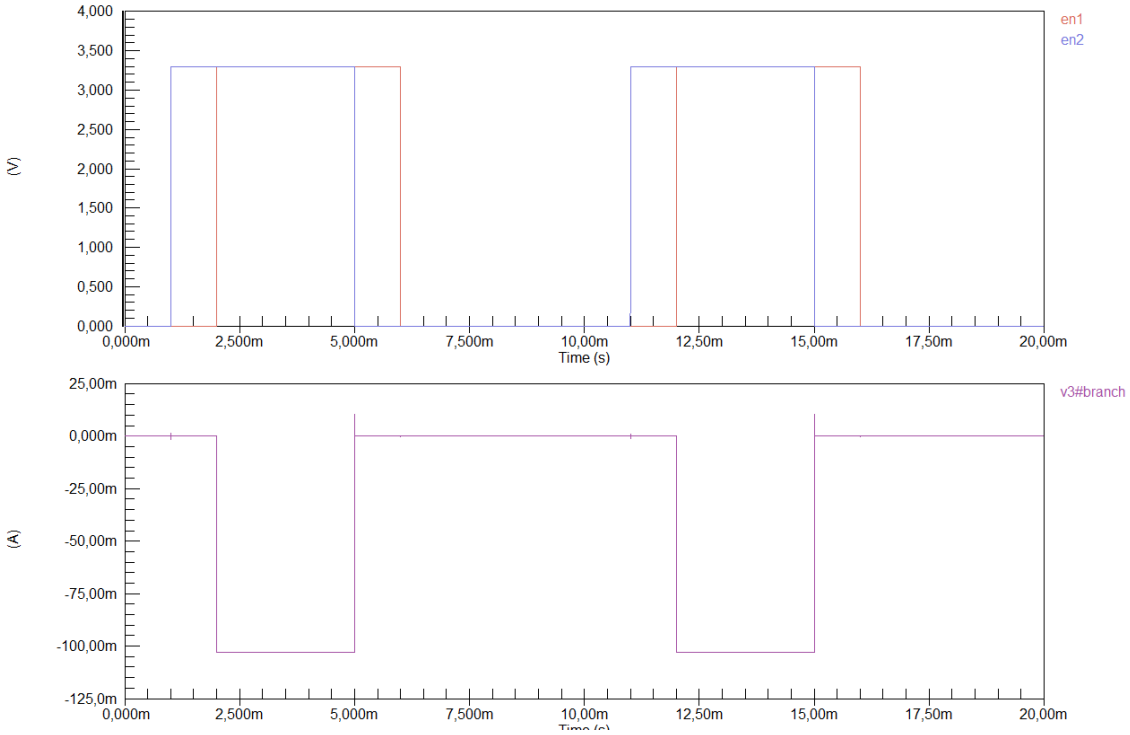


Figure 29. TEST_Bk1B6713_Fuser_System_Series_MOS Simulation (Transient analysis).

3.2.2. DC sweep analysis.

This analysis shows the behaviour of the temperature in the thermal fuser depending of the temperature. When the voltage decrease the temperature increase. The control of the temperature is necessary in order to avoid the damage of some component.

For this simulation has been chosen these temperatures:

Start Temperature	0°C
Step Temperature	20°C
Stop Temperature	180°C

Table 8. Parameters of DC sweep analysis.

1. *TEST_Bk1B6713_Fuser_System_Parallel_MOS Simulation.*

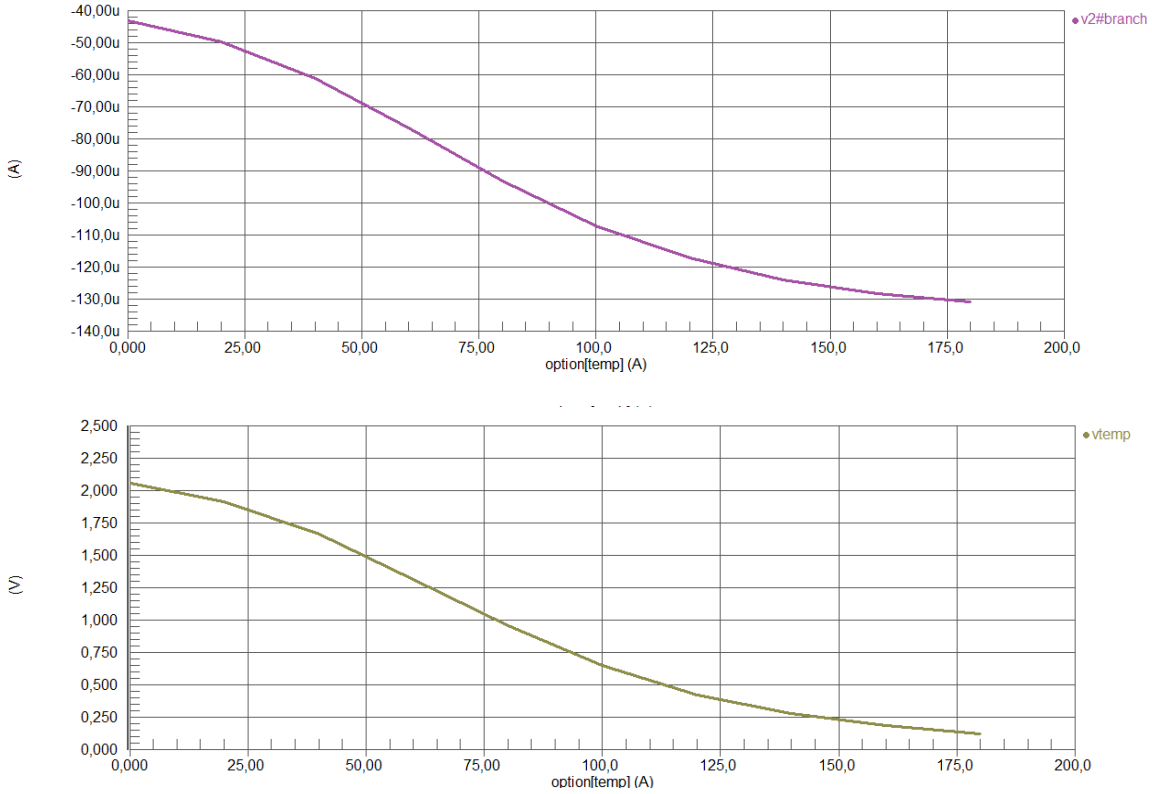
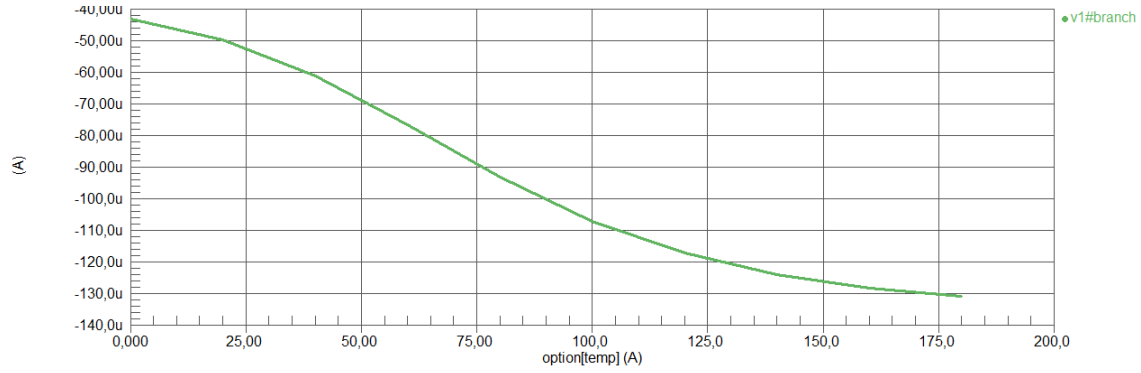


Figure 30. TEST_Bk1B6713_Fuser_System_Parallel_MOS Simulation (DC sweep analysis).

2. *TEST_Bk1B6713_Fuser_System_Parallel Simulation.*



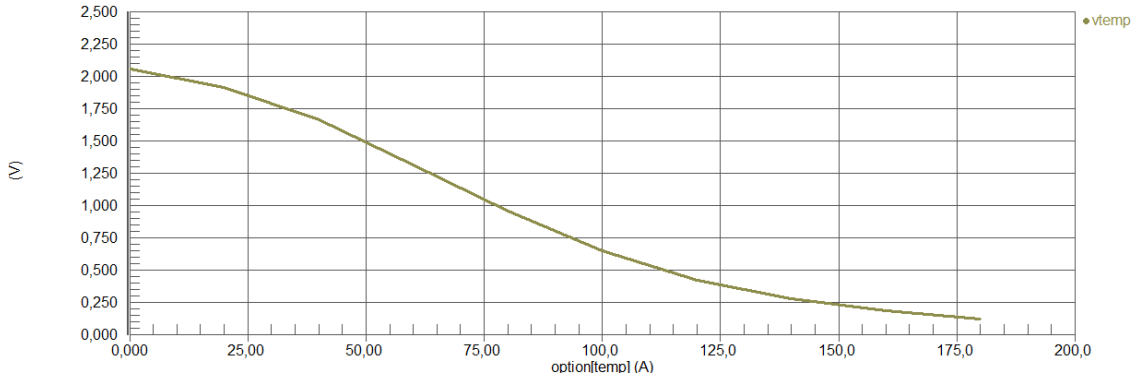


Figure 31. TEST_Bk1B6713_Fuser_System_Parallel Simulation (DC sweep analysis).

3. *TEST_Bk1B6713_Fuser_System_Series Simulation.*

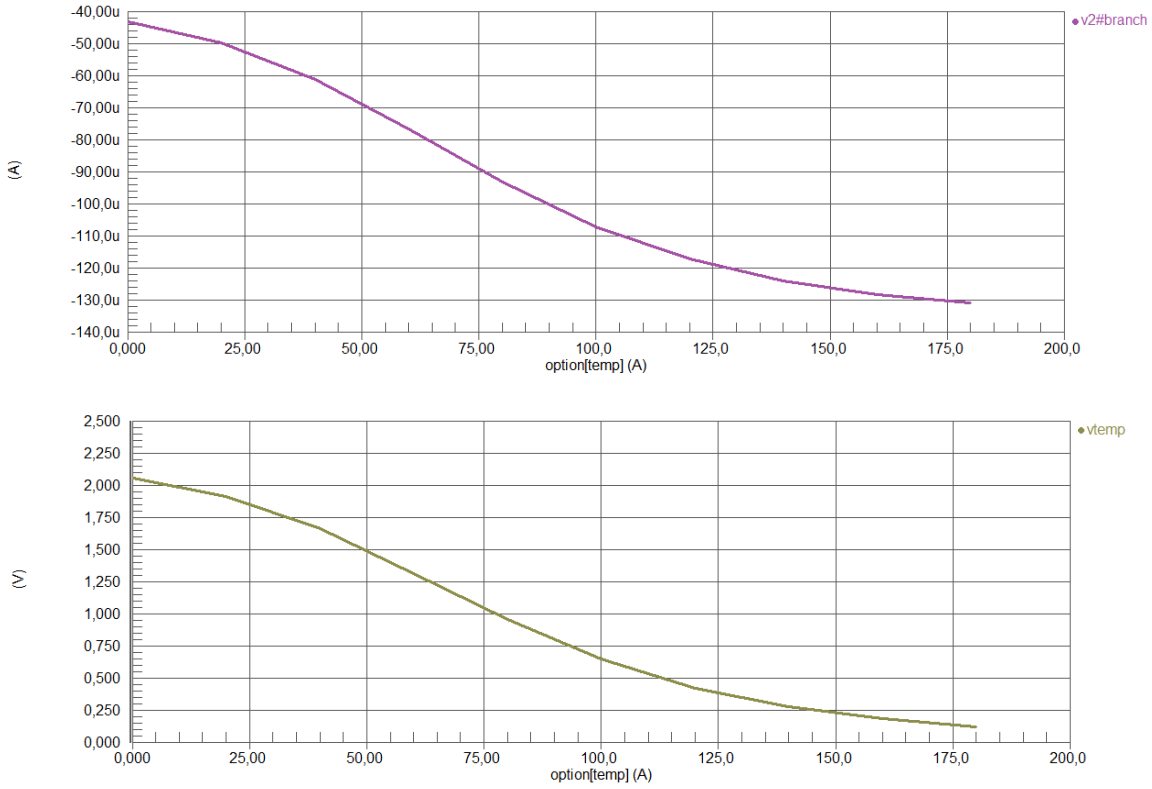


Figure 32. TEST_Bk1B6713_Fuser_System_Series Simulation (DC sweep analysis).

4. *TEST_Bk1B6713_Fuser_System_Series_MOS Simulation.*

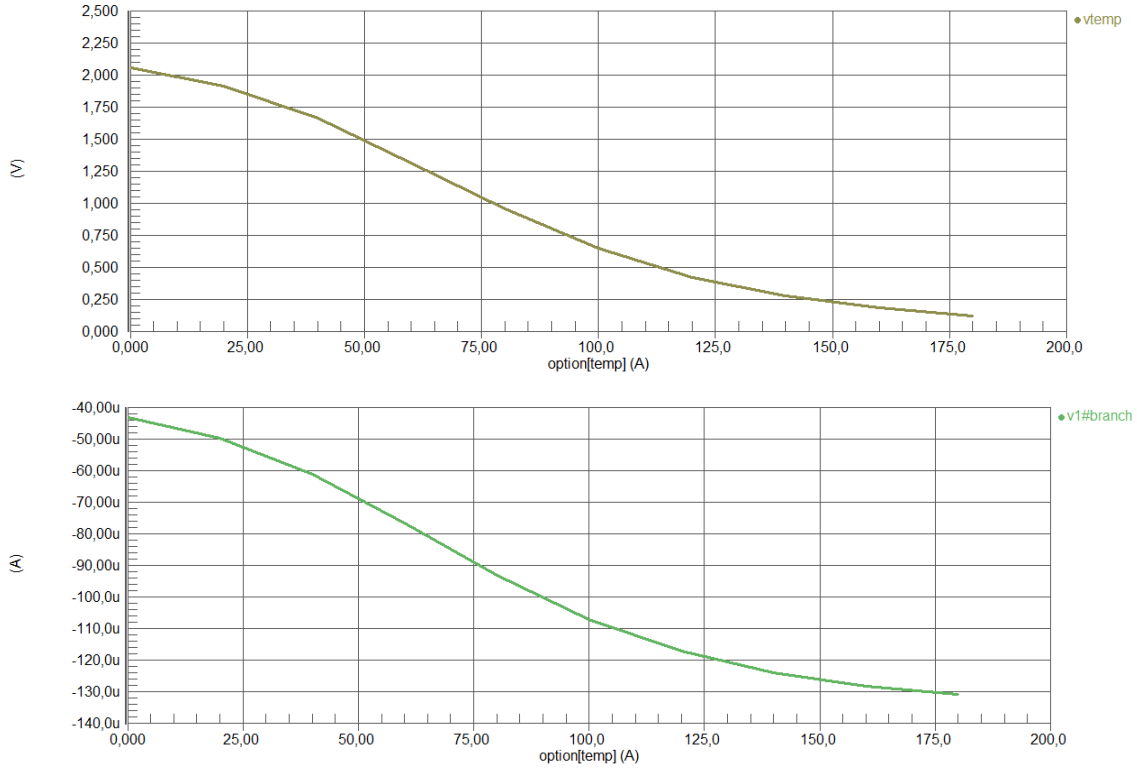


Figure 33. TEST_Bk1B6713_Fuser_System_Series_MOS Simulation (DC sweep analysis).

Chapter 4.

4. Bk1B111E board.

This chapter is entire dedicated to *Bk1B11E* board, in previous chapters the components, their simulation and features has been seen. With all this information the board has been design and assembly.

First of all a schematic has been done, in the schematic is easy to know how the connection is. Then, the simulation of schematic has been done, in this manner, verify of the circuit has been done. In second of all the PCB of *Bk1B11E* keeping in mind all the restrictions required. To end the chapter, the files necessary as GERBER or a 3D model have been done.

4.1. Schematic of *Bk1B111E20_DepTilePanel_1U*.

As was previously mentioned, ARAMIS CubeSat is composed by three deployed tiles. These tiles are formed for *Bk1B111E* board and are connected between them by *J_8_CABLE_FFC*. The board has four solar cells, two on the top and another two on the bottom, so that, a part of the satellite will be always exposed to the sun. The solar cells are connected in series in all the deployed structure.

In figure X the schematic has been represented with all of the components connected.

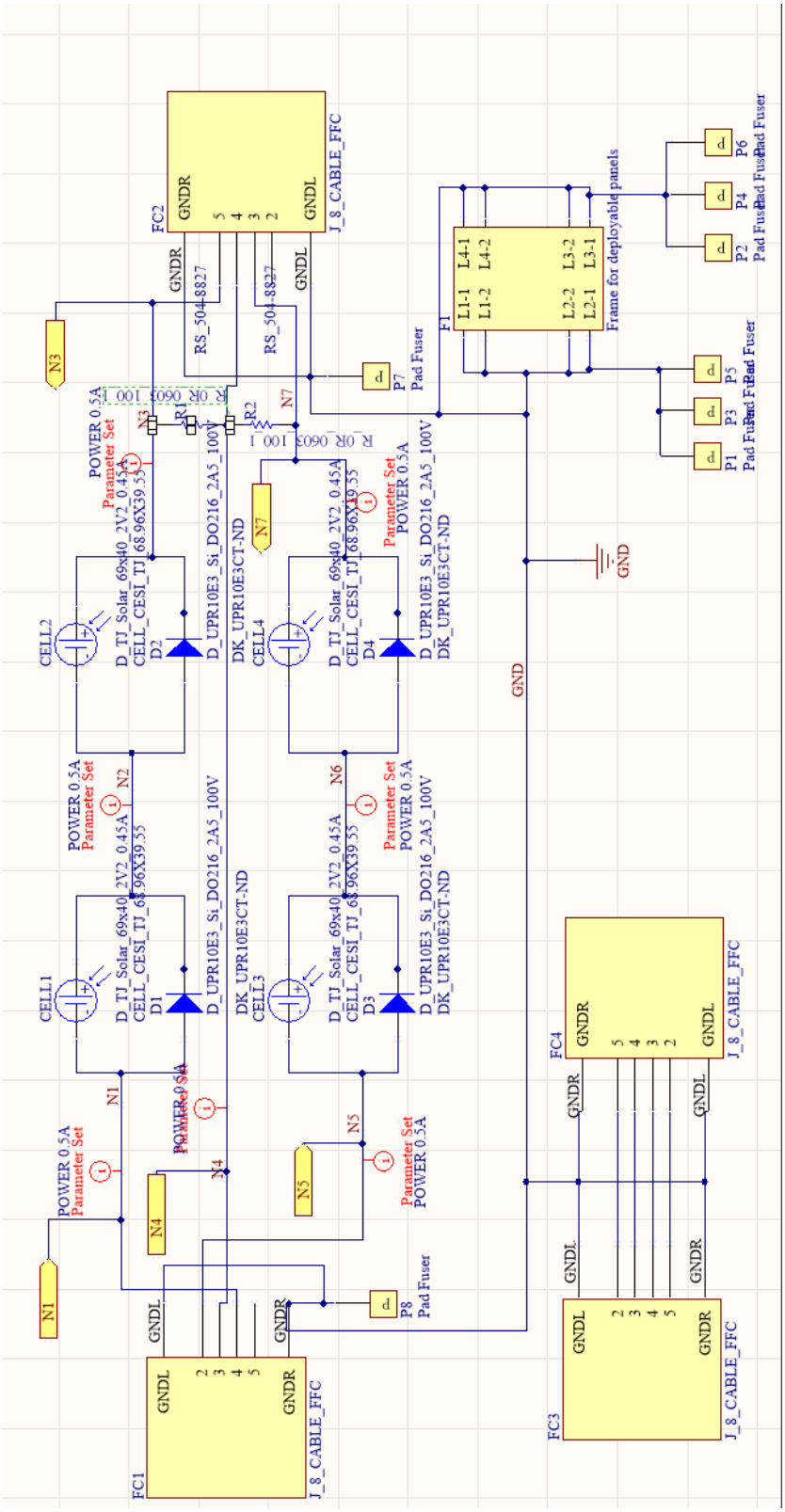


Figure 34. Bk1B111E20_DepTilePanel_1U schematic.

Each solar cell has one bypass diode connected in parallel, the reason is the connection of the series circuit. When there are no shadows and the solar cells work correctly, all of them receive radiation, therefore function as a source, in this case the bypass diode does not allow to pass the current and it will drive to the next solar cell.

In the case one solar cell were damage or does not were fully illuminated, some of them will behave as resistive, becoming in energy consumers, in the absence of radiation the bypass diode does not allow pass the current. The solar cell will be disabled without breaking the connection with the others elements and allow the operation of them, although the yield will be lower. Thus the deterioration will be avoid.[8]

The connector *J_8_CABLE_FFC* has eight pins, two of them are used for the solar cells, two for the GROUND and one is disable.

The connection from the pin 4 of FC1 to the pin 5 of FC2 of the *J_8_CABLE_FFC* represents the top of the board where CELL1 and CELL2 are connected, and pin 2 of FC1 to pin 3 of FC2 represents the bottom of the board where CELL 3 and CELL 4 are connected. And finally pin 3 of FC1 is connected with pin 4 of FC2, this wire is the negative of the circuit.

At the end of the connection two resistances have been connected, the resistances are connected at the end of the tiles, and the value of them is 0 Ω. The resistances are used to close the circuit.

The *Frame for deployable panels* has been included in the schematic, they are connected to the *Pad Fusers* which have to pass through the board. *Pad Fuser* are connected symmetrically three on one side, three on the other side, one on the top and one on the bottom, all of them are exactly matched with the *Pad Fusers* of the *Bk1B6711* board.

In the schematic has been also include another two *J_8_CABLE_FFC* (FC3 and FC4) this is due to allowing others future connections as an antenna, or any other element.

4.1.1. Simulation of *Bk1B111E20_DepTilePanel_1U*.

A simulation of the connection of *Bk1B111E20_DepTilePanel_1U* has been done, thus has been possible to check the correct work of the system.

For this simulation has been created a sheet symbol, which has been connected to a voltage source of 4.4V. Each side of the deployable solar panels' structure 1B111E is composed by a power channel in order to transfer power into the CubeSat. Thus, the deployable solar panels' structure has two power channel, positive and negative. The negative of the source has been connected to the positive channel of the schematic circuit represented by Net 1 and Net 5, and the positive of the source has been connected to the negative channel.

Figure X shows the circuit of the simulation, the sheet symbol represents the entire circuit (*Bk1B111E20_DepTilePanel_1U*).

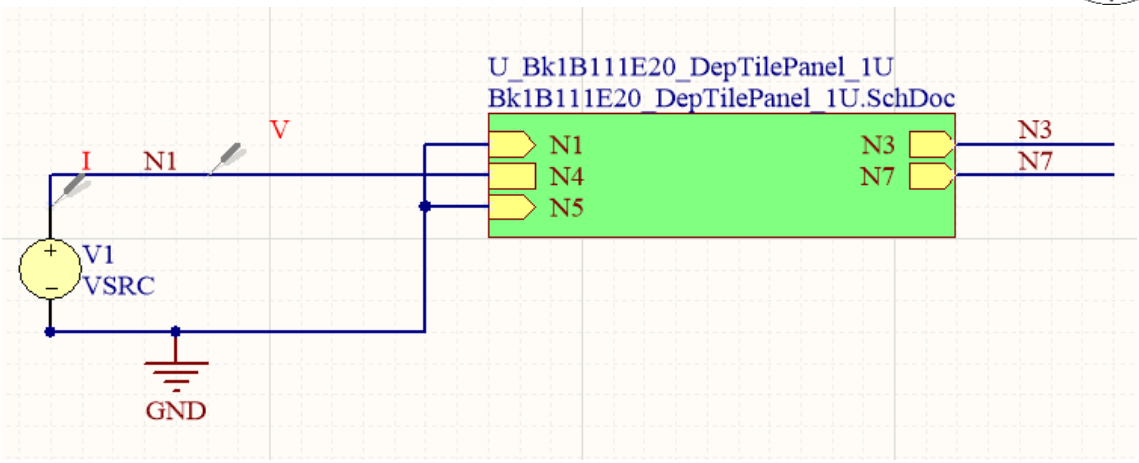


Figure 35. TEST_Bk1B111E20_DepTilePanel_1U circuit.

The Solar Cell I-V Characteristic Curves has been the result obtained, where is shown the current and voltage characteristics of the photovoltaic cells, giving a detailed description of its solar energy conversion ability and efficiency. Knowing the electrical I-V characteristics of the solar cell, is critical in determining the device's output performance and solar efficiency.

If the product of current and voltage is done, it would obtained the power delivered by the solar cell. For the multiplication done, point for point, for all voltages from short-circuit to open-circuit conditions, the power curve above is obtained for a given radiation level.

When the solar cell is become in open-circuited (not connected to any load) the current is at its minimum and the voltage across the cell is at its maximum, known as the solar cells open circuit voltage, (Voc). On the other hand, when the solar cell is short circuited, that is the positive and negative wire connected together, the voltage across the cell is at its minimum but the current flowing out of the cell reaches its maximum, known as the solar cells short circuit current, or Isc.

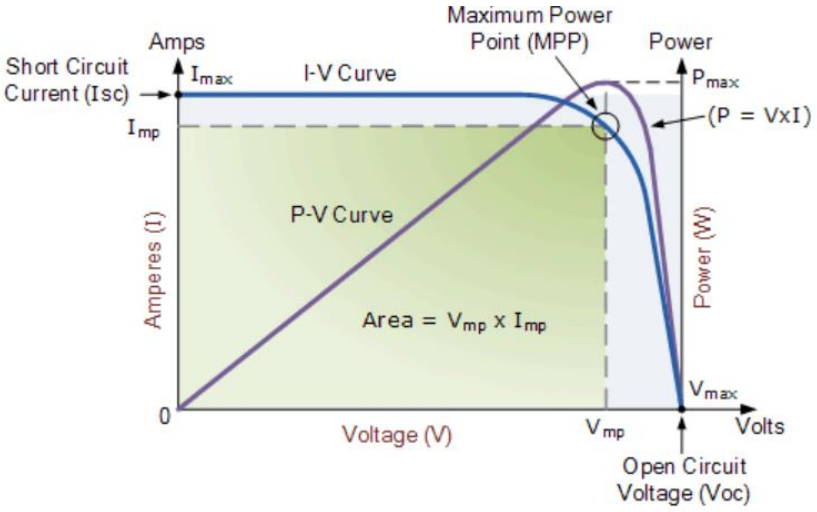


Figure 36. Characteristics curve explanation.

Then the span of the solar cell I-V characteristics curve ranges from the short circuit current, Isc, at zero output volts, to zero current at the full open circuit voltage, Voc. That's means, the maximum voltage available from a cell is at open circuit, and the maximum current at closed circuit. Neither of these two conditions generates any electrical power, but there must be a point somewhere in between were the solar cell generates maximum power.

The series combination of the solar cells connection produces the increase of the voltage, if were connected in parallel the current would be increase.[9]

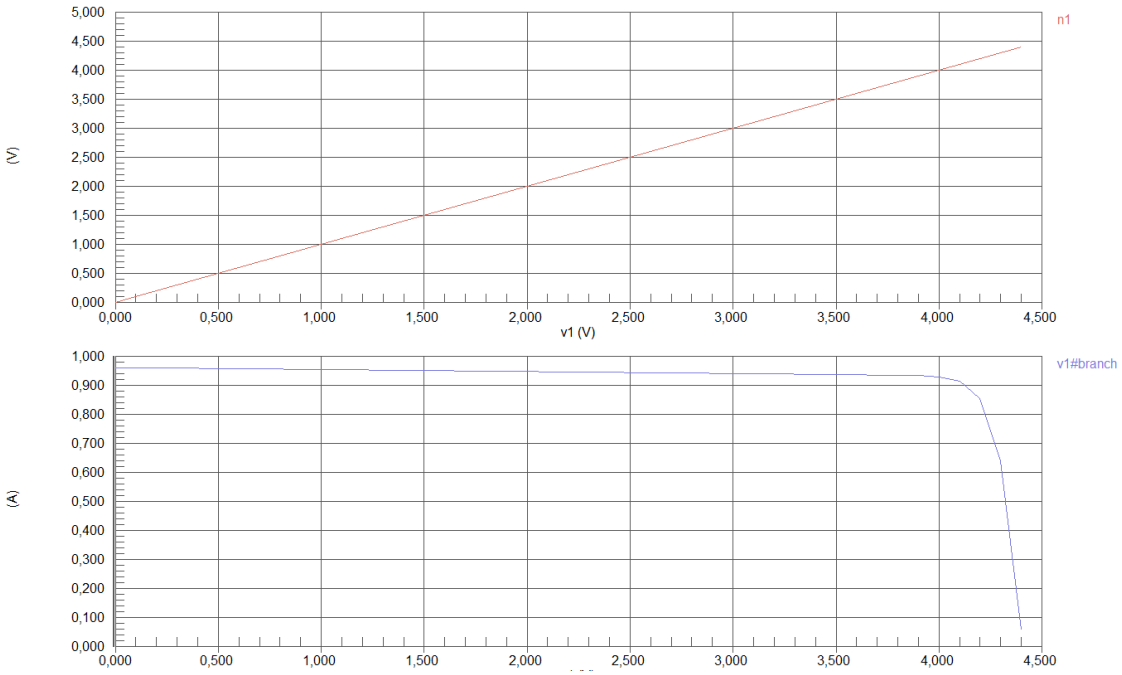


Figure 37. TEST_Bk1B111E20_DepTilePanel_1U.PrjPCB simulation.

4.2. Printed circuit board of *Bk1B111E20_DepTilePanel_1U*.

The main specifications of the printed circuit board of *Bk1B111E20_DepTilePanel_1U* as well as other characteristics of the board will be explained in this point. In this part of the project the final design of the board has been created. The correct placed of the components, the size of the wire or the holes, the space between each components or others details are really important for the objective of the mission.

The PCB was made from the schematic once it was designed in ALTIUM Design.

4.2.1. Components specifications.

Board size.

First of all the board has been designed with the same size as other board of ARAMIS as *Bk1B6711*, thus the symmetry is maintained. Both boards (*Bk1B6711* and *Bk1B111E20*) have to be symmetrical for the thermal fusers system, which have all the board joined. The size of the board is 82.6 x 98 mm (X=82.6; Y=98).

Pad fuser.

The *Pad Fusers* has been placed in the same position that thermal fusers of *Bk1B6711* in order to make possible pass the wire that keep the tiles together. The hole has been normalized, so that all of them have the same size in all of the boards.

Putting origin of the board as in figure X, all of the *Pad Fusers* have been placed.

.

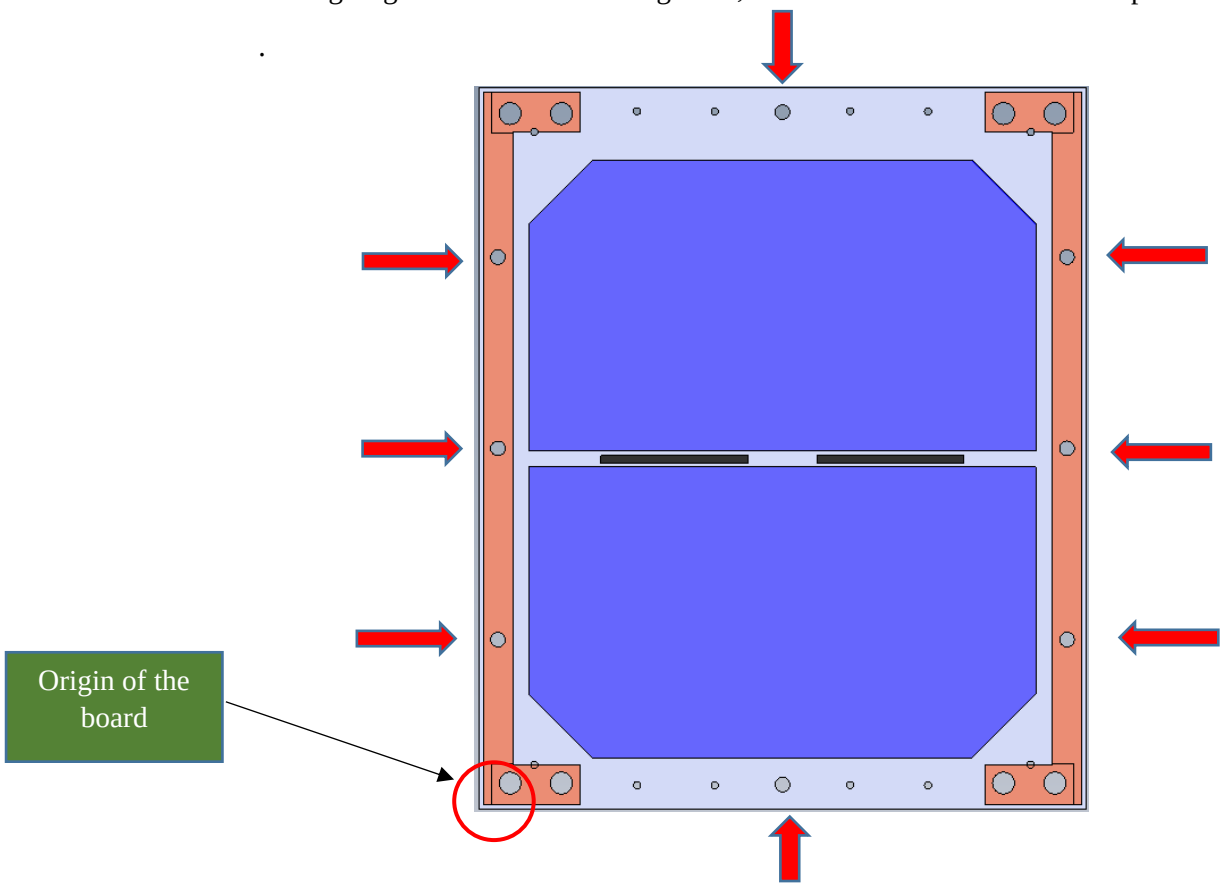


Figure 38. Origin of Bk1B111E20 board.

Pad Fusers have been placed in the following position:

Number	X (mm)	Y (mm)
Pad Fusers 1 (P1)	2.6	23
Pad Fusers 2 (P2)	80	49
Pad Fusers 3 (P3)	2.6	49
Pad Fusers 4 (P4)	80	75
Pad Fusers 5 (P5)	2.6	75
Pad Fusers 6 (P6)	80	23
Pad Fusers 7 (P7)	41.3	94.7
Pad Fusers 8 (P8)	41.3	3.3

Table 9. Pad fusers positions

Diodes.

There are four diodes in *Bk1B111E20* one per solar cell, that means two in each side of the board. The position of the diodes is important for two reasons.

The first reason is to avoid friction between each diode when the system is folded, when the system is folded the tiles are very close, therefore the top of the board will be face to face with the bottom. In case two elements coincide in a point the component could be damage. For this reason the position has been chosen carefully. Another consideration is to place others components sufficiently spaced.

Layer	Diode	X(mm)	Y(mm)
Top	D1	7.783	87.04
	D2	7.718	11.317
Bottom	D3	8.739	87.104
	D4	8.352	11.42

Table 10. Diodes position.

Solar Cells.

The solar cells are the component which occupies more spaced, there are two on the top and two on bottom.

In order to avoid problems of friction between both solar cells has been separate at least one millimetre, and have been placed symmetrically. Between CELL1 and CELL2 the separation is 2.44 millimetres and between CELL3 and CELL4 is 1.1 millimetres. The position of all of them is shown in the figure below.

Layer	Diode	X(mm)	Y(mm)
Top	CELL 1	41.65	69
	CELL 2	41.65	27
Bottom	CELL 3	41.65	69.95
	CELL 4	41.65	29.3

Table 11. Solar cell position.

Resistors.

The resistors are just assembled in the last tile, although its position in the board is important to not interfere with the other components and the wires. In this case there are only two resistors, and both are placed in the same layer (top), so it is not necessary to position the resistor in any specific place, because when the system is folded it will not touch any component.

Resistor	X (mm)	Y (mm)
R1	64.15	4.044
R2	66.732	4.026

Table 12. Resistors position.

Connectors.

The connectors are another element which position is really important. When the system is deployed, the three tiles are connected between them by the connectors *J_8_CABLE_FFC*, thus each solar cell is connected in series when it received the solar light. Although, while one side of the system receive light the other will be in the darkness, so to complete the circuit, all of the solar cell have to be working.

For this reason, if the wire are not correctly connected, the circuit formed by the tiles could be shorted, since if a wire from a working solar cell is connected to a side of the tile which are not illuminated the current could not get to the next tile and a short circuit would be produced.

In order to avoid this connectors have been placed as the table below.

Layer	Connector	X(mm)	Y(mm)
Top	FC1	21.5	94.8
	FC3	50.5	94.8
Bottom	FC2	21.5	3.2
	FC4	50.5	3.2

Table 13. J_8_CABLE_FFC *position.*

Bk1B111E20 board the connection has been the following:

- Connector 4 from FC1 has been connected to CELL1 and CELL2 this net arrive to the connector 5 of FC2.
- Connector 5 of FC2 is perfectly symmetric to connector 2 from FC1 of the next tile, thus the net of connector 2 connect CELL3 and CELL4 and it arrives to connector 3 of FC2.
- Connector 3 form FC2 is perfectly symmetric to connector 4 from FC1 of the next tile, thus closing the circuit.
- The GNDL and GNDR of the connector are connected to GND of the board.

On the other hand, connectors FC3 and FC4, which are integrate in the project for future design have the following connection:

- Connector 5 from FC4 is connected to connector 2 of FC3.
- Connector 4 from FC4 is connected to connector 3 of FC3.
- Connector 3 from FC4 is connected to connector 4 of FC3.
- Connector 2 from FC4 is connected to connector 5 of FC3.
- The GNDL and GNDR of the connector are connected to GND of the board.

The figure X below show how the connection are made.

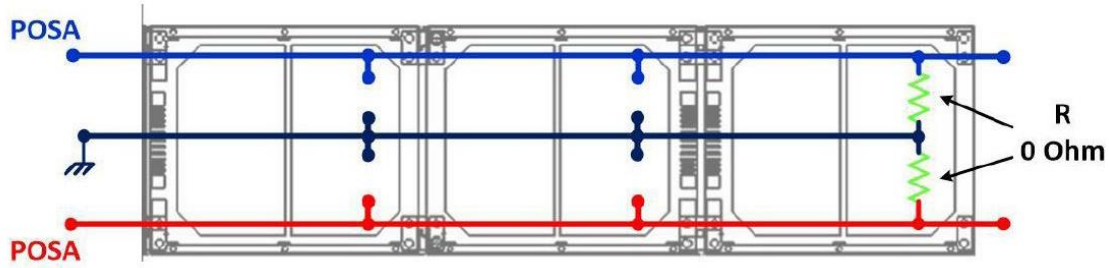


Figure 39. Connection of deployed system.

4.2.2. PCB Rules.

Nets.

In *Bk1B111E20* has been defined two different class for the nets. The standard net, which has been design for the connection between FC3 and FC4 connectors, this net has been thought for other possible functions of the satellite. On the other hand, the POWER 0.5A net has been designed for FC1 and FC2 connection, this net has more width since are connected to solar cells and by them will pass a current of 1A.

The table below show the value of the nets.

Net	0.254 mm	0.3-0.5 mm
GND	✓	-
N1	-	✓
N2	-	✓
N3	-	✓
N4	-	✓
N5	-	✓
N6	-	✓
N7	-	✓
NetFC3_2	✓	-
NetFC3_3	✓	-
NetFC3_4	✓	-
NetFC3_5	✓	-

Table 14. Net classes.

Due to the different nets, the vias have different size too, depending of the net they belong to.

Via	Diameter (mm)	Hole size (mm)
0.254 mm	0.7	0.3
0.3-0.5 mm	0.4	1

Table 15. Vias measure.

Layers.

For the board design has been used several kinds of layers, the most mentioned in this project have been top layer and bottom layer. Although another layers have been used. The features have been shown on the table below.

Layer name	Type	Material	Thickness (mm)	Dielectric material	Dielectric constant
Top Overlay	Overlay	-	-	-	-
Top Solder	Solder Mask/Coverlay	Surface Material	0.01016	Solder Resist	3.5
Top Layer	Signal	Copper	0.03556	-	-
Dielectric 1	Dielectric	None	0.32004	FR-4	4.8
Bottom Layer	Signal	Copper	0.03556	-	-
Bottom Solder	Solder Mask/Coverlay	Surface Material	0.01016	Solder Resist	3.5
Bottom Overlay	Overlay	-	-	-	-

Table 16. Layer stack manager.

It has been decided that surface finish is made of immersion gold, the reason is for the benefit of solar cells, since if it were made of tin, they would react chemically and this could damage the solar cells.

The final design of the PCB is reported in figures X and X. Figure X show the TOP side and figure X bottom side. Otherwise 3D view is shown in figure X (TOP) and figure X (bottom)

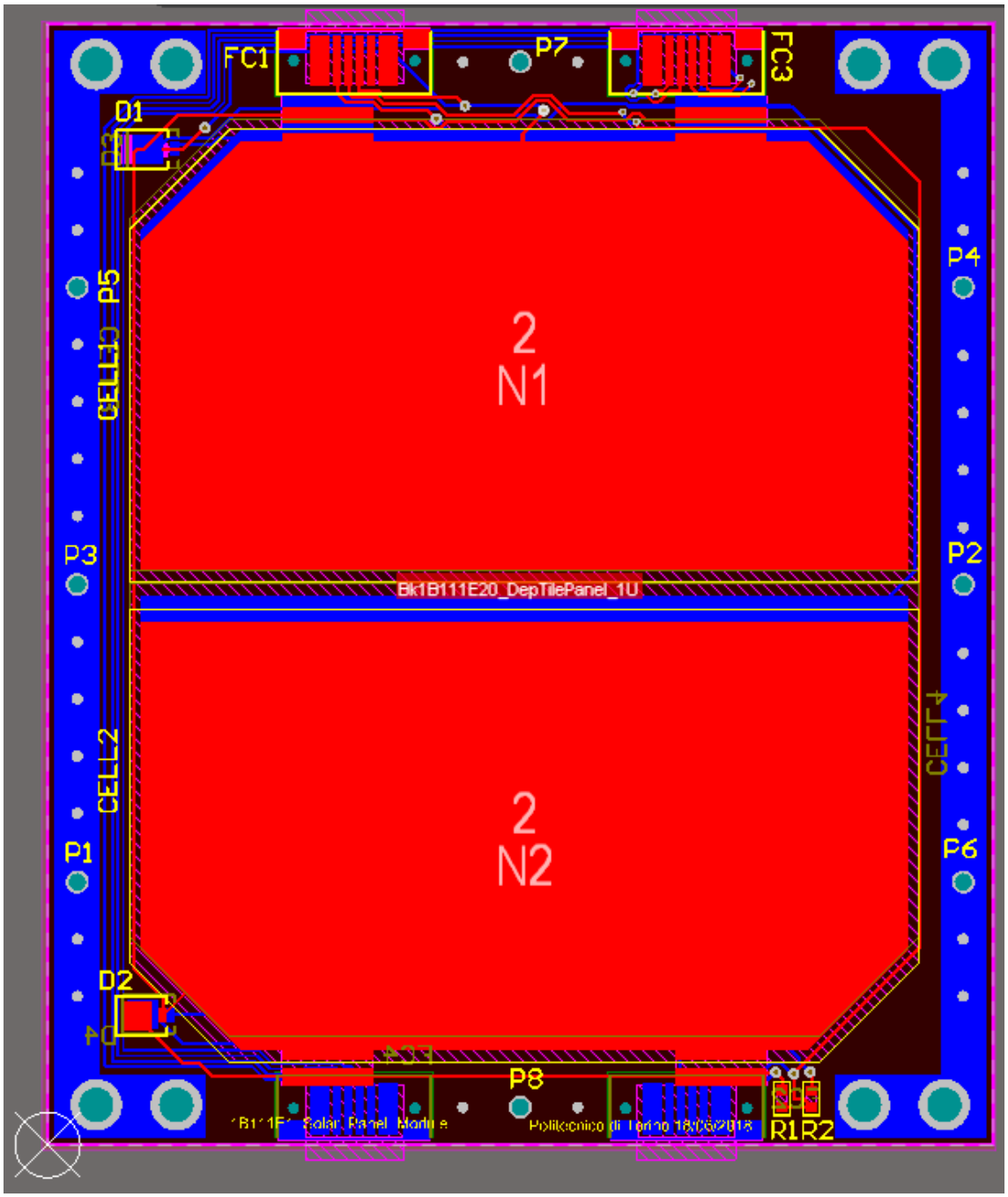


Figure 40. Bk1B111E20 PCB Top view.

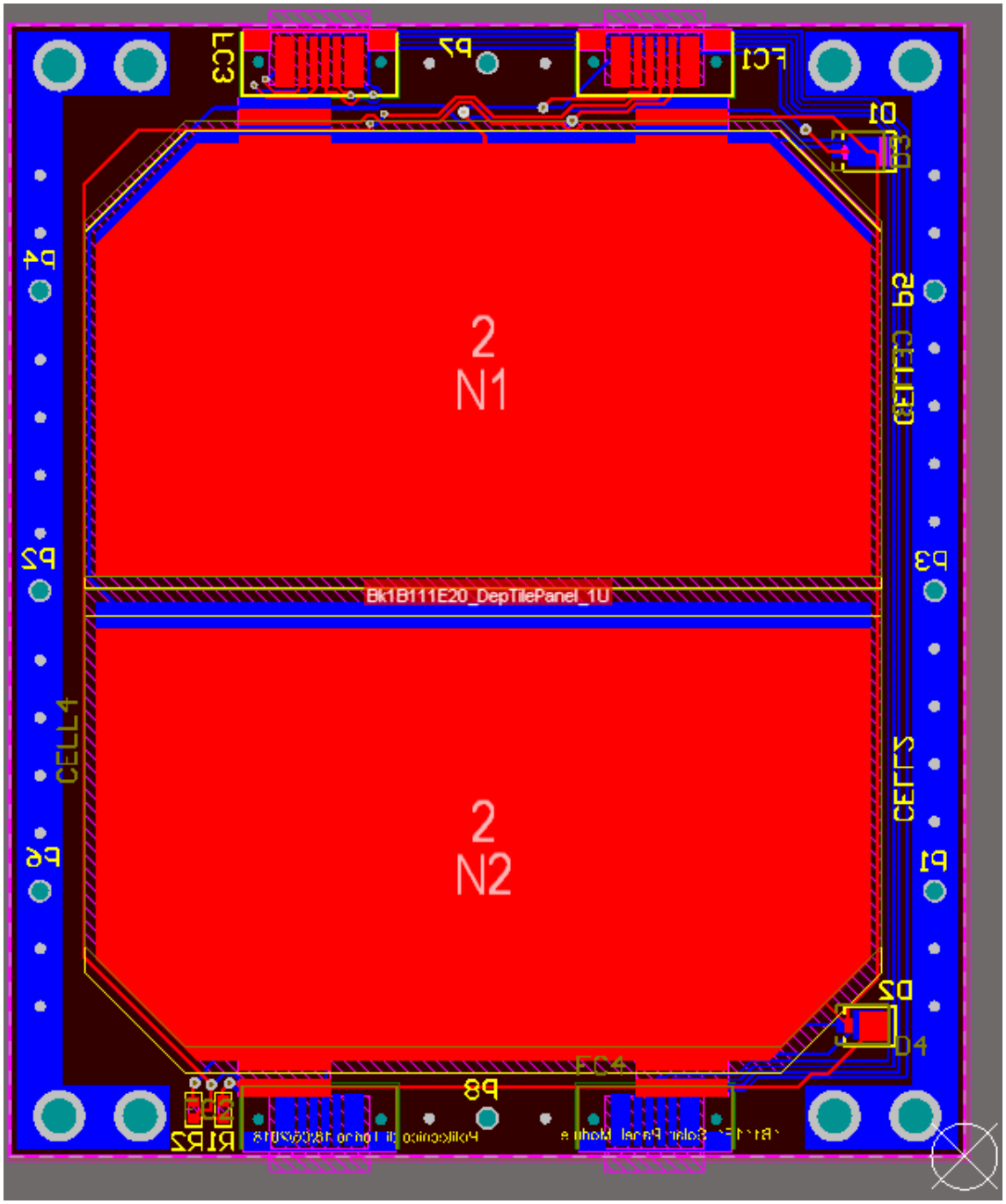


Figure 41. Bk1B111E20 PCB Bottom view.

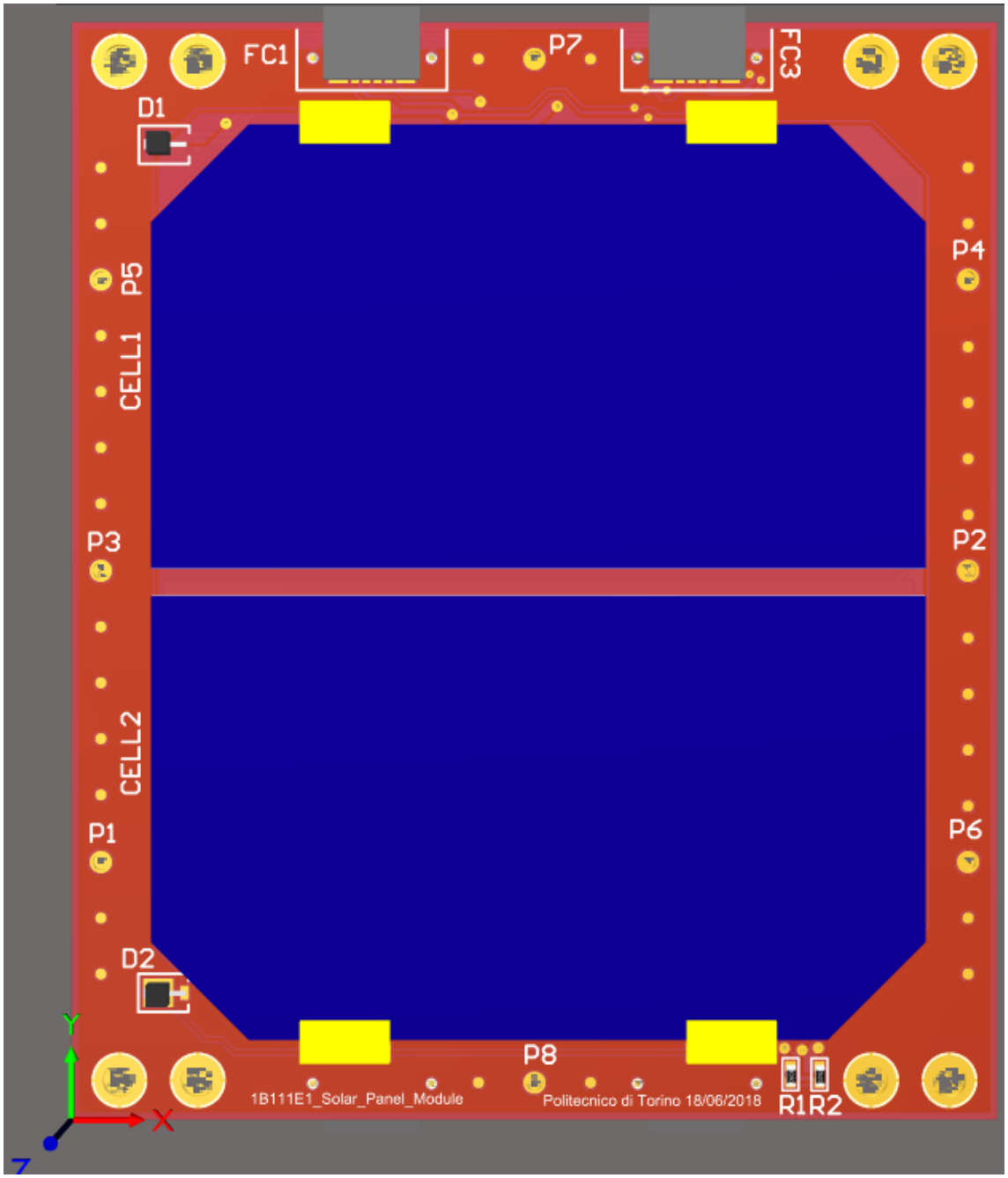


Figure 42. Bk1B111E20 3D Top view.

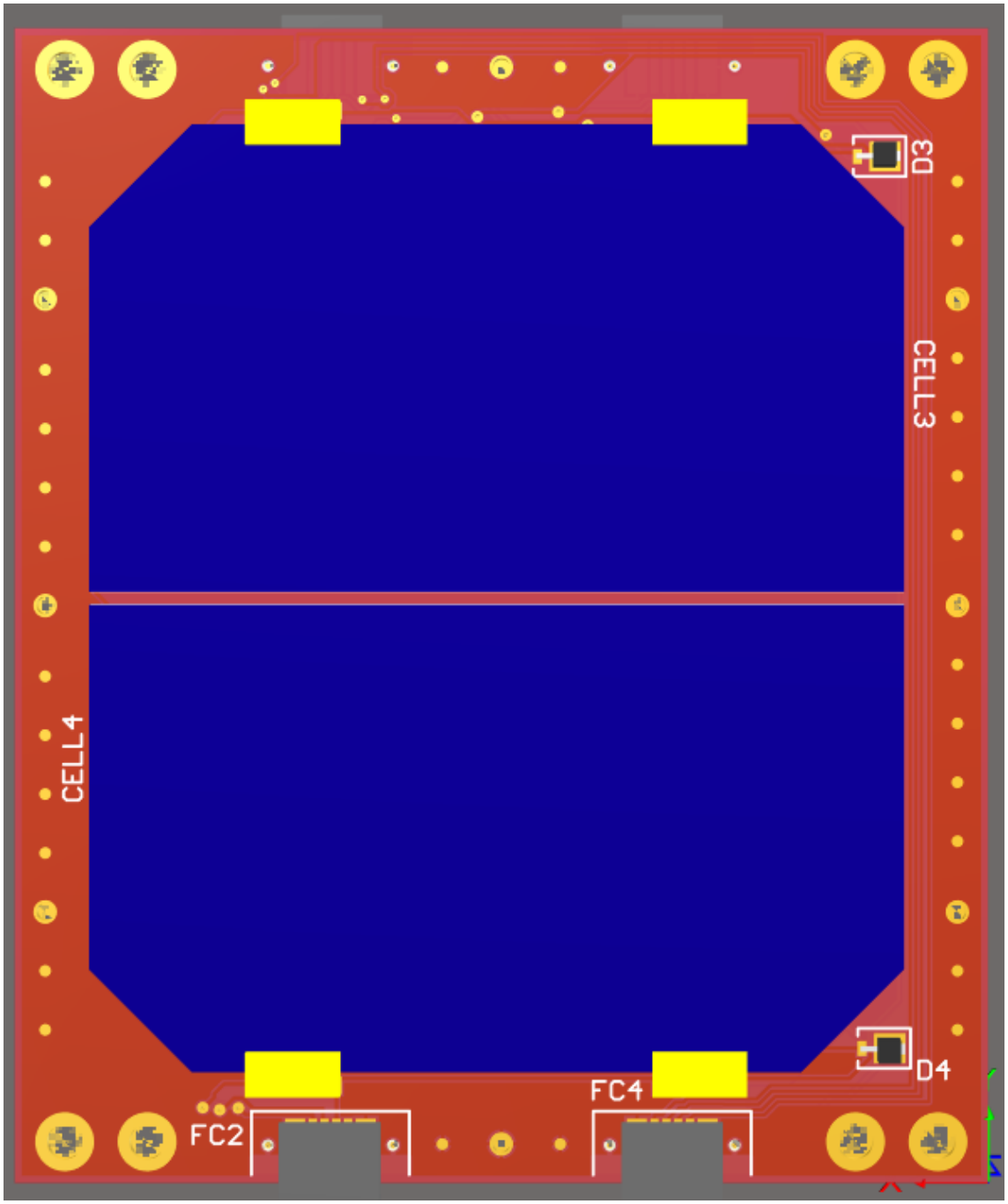


Figure 43. Bk1B111E20 3D Bottom view.

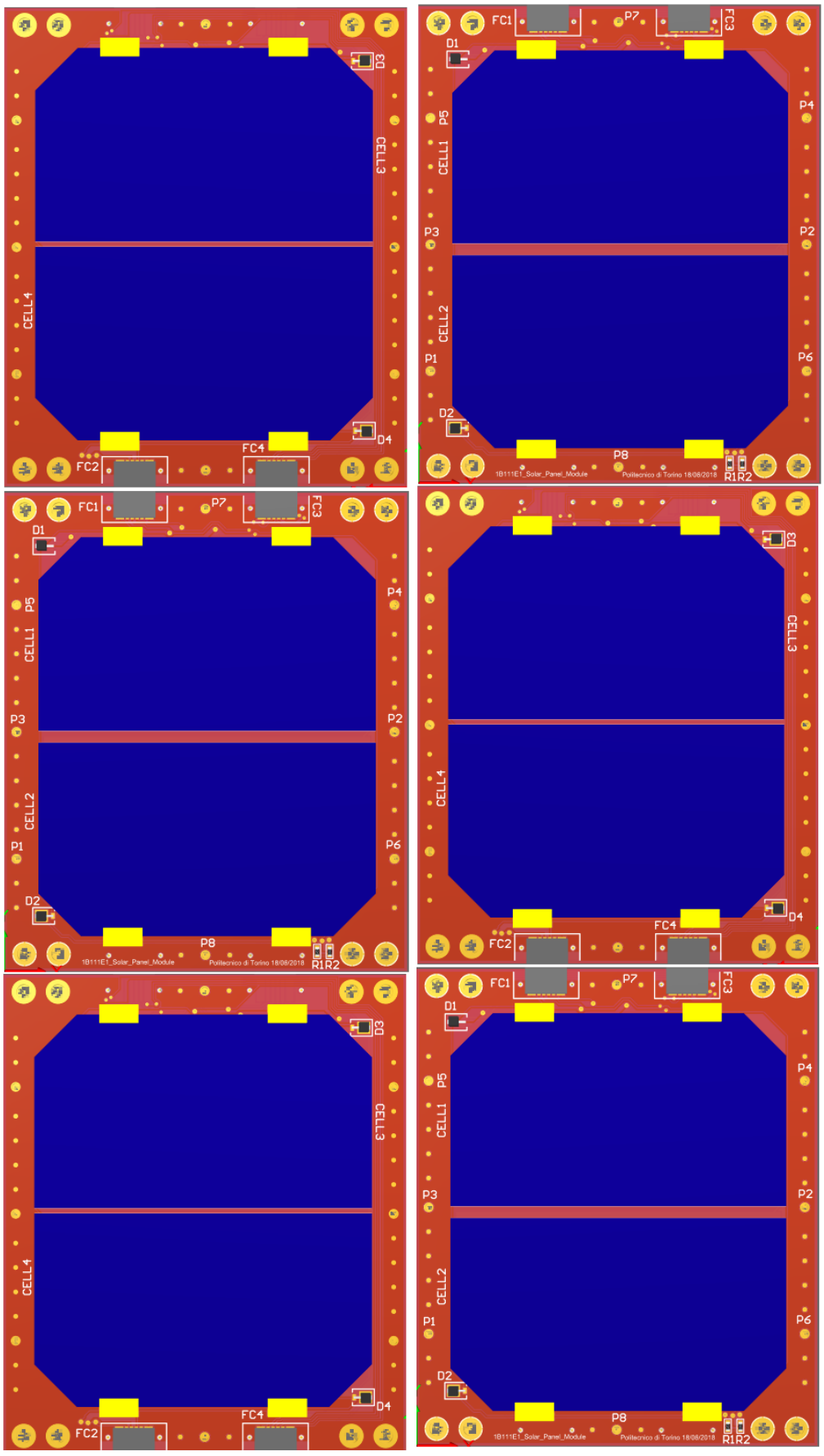


Figure 44. Final connection of deployed system.

4.2.3. Bk1B111E10_BoardLatSuppBar and Bk1B111E11_BoardCenterSuppBar.

Another two boards have been created to be assembled into *Bk1B111E20_DepTilePanel_1U*, *Bk1B111E10_BoardLatSuppBar* and *Bk1B111E11_BoardCenterSuppBar*. These board fulfil the function of to provide rigidity where the pads of the fuser have been positioned. Besides, it prevents the components do not be touch by each other.

***Bk1B111E10_BoardLatSuppBar*.**

This board are assembled in the lateral of the board, and have three PADs.

Its schematic are very similar to the schematic PADs connection of *Bk1B111E20_DepTilePanel*.

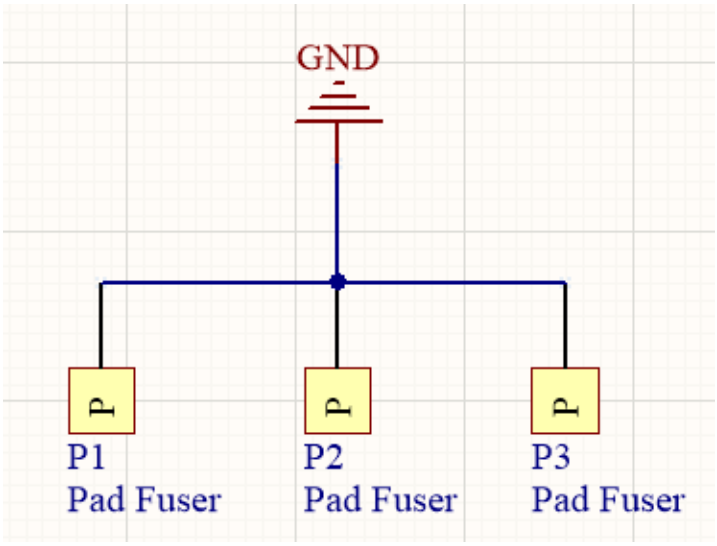


Figure 45. Bk1B111E10_BoardLatSuppBar schematic.

Therefore the PCB design is similar to the side where the board have to be assembled.

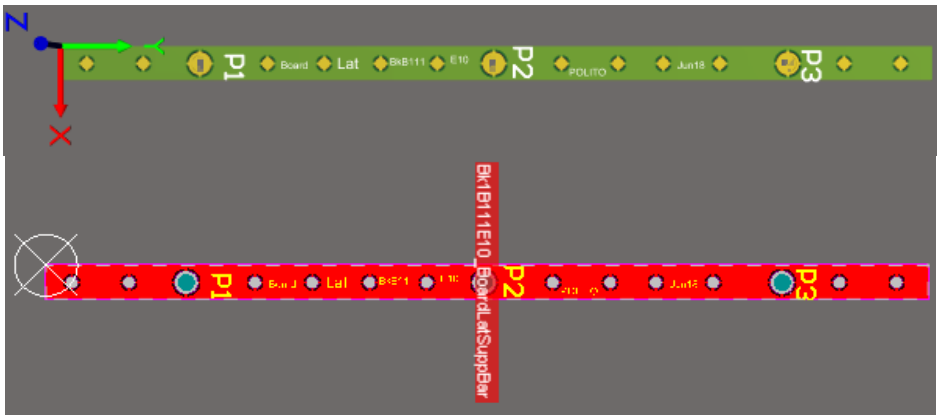


Figure 46. 3D and PCB model of Bk1B111E10_BoardLatSuppBar.

Keeping in mind the origin of the board, the position of each *PAD Fuser* is:

PAD	X (mm)	Y (mm)

P1	1.532	12.247
P2	1.532	38.247
P3	1.532	64.265

Table 17. Bk1B111E10_BoardLatSuppBar PAD position.

Bk1B111E11_BoardCenterSuppBar.

This board are assembled in the center of the board, and have one PAD. As *Bk1B111E10_BoardLatSuppBar* its schematic is very simple and similar to schematic PADs connection of *Bk1B111E20_DepTilePanel*.

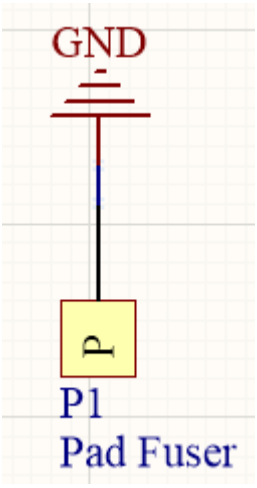


Figure 47. Bk1B111E11_BoardCenterSuppBar schematic.

Finally its 3D and PCB model are as shown in figure X.

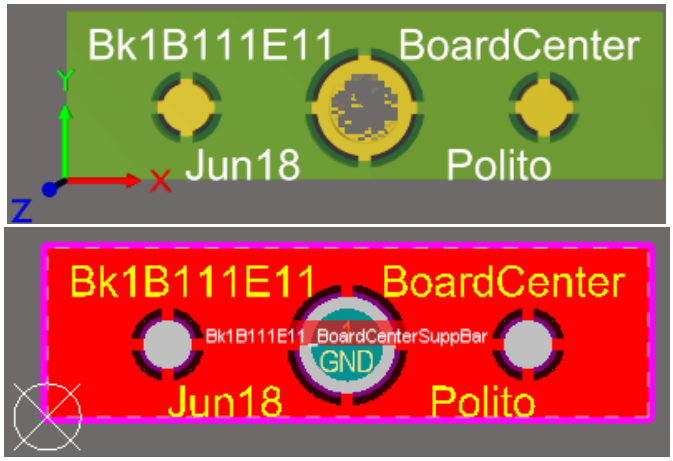


Figure 48. 3D and PCB model of Bk1B111E11_BoardCenterSuppBar.

The PAD position is:

PAD	X (mm)	Y (mm)
P1	6.235	1.491

Chapter 5.

5. Test of the printed circuit board.

In this chapter Bk1B111E board has been assembled and tested. It has been made 10 boards of *Bk1B111E20_DepTilePanel_1U*, and 40 of *Bk1B111E11_BoardCenterSuppBar* and of *Bk1B111E10_BoardLatSuppBar*, since in each *Bk1B111E20* there are four pieces of *Bk1B111E11* and *Bk1B111E10* assembled.

For the assembly of the board a procedure has been followed, the process has consisted in the connection of elements of the board and its soldering. Several machines have been used which will be describe below.

Once the board were assembled it has been checking the strength of the structure and if solar cells were damaged. The board has been tested three times with different process, and therefore with different results that have been described in this chapter.

5.1. Machines used in the procedure.

In order to complete the process several instruments have been needed, the instruments belong the laboratory where the assemblage has been done. At this point, to understand the process, the main features of this instrument have been explain.

5.1.1. Essemtec (pick and place machine).

The components are deposited in each necessary boxes, with an X/Y guiding system and easy-gliding head is more accurate and efficient than placing components by hand. The easy-glide head rotates up to 360°.

With the control located right on the head, adjusting component polarity and alignment to pad is effortless. Once the component is lowered to the PCB, the vacuum shuts off automatically, releasing the part. Vacuum pressure is fully adjustable. Placement nozzles are quick and easy to change out.

The pick and place machine also have a support which help to keep fixed the board, and its connected to a computer screen where show the images of a cam which record enlarged images of the component.[10]

Figure 49. Pick and place machine.

5.1.2. Soldering instruments.

Clever – Dispense 04.

This instrument is a table top dispenser for precise delivery of dots and lines with media from high until medium viscosity. An intelligent, patented technology takes account of all necessary factors and computes the pressure pulse required for a precisely defined volume to be dispensed with the highest accuracy and repeatability. All of this while surprisingly easy to use.

In *Bk1B111E20*, the paste has been delivery only one side, on the solar cells positions in the diodes and the points of soldering where *Bk1B111E10_BoardLatSuppBar* and *Bk1B111E11_BoardCenterSuppBar* are placed.[11]

It also contains features as temperature compensation and fill level compensation.

Dispense volume	0.001 - 9.99 mm^3
Medium delivery pressure	0.2- bar -5 bar
Temperature com	20°C - 50°C

Figure 50. Clever – Dispense 04.

Mantis Elite.

Mantis Elite is a microscope used for inspection of the board, this instrument has been used to help the distribution of the welding points.

Figure 51. Mantis Elite.

PVR300 Regulated DC power supply.

This regulator has been used to provide power supply to Mantis Elite.

Figure 52. PVR300 Regulated DC power supply.

5.1.3. JBC-JTE2D.

This machine has been used as a pick and place, useful to place medium boards as *Bk1B111E10_BoardLatSuppBar*.

Beside it has been used as a precision hot air station for welding a small piece (*Bk1B111E11_BoardCenterSuppBar*) quickly and safely.

Figure 53. JBC-JTE2D.

5.1.4. Infrared IC heater.

Is a microprocessor controlled reflow-oven. It can be used for effectively soldering various SMD components. The whole soldering process can be completed automatically. This machine uses a powerful infrared emission and circulation of the hot air flow, so the temperature is being kept very accurate and evenly distributed.

This machine use several waves of heat which have different temperatures and different air flow. For the assemblage process has been used two different waves.[12]

Figure 54. Infrared IC heater.

5.2. Assembly procedure of the board.

For the mounting of the board has been following several steps. The step are similar for the three different process of the building board, the unique change has been the solder past or the curve temperature of the Infrared IC heater, these changes will be explained in detail in the next point.

First of all the components have been chose keeping a method, searching in a database of the laboratory the component, thus the component is taken in its location.

Once in the laboratory, the component is picked and transported and taken to the pick and place machine where it will remain until its placement once the solder paste has been distributed.

In order to distribute the solder paste the Clever – Dispense 04 machine has been used. Just one side of the board has been welding on the three assemblage, which is due to the difficult of the soldering on the other side. Therefore on one side have been welding the two diodes, two boards *Bk1B111E10_BoardLatSuppBar* and two *Bk1B111E11_BoardCenterSuppBar*.

Then, the board, with the solder paste distributed, is fastened on the pick and place machine to place the components. The head produce vacuum in the component and with the help of a computer screen that enlarge the image is moved to its correct place in the board. This machine were used to place the SMD component, the diodes.

Figure 55. Component placed in the pick and place machine.

To place two solar cells and *Bk1B111E10_BoardLatSuppBar* the JBC-JTE2D has been used, its work is similar to the pick and place machine. Although to place two boards *Bk1B111E11_BoardCenterSuppBar*, due to its small size a pin has been used, the placement of this board has been very difficult.

To finalize the process, the board, with all the components on its position has been introduce into Infrared IC heater, thus the solder past is weld on the board. In each test a different heat wave has been used, in such wise different results have been obtained. Three waves have been used for the process, wave 3 for the first, wave 6 for the second and wave 2 for the last test.

For the last test, solar cell were placed with a special glue after were introduced into the Infrared IC heater, the reasons are explained in point 5.3.3.

5.3. Testing and conclusions.

Three boards *Bk1B111E20* have been assemblage in different ways. The main differences are the solder paste, the heat wave and the placed of the solar cells. In this point these difference and its conclusions will be developed.

5.3.1. Test one.

In the first test two diodes, two *Bk1B111E10_BoardLatSuppBar*, two *Bk1B111E11_BoardCenterSuppBar* and two solar cells have been placed on the top side of the board *Bk1B111E20.*

The solder paste used has been SMD291SNL10T5, which its thermal conductivity is 59W/(m·K) and its melting point is 217-220°C. For the Infrared IC heater has been programed the wave 3, the recommend profile for this solder paste. The reflow oven reach until 250°C and its duration is seven minutes.

In this test *Bk1B111E10, Bk1B111E11* and the solar cells were placed manually, for this reason them were not placed correctly.

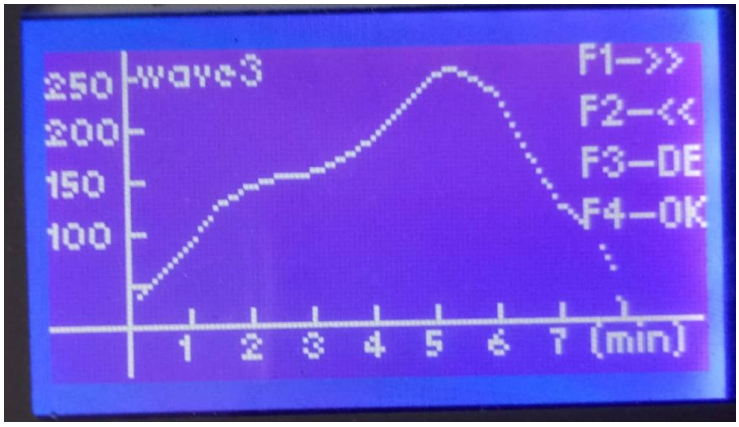


Figure 56. Temperature profile for test 1.

Conclusion.

The conclusion for the first test are the next:

- Due to the high temperature of the reflow oven thermal expansion has been produced. That is due to the different coefficient of the surface of the board and the surface of the solar cell. The result is the curvature of the board, whose vale was 0.9mm.
- Due to the small size of *Bk1B111E10_BoardLatSuppBar* and *Bk1B111E11_BoardCenterSuppBar* it cannot be soldering well. Although *Bk1B111E10* has been soldered, however piece moves from its places and the whole size of the hole is reduced. Otherwise *Bk1B111E11* could not remain welded.
- Besides due to the heat the solar cell has been damage.

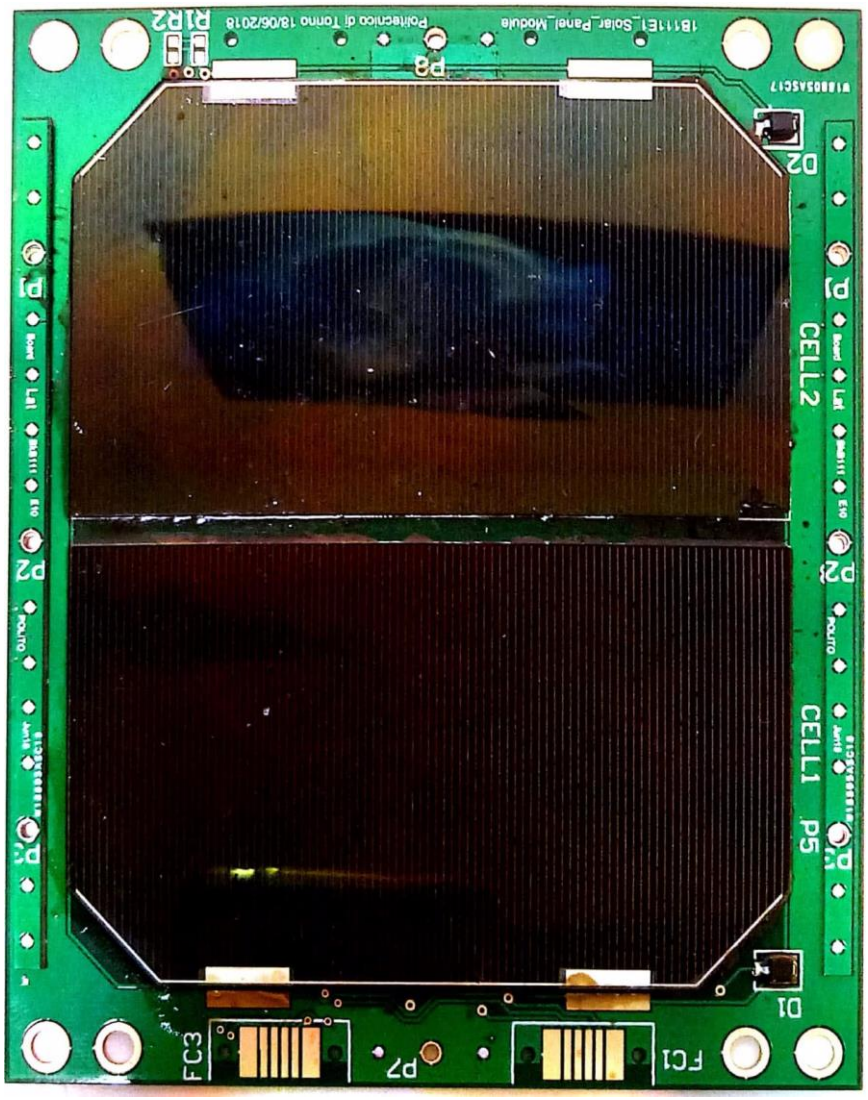


Figure 57. Result first test for Bk1B111E20.

5.3.2. Test two.

In this test, as in the last test, two diodes, two *Bk1B111E10_BoardLatSuppBar*, two *Bk1B111E11_BoardCenterSuppBar* and two solar cells have been placed on the top side of the board *Bk1B111E20.*

Due to the results of the first test (point 5.3.1), it has been decided that the solder paste used were changed for SMDTLFP10T4, whose melting point is 138°C. The wave for Infrared IC heater has been also changed, since the solder paste is different and therefore it melting point, it has been chose wave 6, which higher point is 250°C.

This time the medium component, *Bk1B111E10* and the solar cells, have been placed with JBC-JTE2D (pick and place machine), in order to reduce the errors. Besides *Bk1B111E11* was placed with a pins.

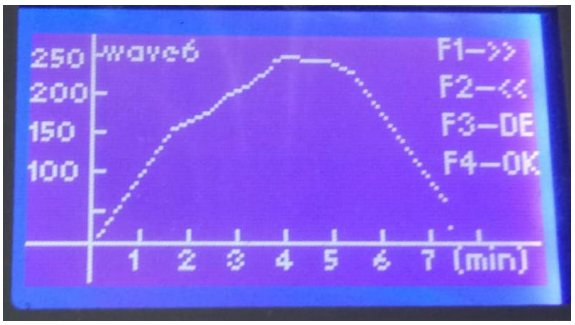


Figure 58. Temperature profile for test 2.

Conclusion.

This test has resulted worse than the first test:

- Due to the high temperature of the reflow oven thermal expansion has been produced. That is due to the different coefficient of the surface of the board and the surface of the solar cell. The result is the curvature of the board, whose value has been increased until 1.1mm.
- Due to the small size of *Bk1B111E10_BoardLatSuppBar* and *Bk1B111E11_BoardCenterSuppBar* it cannot be soldering well. Although *Bk1B111E10* has been soldered, however piece moves from its places and the whole size of the hole is reduced.
- Otherwise *Bk1B111E11* could not remain welded.
- Besides due to the heat the solar cell has been damage.

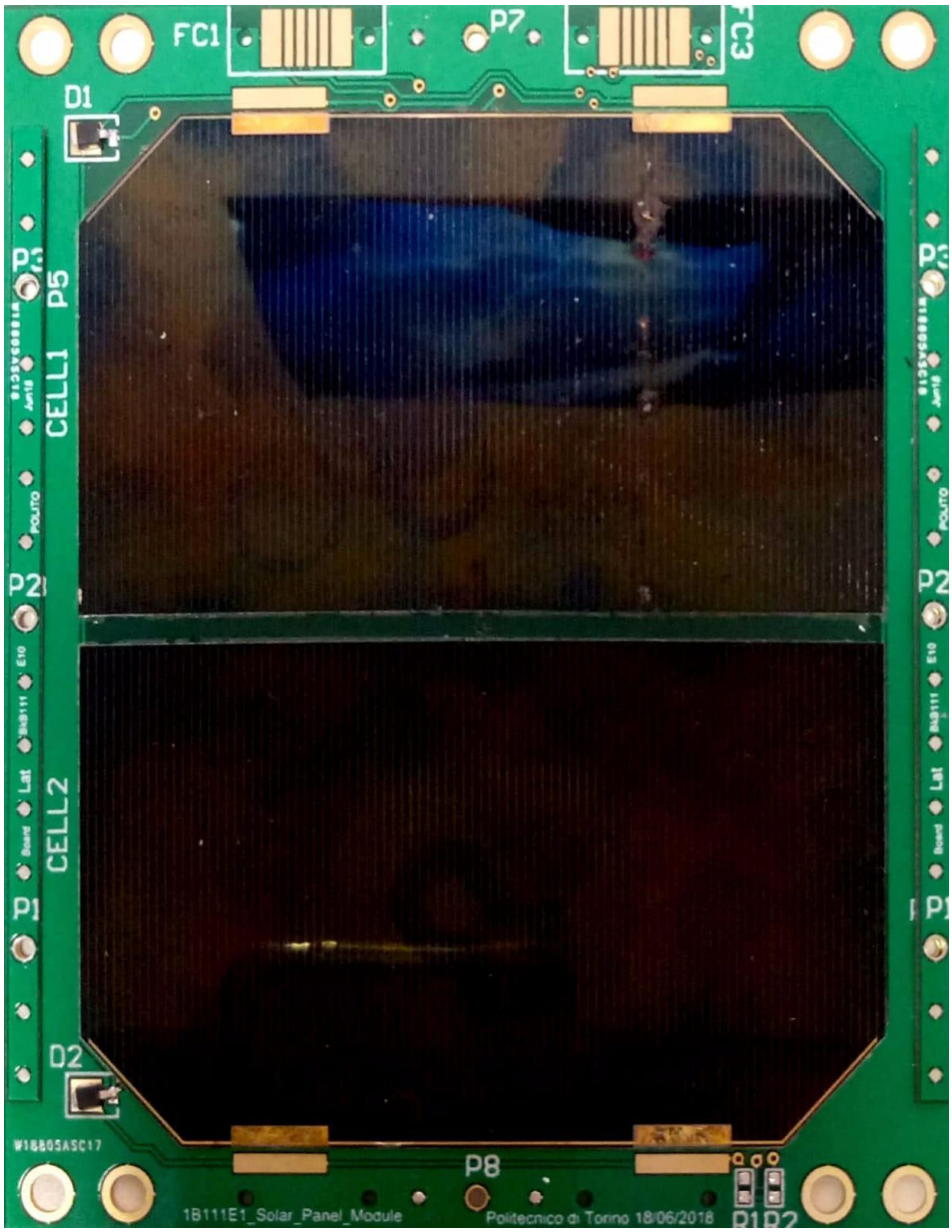


Figure 59. Result second test for Bk1B111E20.

5.3.3. Test three.

For the third test, it has been decided to weld just the two diodes and two boards two *Bk1B111E10_BoardLatSuppBar* and two *Bk1B111E11_BoardCenterSuppBar* have been placed on the top side of the board *Bk1B111E20.* Once these components were soldered, one solar cell has been placed with a special glue, thus it has been avoid the thermal expansion produced in the solar cells.

First of all *Bk1B111E10* and *Bk1B111E11* have been placed. The way to position *Bk1B111E10* has been the same as the other two test, namely using the instrument JBC-JTE2D and introduced in Infrared IC heater. The solder paste has been the same (SMDTLFP10T4) however this time the wave has been changed. It has been programed wave 2, which has been the lowest temperature of the three tests.

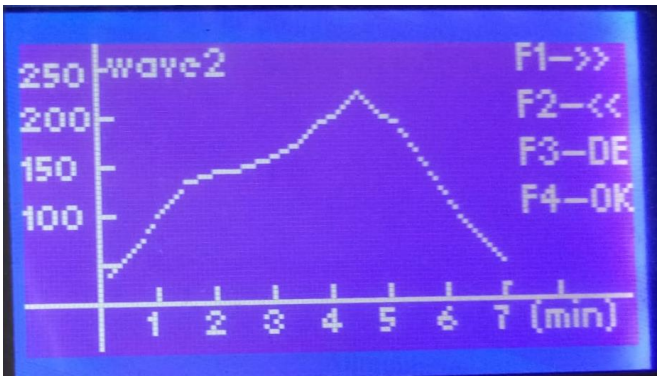


Figure 60. Temperature profile for test 3.

Once *Bk1B111E10* has been positioned, it has been placed *Bk1B111E11* boards. For this test the method of placed has been changed and has been done manually with JBC-JTE2D, with a temperature of 200°C and air to 70%.

The special glue is CV2-2646, a silicone glue electrically conductive. To apply it have to be measure with precision, these means that it has been necessary to calculate the volume of the glue. Beside SP-120 has been added, since improve the characteristic of the glue. Therefore a mix has been prepared.

First the volume of CV2-2646 has been calculated:

Knowing the area of the solar cell 67x37mm and a thickness approximate of 0.3mm the volume is:

$$Vol = 67 \cdot 37 \cdot 0.3 = 743.7mm^3$$

Figure 61. Volume of CV2-2646.

It has been decided to take a volume of 800 mm^3.

Knowing the Specific Gravity has been calculated the weight of CV2-2646 has been proceeded by this way:

Specific Gravity = 3.23 $\frac{N}{mm^3}$

$$\frac{3.23 \cdot 800}{1000} = 2.584g$$

It has been mixed 100 parts base to 0.5 part curing agent by weight, just prior to use.

$$\frac{0.5 \cdot 2.58}{100} = 0.01292g$$

The volume for $0.01292g$ will be $13mm^3$.

Therefore a mix of $800mm^3$ of CV2-2646 and $3mm^3$ of SP-120 has been made

Once the mix has been made, the surface of the board where the solar cell will be placed has been cleaned and degreased the surface being primed with an appropriate solvent and a coarse lint-free cloth. It has been used acetone.

Figure 63. Acetone.

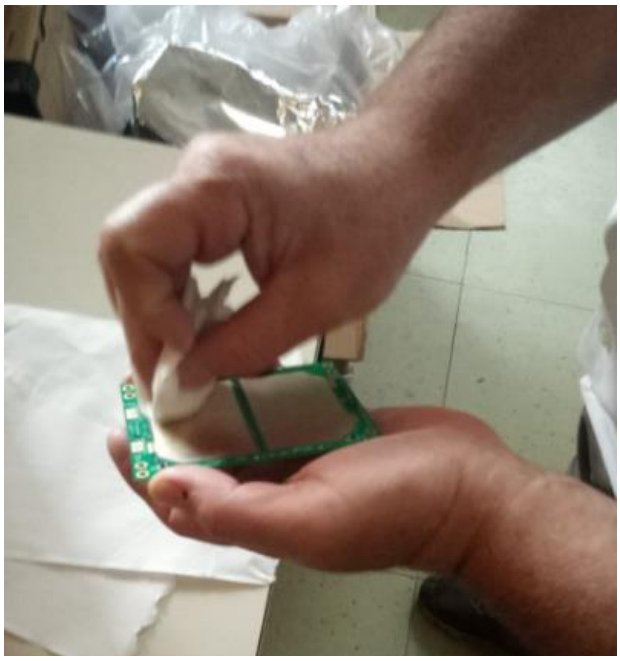


Figure 62. Clean and degrease the surface.

And finally the mix has been apply through the surface of the solar cell (CELL1) and it has been allowed to dry for 2 hours.

Conclusion.

- This has been the test with the best results, since the properties of the solar cell has not been damaged.
- The *Bk1B111E11* has remained in its position.
- No dilation has occurred.

Despite this, it has not made a conductivity test.

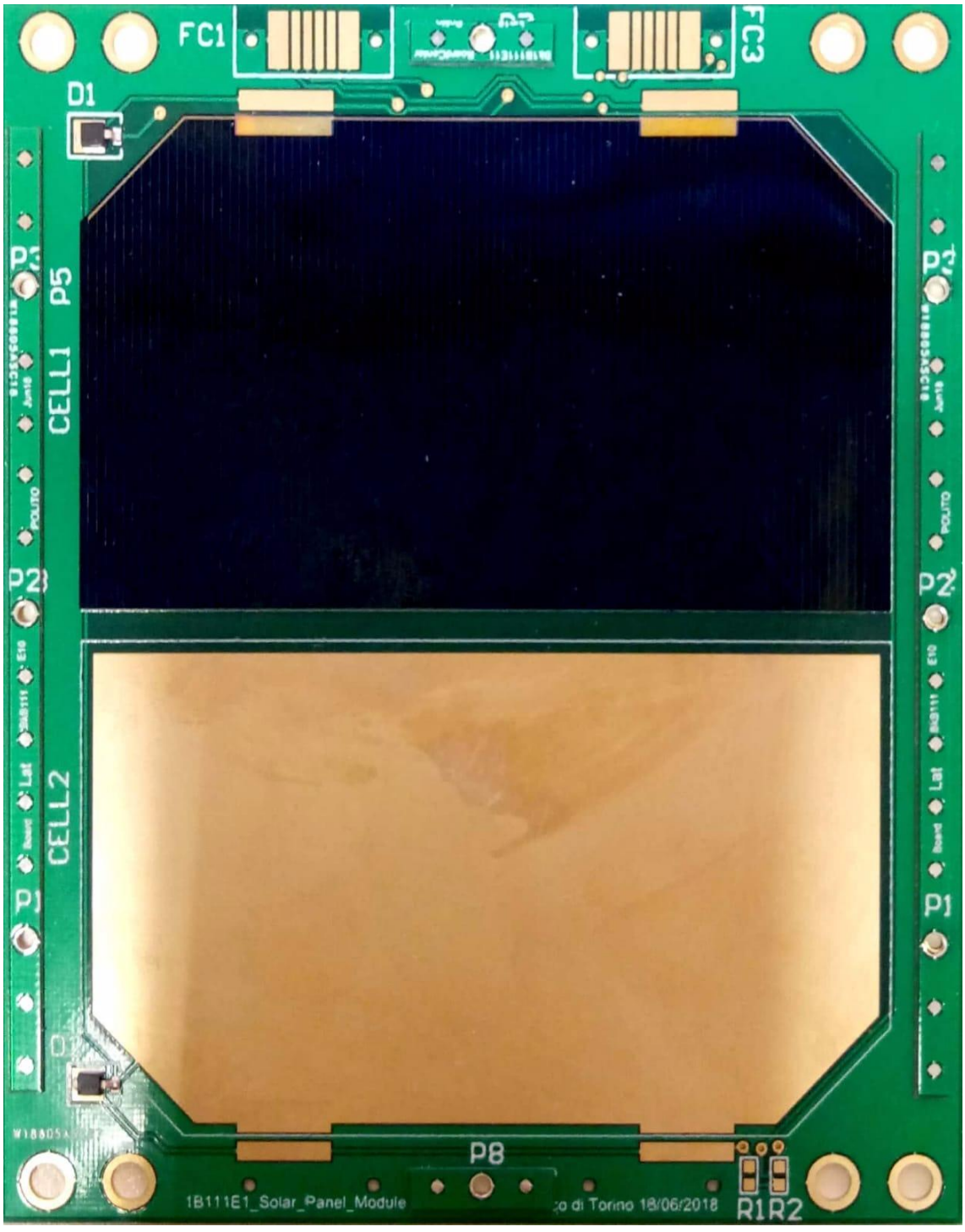


Figure 64. Result third test for Bk1B111E20.

6. Bibliography.

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