

Onboard communication systems for low cost small Satellites

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Problem Statement

Nowadays the biggest challenge to space industry is to design space systems

- Cheaper-Lower the mission cost
- **•** Faster-Lower the design and implementation time
- Better- Keep a high quality standard and achieve most mission targets
- How to achieve this Cheaper-Faster-Better philosophy?
 - Scale down the satellites
 - □ Simplify their design
 - Reduce Power and data har
 - □ Simplify their testing



Undesirable

Desirable



Outline

- □ AraMiS Project
- \Box Concept of tiles
- □ Smart Harness
 - Embedded and smart harness
 - In Module Life cycle
 - Spacecraft configurations
 - Test board for functional testing
- □ Inter-tile Communication
 - Description Module design: Wired inter-tile communication
 - Description Module design: Optical Based communication
 - Description Module design: Radio Frequency Based communication
- □ Conclusion

ARAMIS Project

- ARAMIS (Modular Architecture for Satellites) is an innovative modular architecture for flexible and more demanding satellite configurations.
- Panel bodies or tiles
 - Different size and technology
 - Power and data standardized interfaces
- Modularity
 - Mechanical, electronic and testing level
- Low cost
 - Design, qualification and test cost shared among multiple modules
- □ Mostly LEO Satellites (600 800 km)
- The size of the satellite varies based on payload demands

Hardware Architecture of Tile (1)

Single-size AI: 16.5x16.5 cm² tile, a 1.6mm thick monolithic Aluminum structure, for cheaper and smaller configurations







Hardware Architecture of Tile (2)

 CubeSat standard: (8.25 x 9.8cm²) tile, with all electronic components integrated and compatible with CubeSat dimensions.
 All structure on PCB only

□All the subsystems integrated on each tile









Hardware Architecture of Tile (3)

□<u>Honeycomb Structure</u>: 16.5x33 cm² tile, with 10mm thick honeycomb structure for more rigid and larger structures



Smart harness

Plug and Play Modules

Spacecraft configurations Physical Module based configuration: Honeycomb tile Functional Test board



Embedded harness

- Distributes electrical power and data signals all around the spacecraft and payloads by
 Minimizing power and data harness complexity
 Reduction in harness mass by distributing power and data signals embedded in the printed circuit board
 - Embedded signals interfaced to other panels by
 Multiple board to board connectors
 Processing done by the central processor
 Some space systems already employ this scheme.
 [1]



Smart Harness

□Minimize Power, data, RF harness with additional signal processing capabilities. **Tiles**: provide power, data standardize interfaces Tile Processors: on every tile Signal processing capabilities at tile level Every subsystem is housed in small daughter boards pluggable on tiles Internal subsystems interfaced with tile processors using slots External subsystems interfaced with tile processors

using pluggable connectors

Smart Harness: Block Diagram





Smart Harness: Subsystem Modules



Smart Harness: Extended Modules



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Smart Harness: Module Slot Serial Data

RS232 signals on Odd Modules only (i.e. modules A, C, E, G)
 I²C signals shared in pairs i.e.

- □ connectors A, B share same I²C channel
- □ SPI signals on Even Module (module B, D, F, H)
- Odd numbered module can be configured for SPI if not configured for RS232 mode

	A	В	С	D	SPI (O)	SPI (E)	² C	RS232 (O)
D0/RX/SOMI	SOMI / RX	TA1.2	SOMI / RX	TA0.1	\checkmark			\checkmark
DI/TX/SIMO	SIMO / TX	TA0.0	SIMO / TX	TA0.2	\checkmark			\checkmark
D2/SCL/SOMI	SCL	SCL / SOMI	SCL	SCL SOM		\checkmark	\checkmark	
D3/SDA/SIMO	SDA	SDA / SIMO	SDA			\checkmark	\checkmark	
D4/CLK	CLK	CLK	CLK	CLK	\checkmark	\checkmark		
D5/PWM	TB0.0	TBQ.	TB0.2	TB0.3				
D6/A0	A0	A2	A4	A6				
D7/AI	AI	A3	A5	TBOCLK/ SMCLK				
D8/ID	TA0CLK/ACLK	TA0.I	TA0.3	SMCLK				
D9/EN	D9	TA1.2	D9 /17/2019 PhD	Presentation				15



Smart Harness: Module Life Cycle

- UML to define, specify, design, implement, test and document a complete subsystem.
- Define intended functions: Use case diagrams
- Define electrical and functional requirements: Requirement diagrams
- □ Electrical/software/Mechanical design: Class diagrams
 - Code details: Software (SW) class
 - Schematics : Hardware (HW) class
 - Mechanical details: Mechanical class
 - Component selection: Component class
- □ Testing design: Sequence diagram
- Manufacturing: Commercial CAD tools
- □ Real Testing
- Redesign
- Production
- Integration

Smart Harness: Module Life Cycle



Smart harness

Plug and Play Modules Spacecraft configurations

Physical Module based configuration: Honeycomb tile Functional Test board

Smart Harness: Spacecraft Configurations

Design the new subsystems either on single, double or quadruple module configuration.

Test the subsystems on ground using development board.

Integrate each physical module in a physical module based satellite configuration.

- Embed the logical modules in the main tile for a Satellite on demand configuration.
- The Satellite on demand configuration can be altered very easily for Reusable design configuration



Physical Module Based Configuration

- Develop standard tiles hosting multiple connectors
- Physical daughter boards connected to the tile via pluggable connectors
- □ The subsystem module only plugged if mission needs it.
- High level of design flexibility, testability and upgradability
- Testing of modules, tiles and whole satellite is needed
- For teaching/research purposes





Satellite on demand Configuration

□ Already tested modules integrated inside the PCB.

Reusability of physical subsystem modules

Permanent configuration

□ Testing of modules: not required

□ Testing of tiles and mission is required only

CubeSat standard tile built

using this approach





Reusable design configuration

- Optimised spacecraft configuration based on customer requirements
- Reuse of the satellite on demand configuration
- Minor addition or removal of subsystems on customer demands
- □ Follows the Cheaper-Faster-Better philosophy
- □ Module and tile testing: not required
- □ Only mission testing is needed for this configuration

Smart Harness: Design trade off



Smart harness

Plug and Play Modules Spacecraft configurations Physical Module based configuration: Honeycomb tile Functional Test board



Honeycomb Tile

- Sandwich structure for lighter and more rigid spacecraft configurations.
- Honeycomb core: integrated between two lateral FR4 PCB skins
- Solar cells: 14 solar cells in series achieving 30.8V, 0.4A current and 12.32W output power.
- □ Tile processors: two MSP430F5438
- Module interface: Tile processor signals interfaced to slots and connectors
- Primary switching: MPPT Buck converter to achieve power distribution bus (PDB) level.
 - **Regulators:** 5V, 3.3V, 3.0V
 - Sensors: Temperature (-30 to+70), voltage, current and sun sensors
 25

Honeycomb Tile

Visual Paradigm for UML Standard Edition(Politecnico di Torino, Dip. Elettronica) Solar Panel Honeycomb Sun S	External skin
	Honeycomb core
70C Temperature Sensor Calibration Memory 1B1121C_Primary_Switching_Buck_V2	Internal skin
20V Voltage Sensor 2.5A Current Sensor 400mA Low Side Current	ensor Tile Processor 8M V1 Quadruple Module Interface Receptacle
3V3 1A6 Mixed Regulator	
5V 5A Switching Regulator	
3V0 Reference	Quadruple Module Interface Receptacle Tile Processor 8M V1 Quadruple Module Interface Receptacle

Honeycomb Tile-Solar In



Honeycomb Tile-PDB (14-16V)



Honeycomb Tile-3.3V



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Honeycomb Tile-5V



Honeycomb Tile-Physical view



Smart harness

Plug and Play Modules Spacecraft configurations Physical Module based configuration: Honeycomb tile Functional Test board

Smart Harness: Functional Test Board



Inter-tile Communication

Module design: OBDB interface

Module design: Optical based Module design: Radio frequency based



Module Design: OBDB interface





Inter-tile Communication

Module Design: OBDB interface

Module Design: Optical (Free space and Glass based)

Module Design: Radio Frequency



Module Design: Optical

□No harness mass

To save cost and simplify integration

□Low datarate (~ IMbps)

Mainly for housekeeping and low-end payloads

□ Insensitive to VHF or S-band noise

□ Should not be disturbed by on-board transceivers

□ Short communication distance

□ Maximum 2 ÷ 3 m

Low power consumption

Limited power budget



+

Commercial Devices

Integrated Transceiver Modules Integrated Transceiver Controllers





Low Power Consumption, Fast development time, Low Cost, Small Size

Lack of Flexibility, Radiation testing complexity

Our Solution - IrDARAMIS

Develop an electronic front-end

- + Flexibility in data rate and modulation
- + Flexibility in component selection
- Longer development time
- Use a microcontroller to implement protocol stack
 - + Easy to implement and modify
 - + User selectable encoding scheme

Inter Tile Communication: Optical Based



Optical Based: Transceiver Design



□ First Stage TIA: $H_1(s) = -\frac{V_{out1}}{I_{in}} = -\frac{R_{f1}}{1+R_{f1}C_1s}$ □ Second Stage Voltage Amplification $H_2(s) = -\frac{V_0}{V_0}$ $-\frac{1}{1+R_{f2}C_2s} * \frac{R_{f2}C_{z1}s}{1+R_{z1}C_{z1}s}$ □ DynamicThreshold Comparator $\frac{R_{01}}{R_{T1}} \le \frac{V_{CC}}{V_{off}} - 1$



Transciever design:Frequency Response

□ First Stage response

□ Second Stage Response

Band Pass Filter





Transciever design: Transient Analysis





Transciever Design: Range testing

Received current as a function of distance and input radiated optical power
 Can easily handle wide dynamic range



Bus Configuration - IrDARAMIS

- Line-of-Sight communication
 - Add small mirr the corner of each module
 - Different configuration of transmitters and receivers in the cube



Received current at different Tile s locations



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Otical: Glass Fiber Communication



Optical Module: Glass Fiber Based



Optical Module: Testing Results



Inter-tile Communication

Module Design: OBDB interface Module Design: Optical(Free space and glass based)

Module Design: Radio Frequency based



Module Design: Radio Frequency Based

- Radio Frequency Modules: For inter tile communication.
- □Software: IB45 subsystem serial data bus+ additional software needed
- Hardware: Based on TI CC2510/CC1110 transceivers.
 - Not yet fabricated on modules.
 - Therefore we use evaluation modules for testing purposes.
- We therefore concentrated on the software side
- SimpliciTl protocol was used in the design

Inter Tile Communication: Wireless SimpliciTI

- A proprietary low-power radio frequency (RF) protocol by Texas Instruments (TI).
- It targets simple and small RF networks (less than 100 nodes).
- SimpliciTI network protocol was designed for easy implementation with minimal microcontroller resource requirements.
- Flexible: Direct device to device communication
 Utilizes a five command API.



SimpliciTI Protocol:Transceiver

- The CC2510/CC1110 Systemon-Chip (SoC) transceiver used for SimpliciTI applications.
- It comes with 32/64/128 KB of flash memory and 8051 MCU core.
- Range: 5-500 Meters, depending on the RF environment and the power output consumption required for a given application.
- The SmartRF04EB used as main platform in the development kit.









- Layers
 - MRFI ("minimal RF interface")
 - NWK
 - nwk applications (modules)
 - customer applications

- Network Support
 - init
 - ping
 - link / linklisten
 - nwk mgmt
 - send / receive
 - I/O



SimpliciTI:API

- initialization
 - smplStatus_t SMPL_Init(uint8_t (*callback)(linkID_t));
- linking (bi-directional by default)
 - smplStatus_t SMPL_Link(linkID_t *linkID);
 - smplStatus_t SMPL_LinkListen(linkID_t *linkID);
- peer-to-peer messaging
 - smplStatus_t SMPL_Send(lid, *msg, len);
 - smplStatus_t SMPL_Receive(lid, *msg, *len);

configuration

smplStatus_t SMPL_loctl(object, action, *val);

SimpliciTI: Class diagram





SimpliciTI: Measured RSSI

Results for equivalent length of CubeSat in open air conditions





Packet Sniffer

The packet sniffer
 visualizes all RF
 traffic and content
 a graphical format.

Each packet receive
 a time stamp and R
 protocol flow can b
 inspected in
 chronological order

`	🚸 Texas Instruments SmartRF Packet Sniffer SimpliciTI v1.1.0									
	File Settings Help									
	🗅 🗅		► II	i 🕲 📮 🖏	SimpliciTi v1.1.0 💌					
_ :	P.nbr.	Time (ms) 10	Length	Dest. Address	Source Address	Applicaton payload AroMi	User Port	RSSI (dBm)	LQI	FCS
τΙ	1	=0	21	87 56 34 12	54 76 03 05	S!!!*	0x20	-22	24	0K
_	P.nbr.	Time (ms) +3	Length	Dest. Address	Source Address	Applicaton payload AraMi	User Port	RSSI (dBm)	LQI	FCS
	2	=3	21	87 56 34 12	54 76 03 05	S!!!*	0x20	-21	12	OK
	P.nbr.	Time (ms) +3	Length	Dest. Address	Source Address	Applicaton payload AraMi	User Port	RSSI (dBm)	LQI	FCS
	3	=6	21	87 56 34 12	54 76 03 05	S!!!*	0x20	-22	25	OK
ve	P.nbr.	Time (ms) +3	Length	Dest. Address	Source Address	Applicaton payload AraMi	User Port	RSSI (dBm)	LQI	FCS
	4	=9	21	87 56 34 12	54 76 03 05	S!!!*	0x20	-21	13	OK
K	P.nbr.	Time (ms) +3	Length	Dest. Address	Source Address	Applicaton payload AraM1	User Port	RSSI (dDm)	LQI	FCS
. I	5	=12	21	87 56 34 12	54 76 03 05	S!!!*	0x20	-22	17	OK
b	P.nbr.	Time (ms) +3	Length	Dest. Address	Source Address	Applicaton payload AraMi	User Port	RSSI (dBm)	LQI	FCS
	6	=15	21	87 56 34 12	54 76 03 05	S!!!*	0x20	-21	24	OK
	P.nbr.	Time (ms) +3	Length	Dest. Address	Source Address	Applicaton payload AraMi	User Port	RSSI (dBm)	LQI	FCS
	7	=18	21	87 56 34 12	54 76 03 05	S!!!*	0x20	-21	13	OK
er	<			IIII						



Conclusion

- The wiring and data harness has been reduced by the proposed smart harness technique
- The proposed spacecraft configurations are very flexible and modular
- The proposed test board can easily test the modules, tiles and whole satellites
- The modularity has been achieved at mechanical, electrical, protocol and testing level.
- Multiple communication protocols realizable in small spacecrafts using proposed intelligent mapping
- Optical and radio frequency based module design for innovations in on-board communication and highly reduction in harness mass

Thank You !!!



References

[1]. Komninou, M.Vasile, E. Minisci, <u>Optimal Power Harness Routing for Small-Scale</u> <u>Satellite</u>, in: IAC-11,C3,3,5,x10550, 62nd International Astronautical Congress, 3-7 October 2011, Cape Town, South Africa.