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Testing of a Power Management Module for Modular Satellites

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Acknowledgements

I will start dedicating my master thesis to my mother, my father and my sister.

First of all I would like to thank my family, to support me at all and helping me during my career, especially in my eighteen months in Torino studying my last academic year and master thesis.

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Valencia, April 10th, 2015

Eduardo Mollà Muñoz

Summary

Avionics for satellites is a market which is continuously expanding in the recent years, especially due to the availability of low cost launch vectors. The reduction of the cost allowed many institutions and universities to develop their own satellites. The Politecnico di Torino has also followed this trend in the early 2000 and developed its own satellite which is called PiCPoT (Piccolo Cubo del Politecnico di Torino). The main purpose of PiCPoT is to test commercial components (COTS) in space and collect scientific data for research.

After that, Politecnico di Torino starts a further step on cube satellite research field. The new project is called AraMiS which is the Italian acronym for Modular Architecture for Satellites. The project wants to go beyond the CubeSat concept and create a true modular architecture, particularly in the electronic subsystem. The satellite can use as many basic modules as necessary to achieve the mission tasks. Therefore, the AraMiS architecture will lead to an effective cost sharing between different missions since the same module design is adopted in several satellites.

The ARAMIS project aims to achieve a reconfigurable modular satellite, in which each module is designed in a way independent from each other, but at the same time, they can work with other modules of the same type or different, to increase the overall system performance.

The subject of this thesis is to test a power management module of a modular satellite. In Chapter 1, it gives a basic idea of general module architecture, the integrated subsystems and module interfaces. In Chapter 2, the several individual blocks of the module of the modular satellite are introduced theoretically, some of them are the voltage and current sensors, the regulators and the MPPT. Also some simulation problems founded during the test were explained, the modifications of the schematic were exposed and some future improvements are introduced. Chapter 3 is focused on the solar cell, the first point is a study of the simulation model of the solar cell, the second explains the procedure of fabrication the physical model and its test and finally, the last points, expose the characterization of the solar cell.

After that, in Chapter 4 the individual block simulations were done to check the expected behavior, once achieved, after get all simulation models, the entire power management system simulation was done. To end the chapter, the ripple of the regulators was exposed. In Chapter 5, the power management honeycomb board was tested, giving importance at regulators and the PDB, several tables with data about the operational ranges regarding to the input and output voltage and current were included. The temperature of the components was measured and some photos took with the thermal camera were included. To end the chapter, the real ripple of the regulators and the MPPT was compared with the theoretical.

The Chapter 6 is a comparison between the Chapter 4 and 5, contrasting the simulation signals with the real measurements. The real voltage and current ranges of the regulators are compared with the datasheet of the components.

To give a conclusion, the last chapter concludes what has been done in this thesis work and proposes future works in order to improve the functional testing system described in this thesis.

Contents

Chapter 1

Introduction

Our goal is to simulate the Power Management Honeycomb schematic, to being more exact, the analog part of that. After to do the measurements, it is going to compare these with the real values of the Power Management Honeycomb physical PCB.

1.1 – CubeSat concept

Cubesat [1] is a type of miniaturized satellite for space research that usually has a volume of exactly one liter (10 cm cube), has a mass of no more than 1.33 kilograms and typically uses COTS (Commercial Off The Shelf) electronics components. At the beginning of 1999, California Polytechnic State University and Stanford University developed the Cubesat specifications to help universities worldwide to perform space science and exploration.

The Cubesat specification accomplished several high-level goals. Simplification of the satellite's infrastructure makes it possible to design and produce an operating satellite at low cost. Encapsulation of the launcher-payload interface takes away the prohibitive amount of managerial work that would previously be required for mating a piggyback satellite with its launcher. Unification among payloads and launchers enables quick exchanges of payloads and utilization of launch opportunities on short notice.

The standard 10x10x10 cm basic Cubesat is often called a “1U” Cubesat meaning one unit. And they are scalable along only one axis, by 1U increments. Since Cubesats are all 10x10 (regardless of length) they can all be launched and deployed using a common deployment system which is called a Poly-PicoSatellite Orbital Deployer. P-PODs are mounted to a launch vehicle and carry Cubesats into orbit and deploy them once the proper signal is received from the launch vehicle.

Figure 1.1. CubeSat.

1.2 – PiCPoT

The Department of Electronics & Telecommunication Engineering, in collaboration with the Department of Aerospace Engineering at Politecnico di Torino started work on the PICPOT (Small Cube of Politecnico di Torino) project in January 2004.The major objective of the project was to design, implement and launch experimental satellite into Low Earth Orbit (LEO) with the aims to:

- Check the operation and reliability of COTS components in space.
- Acquire and transmit to Earth Station several images and measurements carried into orbit by the on-board sensors.
- Take Earth's surface images.
- Encourage and create interdisciplinary activities to enhance the interaction and coordination of various departments, faculty, PhD students and other students of the Politecnico.

The PICPOT was a satellite of cubic structure with dimensions 13 x 13 x 13 cm and a mass of 2.5 kg. It was intended to be launched together with other university satellites by a DNEPR LV rocket in July 2006. Unfortunately a problem in the first stage of the carrier led to destruction of all satellites and our aim of going to space could not be accomplished.

Then afterwards, we started working on a completely modular and flexible architecture called AraMiS.

1.3 – AraMiS

AraMiS (Modular architecture for Satellites) is a project that wants to take further the CubeSat concept and create a true modular architecture. The design approach of AraMiS architecture is to provide low-cost and high performance space missions with dimensions larger than CubeSats. The feature of AraMiS design approach is modularity and scalability. These modules can be reused for multiple missions which helps in significant reduction of the overall budget, development and testing time. One has just to reassemble the required subsystems to achieve the targeted specific mission.

This architecture is intended for different satellite missions, from small systems weighing from 1kg to larger missions. Figure 1.2 depicts a number of configurations that show the potential capabilities of the proposed architecture. Modularity has been implemented in different ways. From the mechanical perspective, larger satellite structures can be conveniently realized by combining several small modular structures. The modularity concept has also been intended from electronic standpoint. Most of the internal subsystems are developed in such a manner they can be composed together to enhance performance. One such example is the power management subsystem. In conventional missions: to get maximum solar power, solar cells are mounted on all the available surfaces but their number can be different in various missions, thus requiring to re-design each time. This new modular approach makes use of a standard module, as can be seen in figure 1.2 which can be replicated many time to fit mission requirements.

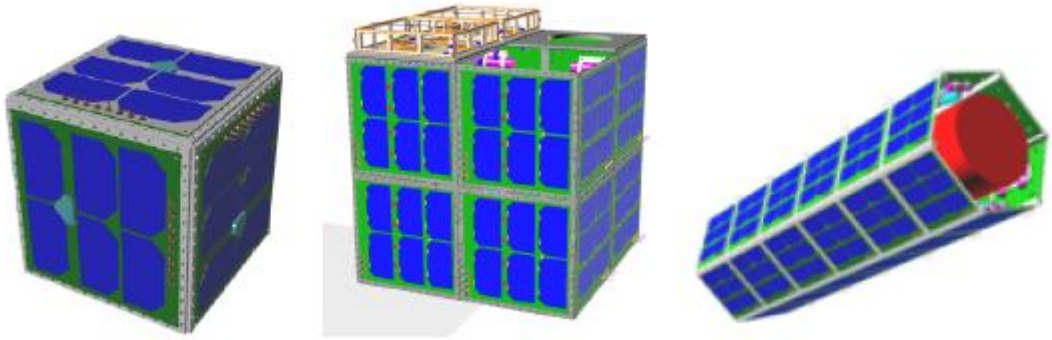


Figure 1.2. Different AraMiS satellites architecture.

1.3.1 – AraMiS subsystems

The AraMiS satellites can achieve the desired flexibility level by combination of several subsystems together. The subsystems of this architecture are:

- Mechanical subsystem.
- Power management subsystem.
- On-board processing subsystem.
- Payload support.
- Telecommunication subsystem.
- Ground segment.

1.3.1.1 – Mechanical subsystem

The mechanical subsystem of AraMiS [2], which is intended for very-low cost satellites, should be as simple as possible (with side not longer than 50 cm). It should have a standard size and the main material used for building the AraMiS structure is Aluminum, to support all the components of the tile. Design screw holes which ensures high mechanical strength, together with an excellent electromagnetic insulation. All of these characteristics allow reducing the overall weight and cost and should also simplify assembling and testing the satellite.

A suitable choice allows a certain degree of freedom in the shape and size of the satellite. A few possibilities could be:

- smallest cubic shape (15 × 15 × 15 cm3 satellite)
- larger cubic (or prismatic) shape (15n × 15m × 15q cm3 satellite)
- small hexagonal/octogonal satellite
- larger satellites (larger than 50 cm in side)

Figure 1.3. AraMiS mechanical structure.

1.3.1.2 – Power management subsystem

The power management subsystem is responsible for generating, storing and delivering power to all the other satellite subsystems. It is one of the most critical subsystem as a failure here can lead to shutting down everything. Fault tolerance is an important parameter and most of the design solutions were selected for this reason.

As for most satellites, the main power sources are solar panels: in AraMiS they are mounted all around the satellite to reduce the complexity of mechanical assembly. Since they are mounted on different faces, experiencing different light and thermal conditions, their output power is highly variable: we therefore need a separate solar panel controller for each of them and this controller should be as small and lightweight as possible. Since our goal is to use COTS components to build a highly reliable system we need to implement different strategies to keep the cost as low as possible and to increase fault tolerance.

The power generation system is therefore really modular, since it is composed by this tile, replicated as many times as needed to get the desired power. All these tiles work in parallel and this redundant solution helps also from the fault tolerance point of view, making the system able to tolerate multiple faults and allowing a graceful performance degradation. For example, if we put onboard two different payloads with different power consumptions, when all the Power Management tiles are working, we are able to use both payloads; if some of the power generating modules get faulty, we are still able to use one of the payloads. The system is still running but with reduced performances. The solar panel controllers (SPC), a Maximum Power Point Tracker (MPPT), is responsible for tracking the maximum power point of the solar panel according to instantaneous environmental conditions. The system is a switch-mode power supply which allows to change the load seen by the solar cells to extract maximum power.

1.3.1.3 – On-board processing subsystem

Tile Computer (OBC) used in AraMiS satellites consist of redundant MSP430 microcontrollers and FPGAs, that are mainly responsible for overall satellite system management. Some of the key responsibilities perform by OBC includes:

- Creating and transmitting (by Transceiver board) Beacon packets,
- Decoding and executing commands,
- Executing attitude control algorithm,
- Storing housekeeping data,
- Controlling Payload sub-systems.

1.3.1.4 – Payload support

The payload is heavily mission dependent and the architecture was developed to allow high flexibility on it: the main requirements that the AraMiS architecture impose on the payload is its compatibility with the tile power distribution and data bus. Different payloads can be fitted in the various configurations but mechanical fixtures should be developed to connect them to the mechanical structure. A view of the payload inside AraMiS is shown in figure below.

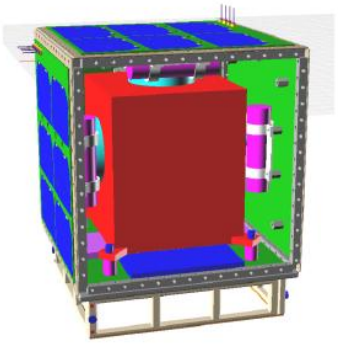


Figure 1.4. AraMiS payload.

1.3.1.5 – Telecommunication subsystem

The AraMiS telecommunications subsystem follows the modularity concept. There is a basic telecommunication tile that is provided in a standard AraMiS satellite. In case of special applications, dedicated tiles can be added to meet mission criteria. This module is used to receive command and control packets from the ground station and to send back telemetry and status information. The bandwidth needed to exchange this kind of information is usually low, so the RF link was designed for low speed and low power. The module has been designed using COTS components which were selected to achieve good fault tolerance level. There are two different frequency bands used for satellite and ground communication: the UHF 437MHz band and the SHF 2.4 GHz band. To reduce occupied bandwidth, both channels are implemented using half-duplex protocol, sharing the same frequency for downlink and uplink. AraMiS telecommunication module are shown in figure below.

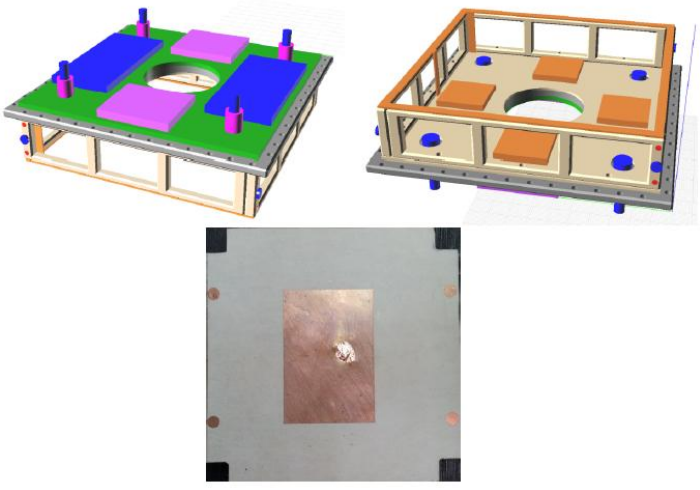


Figure 1.5. AraMiS telecommunication module.

1.3.1.6 – Ground segment

The Ground station [3] uses a parabolic antenna (28dB gain) for S-band and an helical antenna (14dB gain) for UHF. The antennas share a single rotator, controlled by a PC. The UHF section is based on commercial equipment: the received signal is amplified by a LNA and fed to a Yaesu FT847 transceiver. Baseband data is converted by a TNC. The same PC controlling the rotator manages the received telemetry data or picture. On uplink, commands are assembled by the PC, converted in analog via the audio board and sent to the FT847. Output power is up to 50W. The S-band system is derived from the satellite architecture. The received signal is amplified by an LNA (Kuhne LNA2227A) and fed to a CC2400 used as a receiver. The device is controlled by a PIC microcontroller swhich collects the output stream and temporarily stores it. The PIC communicates via RS232 with the PC. The uplink commands originate from the PC and transferred to the PIC, which controls the antenna switch and a second CC2400 used as a transmitter. The RF signal is amplified by a PA (Kuhne KU2325A) to a maximum of 20W and fed to the antenna.

Chapter 2

Analysis of the schematic

Our goal is to simulate the Power Management Honeycomb schematic, to being more exact, the analog part of that. After to do the measurements, it is going to compare these with the real values of the Power Management Honeycomb physical PCB.

For the simulations, is used the Mentor Graphics software. Before start the analysis, it had to tune up several parts of the circuit and some properties of the software that it is going to detailing at next point.

In this chapter, it is going to describe the primary switching buck with the MPPT and the voltage regulators. In addition, it is explained some simulation problems and is exposed the final Primary Switching Buck schematic result after have done some changes. To conclude this chapter, it is going to show some future improvements.

2.1 – Primary switching buck

Primary switching buck is composed for two voltage sensors, two current sensors, a PWM to DC converter and a MPPT (*Maximum Power Point Tracking*).

Primary switching buck converter with maximum power point tracker (MPPT) converts solar panel power to power distribution bus (PDB) voltage. This PDB is available directly on each connector and also to charge the batteries. A number of switching and linear regulators convert the PDB voltage to low voltage levels (i.e. 3 V, 3.3 V and 5 V) used by all subsystem components.

Primary switching buck contains two current sensors and two voltage sensors that constantly monitor the solar panel output and the PDB. They have these characteristics:

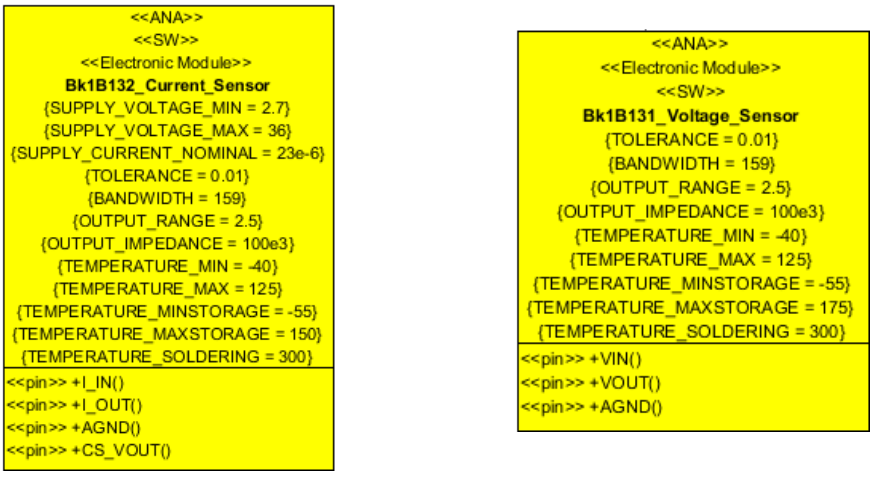


Figure 2.1. Current and Voltage sensor UML class diagram.

2.1.1 – 1B132E_LowSideCurrentSensor_V1

This current sensor is composed with a OA MAX4091, [4] which generates at output CS_VOUT, a voltage proportional at the current I_S which pass across the input resistor.

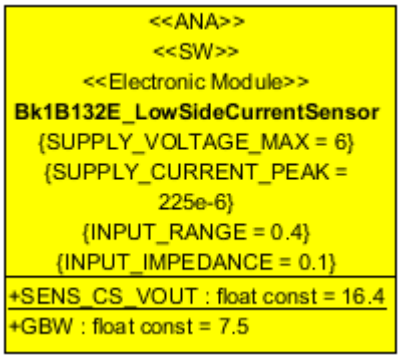


Figure 2.2. Low Side Current Sensor UML class diagram.

The following is the circuit used for this sensor [19]:

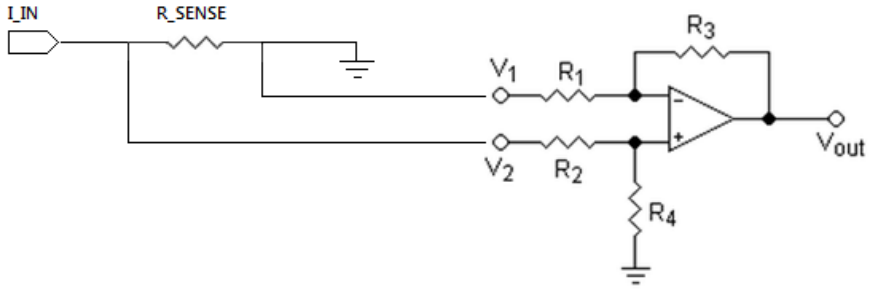


Figure 2.3. Low Side Current Sensor circuit.

And this is the equation to calculate the V_{OUT}:

$$V_{OUT} = V2 \times \left(\frac{(R3 + R1) \times R4}{(R4 + R2) \times R1}\right) - V1 \times \left(\frac{R3}{R1}\right)$$

In our case, V1 is always zero, because V1 is connected to ground. So our equation is simplified:

$$V_{OUT} = V2 \times \frac{(150k + 2k) \times 150k}{(150k + 2k) \times 2k} = V2 \times 75$$

To calculate the gain:

$$A_V = \frac{V_{OUT}}{V2} = 75$$

$$V_{OUT} = I\_IN \times R\_SENSE \times A_V$$

So the minimum and maximum values are:

$$V_{OUT\_MIN} = 0$$

$$V_{OUT\_MAX} = 0.4 \times 0.1 \times 75 = 3\ V$$

$I\_IN_{\_MAX}$ takes the value of the input range. And R_SENSE is equal to 100 mΩ.

We note that the output range of current sensors is 2.5, but the output_range for this sensor, for the maximum input_range, is 3. We just did the calculations, because this sensor was already done, we did not any modification.

To view the schematic of the project go to Appendix A.

2.1.2 – 1B132C_Current_Sensor_V1

This current sensor is composed with a OA INA138, [5] which generates at output CS_VOUT, a voltage proportional at the current I_S which pass across the resistor of 50 mΩ.

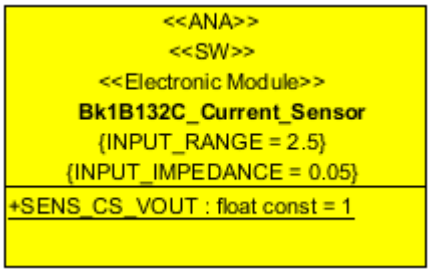


Figure 2.4. Current Sensor UML class diagram.

This is the circuit used for this sensor:

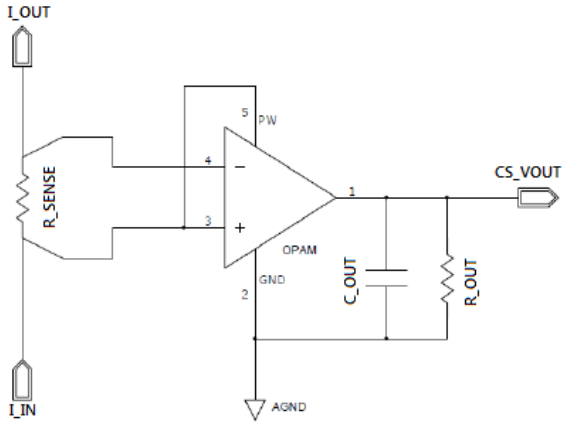


Figure 2.5. Current Sensor circuit.

To calculate the V_{OUT} , observing the INA138 features at its datasheet, it must take in account the transconductance value: gm = 200 μAV^{-1}. So the output voltage is:

$$V_{OUT} = I_{IN} \times R_{SENSE} \times gm \times R_{OUT}$$

So the minimum and maximum values are:

$$V_{OUT\_MIN} = 0$$

$$V_{OUT\_MAX} = 2.5 \times 0.05 \times 200 \times 10^{-6} \times 100 \times 10^{3} = 2.5\,V$$

$I\_IN_{\_MAX}$ takes the value of the input range.

To view the schematic of the project go to Appendix A.

2.1.3 – 1B131D_Voltage_Sensor_V1

This voltage sensor is composed for two resistors and a capacitor.

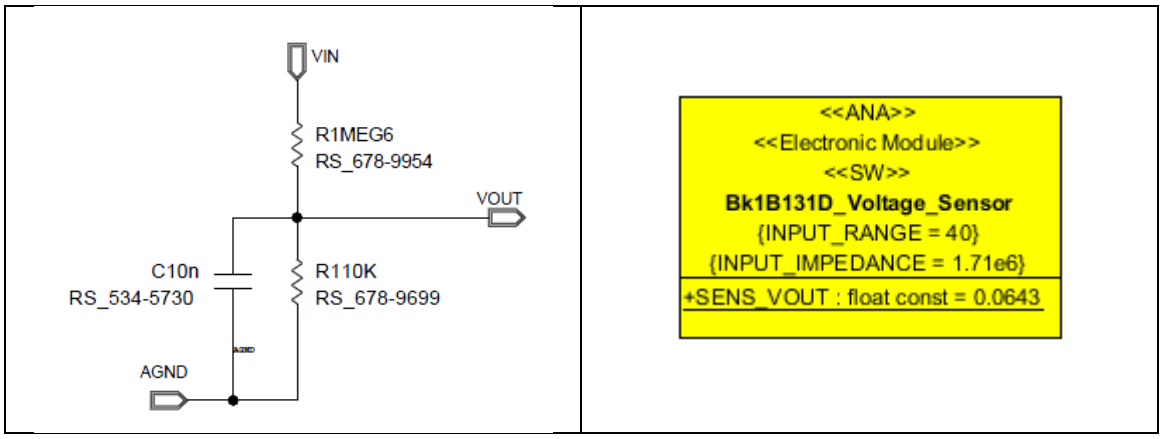


Figure 2.6. Voltage Sensor circuit and UML class diagram.

The output voltage is calculated as following:

$$V_{OUT} = V_{IN} \times \frac{R2}{R1 + R2} = V_{IN} \times \frac{110 \times 10^3}{1.6 \times 10^6 + 110 \times 10^3}$$

So the minimum and maximum values are:

$$V_{OUT\_MIN} = 0$$

$$V_{OUT\_MAX} = 40 \times \frac{110 \times 10^3}{1.6 \times 10^6 + 110 \times 10^3} \cong 2.5\,V$$

V_IN_MAX takes the value of the input range.

To view the schematic of the project go to Appendix A.

2.1.4 – 1B131C_Voltage_Sensor_V1

This voltage sensor is composed for two resistors and a capacitor.

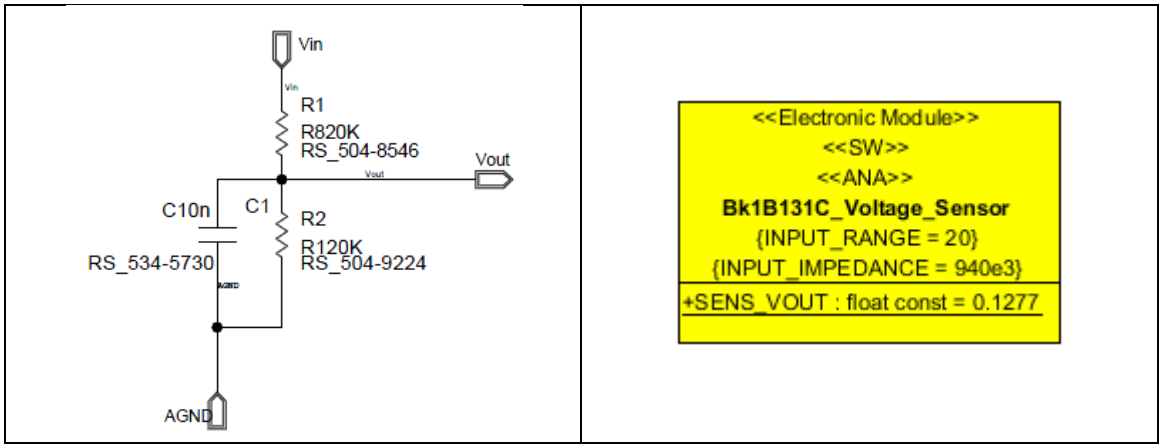


Figure 2.7. Voltage Sensor circuit and UML class diagram.

The output voltage is calculated as following:

$$V_{OUT} = V_{IN} \times \frac{R2}{R1 + R2} = V_{IN} \times \frac{120 \times 10^3}{820 \times 10^3 + 120 \times 10^3}$$

So the minimum and maximum values are:

$$V_{OUT\_MIN} = 0$$

$$V_{OUT\_MAX} = 20 \times \frac{120 \times 10^3}{820 \times 10^3 + 120 \times 10^3} \cong 2.5\,V$$

V_IN_MAX takes the value of the input range.

To view the schematic of the project go to Appendix A.

2.1.5 – 1B1122_PWM_DC_Converter_V1

The PWM DC Converter, converts the PWM input to a DC output signal. Our block has two inputs, the supply and the PWM input, the DC output and the ground. For the test of the Honeycomb Tile and to do the simulations with the same characteristics, in order to compare the both results, it is set the PWM input to 0 V at the simulations, because at the Honeycomb Tile this input comes to the microprocessor MSP430, and this was set to 0 V. Moreover, at point 3.5 of this chapter are explained future improvements changing the duty cycle of the PWM input, so it is studied the behavior of this block with different duty cycle input signal.

Going back to our issue, for the case mentioned above, setting the PWM_IN to 0 V and VCC_3V3 to 3.3 V at the Mentor Graphics simulation, it is obtained approximately 2.6 V at the DC_OUT. This output is used for the MPPT block as voltage reference.

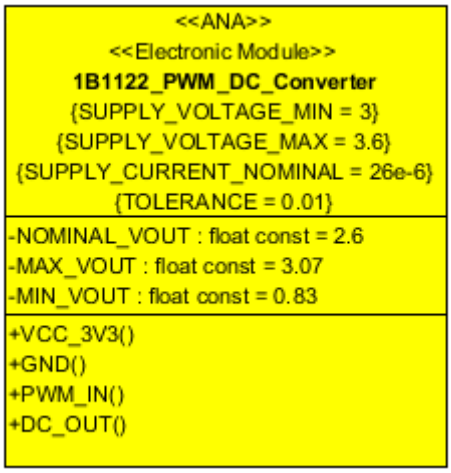


Figure 2.8. PWM to DC Converter UML class diagram.

To view the schematic of the project go to Appendix A.

2.1.6 – 1B1121C_MPPT_V1

The buck converter with maximum power point tracker (MPPT) operates solar panel signals and converts solar panel power to power distribution bus (PDB) voltage.

The switching of buck converter for maximum power point tracking is controlled using an MPPT block, [16] [18] which consists of a hysteric comparator and a MOS driver block. The comparator output is used to control the MOS driver pulses depending on the duty cycle. The output voltage of MPPT rises until the power distribution bus voltage level. To supply the comparator is used a LM2936 regulator, [6] this is exposed at following point.

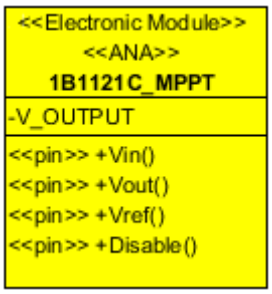


Figure 2.9.MPPT UML class diagram.

To view the schematic of the project go to Appendix A.

2.1.6.1 –1B1121C_LowPowerReg_V1

The LM2936 ultra-low quiescent current regulator features low dropout voltage and low current in the standby mode. With less than 15-µA quiescent current at a 100-µA load, the LM2936 is ideally suited for automotive and other battery operated systems. The LM2936 retains all of the features that are common to low dropout regulators including a low dropout PNP pass device, short circuit protection, reverse battery protection, and thermal shutdown. The LM2936 has a 40-V maximum operating voltage limit, a −40°C to 125°C operating temperature range, and ±3% output voltage tolerance over the entire output current, input voltage, and temperature range. Fixed 3-V, 3.3-V or 5-V with 50-mA output.

In our project, the regulator has these features: maximum output current 0.05 A, input voltage range 4 V – 40 V and the fixed output voltage 5 V.

The simplified schematic is shown below:

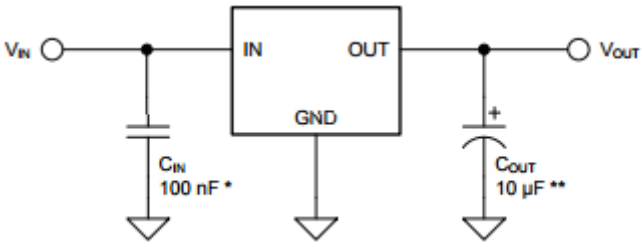


Figure 2.10. Low Power Regulator simplified schematic.

Thw Top View is the following:

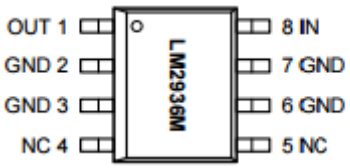


Figure 2.11. Low Power Regulator top view.

And the pin functions are:

Pin	Name	Description
1	OUT	Regulated output voltage. Requires a minimum output capacitance, with specific ESR, on this pin to maintain stability.
2,3,6,7	GND	Ground.
4,5	NC	No internal connection, connect to GND, or leave open.
8	IN	Unregulated input voltage.

Table 2.1. Low Power Regulator pin functions.

The components used at our project are shown below:

Component	Value	Part number
C_{IN}	100 nF	RS_616-9391
C_{OUT}	10 µF	DK_399-3525-6-ND
R_{OUT}	1 Ω	RS_504-8978

Table 2.2. Low Power Regulator components.

To view the schematic of the project go to Appendix A.

2.2 – Voltage regulators

The board has different levels of distributed power bus [18]. This section details about the power regulators that have been used for different types of switching and linear power supplies. Switching and linear regulators have been utilized to output the fixed voltage and distribute all across the subsystems and pluggable modules. Any desired output voltage can be obtained from the solar power by using the appropriate circuitry.

2.2.1 – 1B1253A_5V_5A_Regulator_V2

To achieve 5 V – 5 A, in our project is used a TPS5450 regulator, [7] which has a variable output setting an external resistor divider, the following are the description and the features:

The TPS5450 is a high-output-current PWM converter that integrates a low-resistance, high-side N-channel MOSFET. Included on the substrate with the listed features are a high-performance voltage error amplifier that provides tight voltage regulation accuracy under transient conditions; an undervoltage-lockout circuit to prevent start-up until the input voltage reaches 5.5 V; an internally set slow-start circuit to limit inrush currents; and a voltage feed-forward circuit to improve the transient response. Using the ENA pin, shutdown supply current is reduced to 18 μA typically. Other features include an active-high enable, overcurrent limiting, overvoltage protection and thermal shutdown. To reduce design complexity and external component count, the TPS5450 feedback loop is internally compensated.

It has Enable Input and it is active high, any voltage above 1.3 V is considered logic high, any voltage below 0. 5 V is considered logic low. It has wide input voltage range: 5.5 V to 36 V, fixed 500 kHz switching frequency for small filter size and operation junction temperature range between -40ºC to 125ºC. The output voltage of the regulator is set by feeding back the center point voltage of an external resistor divider network to the VSENSE pin. In steady-state operation, the VSENSE pin voltage should be equal to the voltage reference 1.221 V.

The TPS5450 device is a 36-V, 5-A, step-down regulator with an integrated high-side MOSFET. This device is typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 5 A. TPS5450 is usually applied in circuits of high density point-of-load regulators, battery chargers, 12 V and 24 V distributed power system and so on.

The typical application circuit is shown below:

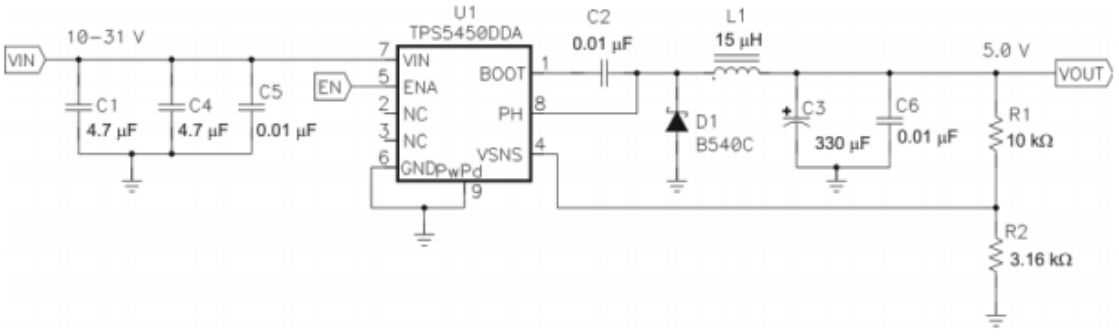


Figure 2.12. TPS5450 typical application.

To calculate the desired output voltage or the values for R1 and R2, is used this equation:

$$R2 = \frac{R1 \times 1.221}{V_{OUT} - 1.221}$$

In our case, fixing R1 to 10 kΩ and th output voltage to 5 V, is obtained a R2 ≈ 3.230 kΩ.

The Top view of the IC:

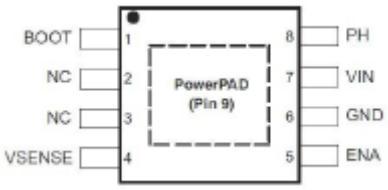


Figure 2.13. TPS5450 top view.

And the Pin Descriptions:

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	1	O	Boost capacitor for the high-side FET gate driver. Connect 0.01-µF, low-ESR capacitor from BOOT pin to PH pin.
NC	2, 3	–	Not connected internally.
VSENSE	4	I	Feedback voltage for the regulator. Connect to output voltage divider.
ENA	5	I	On and off control. Below 0.5 V, the device stops switching. Float the pin to enable.
GND	6	–	Ground. Connect to PowerPAD.
VIN	7	I	Input supply voltage. Bypass VIN pin to GND pin close to device package with a high-quality, low-ESR ceramic capacitor.
PH	8	O	Source of the high-side power MOSFET. Connected to external inductor and diode.
PowerPAD	9	–	GND pin must be connected to the exposed pad for proper operation.

Table 2.3. TPS5450 pin functions.

These are the components used at our project (name of the components corresponds with the names of the project, not of typical application circuit nomenclature):

Component	Value	Part Number
C_1	47 µF	DK_445-3486-1-ND
C_2	47 µF	DK_445-3486-1-ND
C_3	10 nF	RS_534-5730
C_4	10 nF	RS_534-5730
C_5	220 µF	DK_478-3303-1-ND
R_3	10 kΩ	RS_504-8934
$R_1 + R_2$	3.01 kΩ + 220 Ω	RS_505-1081 + RS_505-0303
D_1	Diode Schottky	DK_B550C-FDICT-ND
L_1	15 µH	DK_PCD2154CT-ND

Table 2.4.TPS5450 components for 5V, 5A regulator.

To view the schematic of the project go to Appendix A.

2.2.2 – 1B1254D_3V3_1A6_Mixed_Regulator_V2

To get a 3.3 V – 1.6 A is used two stages regulator. The description and the schematic are shown below.

The top level block has 3.3 V output, maximum current 1.6 A and 3% accuracy at full load. It is a mixed regulator having two stages. The first stage is a switching stage with high efficiency, from PDB to 4 V. The first stage has the same structure of the block 1B1253A_5V_5A_Regulator_V2, but in this case the output voltage is 4 V.

The second stage has a linear regulator with provides more stable supply for sensitive devices, that converts from 4 V to 3.3 V. This regulator has been designed specifically to drive micro controllers that are prone to supply distortions.

The top level block diagram is shown below:

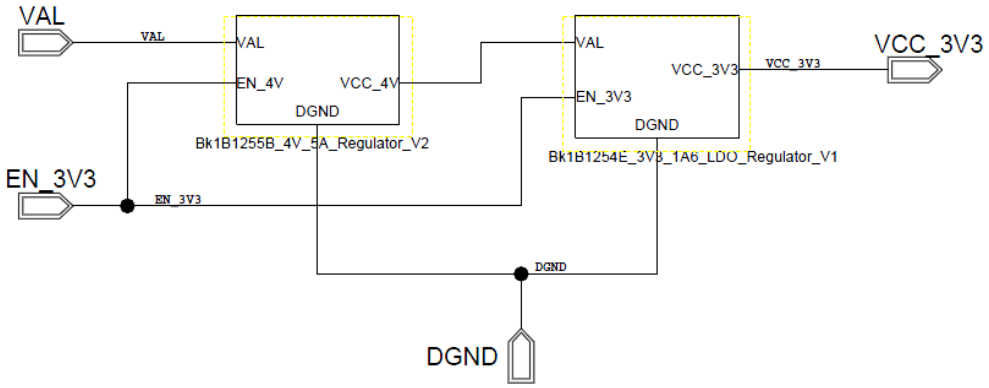


Figure 2.14. Mixed Regulator top level block diagram.

2.2.2.1 – 1B1255B_4V_5A_Regulator_V2

The first stage of the mixed regulator have the same structure of the 5 V, 5 A regulator, [7] just changing the value of the resistor R2 to obtain 4 V output voltage. The list of components and the calculation of R2 is shown below.

These are the components used at our project (name of the components corresponds with the names of the project, not of typical application circuit nomenclature):

Component	Value	Part Number
C_1	47 µF	DK_445-3486-1-ND
C_2	47 µF	DK_445-3486-1-ND
C_3	10 nF	RS_534-5730
C_4	10 nF	RS_534-5730
C_5	220 µF	DK_478-3303-1-ND
R_3	10 kΩ	RS_504-8934
$R_1 + R_2$	2.2 kΩ + 2.2 kΩ	RS_505-0319 + RS_505-0319
D_1	Diode Schottky	DK_B550C-FDICT-ND
L_1	15 µH	DK_PCD2154CT-ND

Table 2.5. TPS5450 components for 4V, 5A regulator.

To calculate the value of R2, is used the previous equation. In our case, fixing R1 to 10 kΩ and the output voltage to 4 V, is obtained:

$$R2 = \frac{R1 \times 1.221}{V_{OUT} - 1.221} = \frac{10k \times 1.221}{4 - 1.221} \approx 4.4\,k\Omega$$

To view the schematic of the project go to Appendix A.

2.2.2.2 –1B1254E_3V3_1A6_LDO_Regulator_V1

For the second stage is used a low-dropout linear regulator. It is exhibit below.

The LT 1963 series are low dropout regulators optimized for fast transient response [8]. The devices are capable of supplying 1.5 A of output current with a dropout voltage of 340mV. Operating quiescent current is 1 mA, dropping to <1 µA in shutdown. Quiescent current is well controlled; it does not rise in dropout as it does with many other regulators. In addition to fast transient response, the LT1963 regulators have very low output noise which makes them ideal for sensitive RF supply applications.

Output voltage range is from 1.21 V to 20 V. The LT1963 regulators are stable with output capacitors as low as 10 µF. Internal protection circuitry includes reverse battery protection, current limiting, thermal limiting and reverse current protection. The devices are available in fixed output voltages of 1.5V, 1.8V, 2.5V, 3.3V and as an adjustable device with a 1.21V reference voltage. The input range is from 2.5 V to 20 V (2.5 V is the minim input voltage for the LT1963-1.5, in our case, for the LT1963-3.3, the minimum input voltage is 4.3 V) and the operating junction temperature range is from -40ºC to 125ºC.

The typical application circuit is the following:

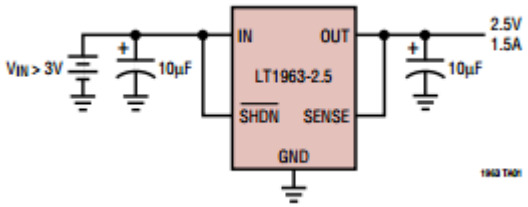


Figure 2.15. 3.3V, 1.6A regulator typical application.

The LT1963 regulators are designed to be stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. A minimum output capacitor of 10µF with an ESR in the range of 50mΩ to 3Ω is recommended to prevent oscillations. Larger values of output capacitance can decrease the peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the LT1963, will increase the effective output capacitor value.

The Front view of the IC:

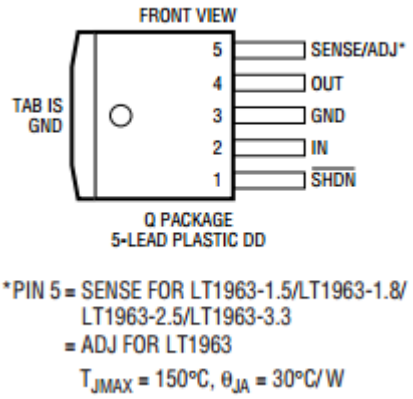


Figure 2.16. 3.3V, 1.6A regulator front view.

And the Pin Descriptions:

Pin	Name	Description
1	SHDN	Used to put the LT1963 regulators into a low power shutdown state. The output will be off when the SHDN pin is pulled low.
2	IN	Input. Power is supplied to the device through the IN pin.
3	GND	Ground.
4	OUT	The output supplies power to the load. A minimum output capacitor of 10µF is required to prevent oscillations.
5	SENSE/ADJ	For fixed voltage. For the adjustable LT1963, this is the input to the error amplifier.

Table 2.6. 3.3V, 1.6A regulator pin descriptions.

At our project the values for the capacitors are:

Component	Value	Part number
C_{IN}	10 µF	DK_399-3525-6-ND
C_{OUT}	10 µF	DK_399-3525-6-ND

Table 2.7. 3.3V, 1.6A regulator components.

To view the schematic of the project go to Appendix A.

2.2.3 – 1B1252A_3V0_1000ppm_Reference_V1

To achieve 3.0 V is used a series voltage reference. Following is presented LM4128 [9].

LM4128 precision voltage reference is ideal for space critical applications. The LM4128's advanced design eliminates the need for an external stabilizing capacitor while ensuring stability with capacitive loads up to 10 µF, thus making the LM4128 easy to use.

Series references provide lower power consumption than shunt references, since they do not have to idle the maximum possible load current under no load conditions. This advantage, the

low quiescent current and the low dropout voltage make the LM4128 ideal for battery-powered solutions.

The LM4128 is available in four grades (A, B, C, and D) for greater flexibility. The best grade devices (A) have an initial accuracy of 0.1% with guaranteed temperature coefficient of 75 ppm/°C or less, while the lowest grade parts (D) have an initial accuracy of 1.0% and a 73 temperature coefficient of 100 ppm/°C. We choose the device of grade A in application.

LM4128 is widely applied in instrumentation and process control, test equipment, data acquisition systems, base stations, battery powered equipment, battery chargers and so on.

It has Enable Input and it is active high. In our case, the voltage input for the LM4128 is 5 V. Any voltage from 3.25 V to 5 V is considered logic high, any voltage below 1.75 V is considered logic low. It has 3.0 V reference output (but the voltage options are 1.8 V, 2.048 V, 2.5 V, 3.0 V, 3.3 V and 4.096 V), 60 µA supply current, maximum 20 mA output current and 0.1% accuracy at full load. The temperature range between -40ºC to 125ºC.

The typical application circuit is shown below:

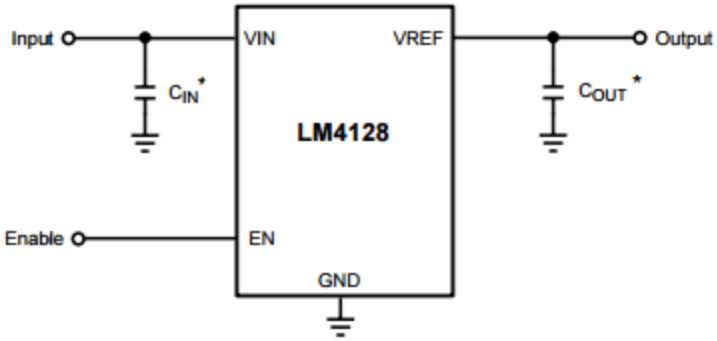


Figure 2.17. 3.0V, 1000ppm reference typical application.

The capacitor C_{IN} is required and the capacitor C_{OUT} is optional.

The Top view of the IC:

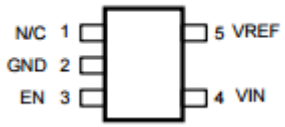


Figure 2.18. 3.0V, 1000ppm reference top view.

And the Pin Descriptions:

Pin #	Name	Function
1	N/C	No connect pin, leave floating
2	GND	Ground
3	EN	Enable pin
4	VIN	Input supply
5	VREF	Reference output

Table 2.8. 3.3V, 1.6A regulator pin descriptions.

A small capacitor on the input must be used to ensure stable operation. The value of C_{IN} must be sized according to the output capacitor value. The value of C_{IN} must satisfy the relationship $C_{IN} \geq C_{OUT}$. When no output capacitor is used, C_{IN} must have a minimum value of 0.1 μF. Noise on the power-supply input may affect the output noise. Larger input capacitor values (typically 4.7 μF to 22 μF) may help reduce noise on the output and significantly reduce overshoot during startup. Use of an additional optional bypass capacitor between the input and ground may help further reduce noise on the output. With an input capacitor, the LM4128 will drive any combination of resistance and capacitance up to V_{REF}/20 mA and 10 μF respectively.

The LM4128 is designed to operate with or without an output capacitor and is stable with capacitive loads up to 10 μF. Connecting a capacitor between the output and ground will significantly improve the load transient response when switching from a light load to a heavy load. The output capacitor should not be made arbitrarily large because it will affect the turn-on time as well as line and load transients.

The components used at our project are shown below:

Component	Value	Part number
C_{IN}	4.7 μF	DK_PCC2325CT-ND
C_{OUT}	100 nF	RS_616-9391

Table 2.9. 3.3V, 1.6A regulator components.

To view the schematic of the project go to Appendix A.

2.3 – Simulation problems

2.3.1 – Problem 1: simulation models

One of the first problems that appears was about the simulation models, due that there was not practically no one of them, and these are necessary to get the simulations. The following, are the simulation models that have found on the website or have wrote by hand.

2.3.1.1– Models founded on internet:

- **DIODE:** UPR60
- **SCHOTTKY DIODES:**
  - B550C
  - BAT54_SCHOTTKY
  - STPS3L60U
- **PMOS:** ZXMP6A16K
- **NMOS:** DI_2N7002A (The diode used at the project is: BS170F [10], but this model did not find on internet, therefore is used the DI_2N7002A [11] model which presents similar features. At the following table we can see the characteristics of both diodes:)

PARAMETER	2N7002A	BS170F
$\mathbf{V_{DSS}}$	60 V	60 V
$\mathbf{R_{DSon(max)}}$	< 5 Ω (@10 V)	5 Ω
$\mathbf{I_D}$	0.20 A	0.15 mA
$\mathbf{V_{GS}}$	± 18 V	± 20 V
$\mathbf{P_{TOT}}$	0.35 W	0.33 W
$\mathbf{V(BR)_{DSS}}$ *	60 V (I_D=250 µA, V_{GS}=0 V)	60 V (I_D=100 µA, V_{GS}= 0V)
$\mathbf{I_{DSS}}$ ($\mathbf{V_{GS}}$=0 V)	1 µA (V_{DS}=max. rating, T=25ºC)	0.5 µA (V_{DS}=25 V, T=25ºC)

Table 2.10. 2N7002A and BS170F comparison.

$V(BR)_{DSS}$ *: Drain-Source Breakdown Voltage

- **NPN:** QBC817-40
- **PNP:** ZXTP2039
- **OPERATIONAL AMPLIFIER:**
  - MAX975
  - MAX4091
  - INA138
- **REGULATORS:**
  - LT1963_33

2.3.1.2– Models written by hand:

- **RESISTOR**

  .model RES1 R (R=1 DEV=1%)

  DEV, it is a parameter to model the tolerance of the resistor.

  Exists other parameters to characterize the resistors, for example the temperature coefficients, TC1, TC2, TCE…

- **CAPACITOR**

  .model CAP1 C (C=1 DEV=1%)

  Exists other parameters to characterize the capacitors, like the resistors.

- **INDUCTOR**

  .model IND1 L (L=1 DEV=1%)

  Exists other parameters to characterize the inductors, like the resistors and capacitors.

- **4-WIRE RESISTOR**

```
.subckt RES50M_4W    1  2  3   4
r1          1        2       50m
r2_null     1        3       0.00000001
r3_null     2        4       0.00000001
.ends RES50M_4W
```

  This is the subcircuit of a 4-wire resistor.

- **LED**

```
.subckt VLMB1300     1  2
d     1     3
v     3     2     2.7
.ends
```

  The subcircuit of a LED includes a diode and a voltage source. The value of the voltage source depends on the colour of the LED (at the example above, 2.7 V LED diode).

- **ZENER DIODE (18 VOLT)**

  This model was not write full by hand, just changed some parameters to create a Zener diode of 18 V, because on internet it was only the Zener diode model of 10 V, of this family of diodes.

  The parameters of original Zener diode are these:

```
IBVC    0    10     0.001
RBVC    10   0      10000
```

  We can calculate the Zener voltage:

$$V = IBVC \times RBVC = 10\,V$$

  For the 18 V Zener diode just we write:

```
IBVC    0    10     0.0018
RBVC    10   0      10000
```

Now:

$$V = IBVC \times RBVC = 18\,V$$

The graphs of both responses are the following:

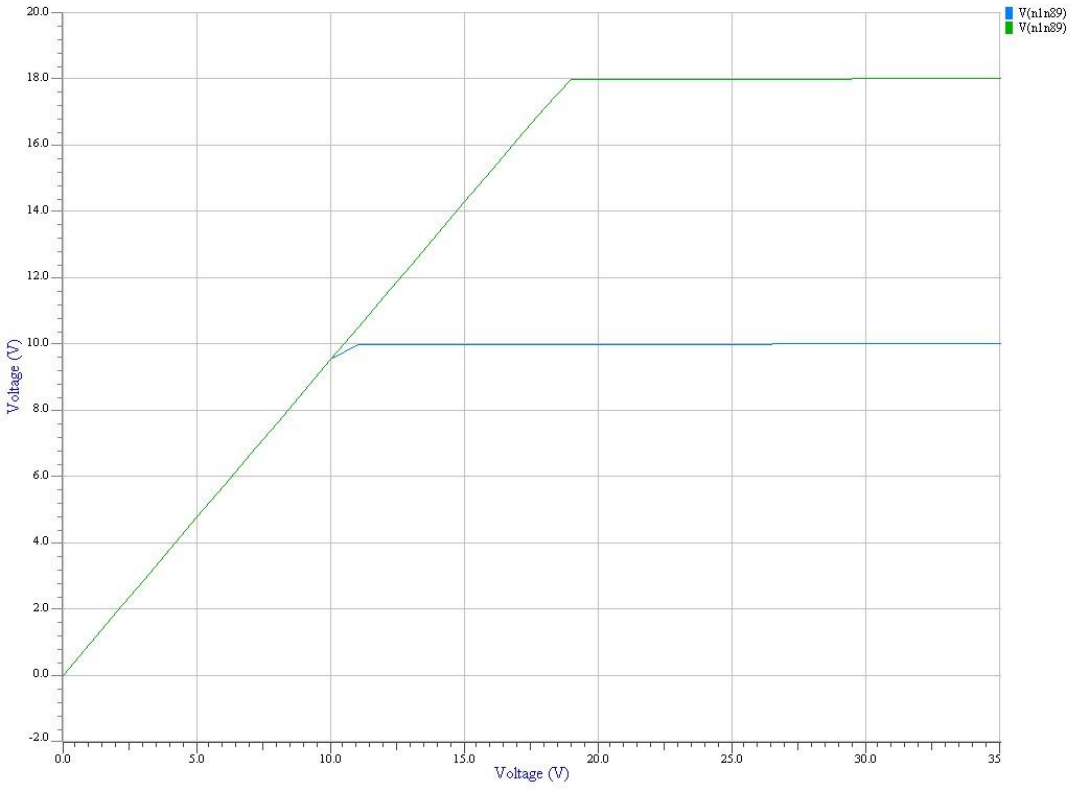


Figure 2.19.Zener 10V and Zener 18V responses.

The subcircuit is the following:

```
.subckt BZM55C18      1     9
df 1 9 dfmod
.model dfmod d n = 2 is = 1.9e-009 rs = 0.36459
+ eg = 1.11 xti = 3
+ cjo = 6.19198e-011 vj = 0.747672 m = 0.5 fc = 0.5
+ tt = 1e-008 tnom = 25
* leakage
rl 1 9 7.89474e+007 rlmod
.model rlmod r tc1 = 0 tc2 = 0 tnom = 25
* breakdown
es 9 90 10 20 1
dr1 90 31 drev1 temp = 25
.model drev1 d is = 1e-015 n = 0.108999 rs = 7.09165 tnom = 25
vr1 31 1 0.0998299
dr2 90 32 drev2 temp = 25
```

```
.model drev2 d is = 1e-015 n = 0.293481 rs = 4.11942 tnom = 25
vr2 32 1 0.000553349
vtrim 20 0 0.210825
ibvc 0 10 0.0018
rbvc 10 0 10000 rbvcmod
.model rbvcmod r tc1 = 0.0007 tnom = 25
.ends
```

- **OPERATIONAL AMPLIFIER**

  - **MYOPAMP**

```
.subckt MYOPAMP     in+   in-    vcc  vee   out
* input impedance
rin          in+        in-        1000meg
* dc gain=1meg and pole1=100hz
* unity gain = dcgain x pole1 = 100mhz
egain       3 vee    in+ in-   1meg
rp1          3          4          1g
cp1          4          vee       1.5915pf
* output buffer and resistance
ebuffer    5 vee    4 vee    1
rout         5          out       10
* voltage limiting
dp           4          105       dlim
evp     105   106   vcc   0  1
voff_vp  106   0    dc  -0.7v
*vp         vcc        105       dc         3.3v
dn           104       4          dlim
evn     104     107   vee   0   1
voff_vn 107     0    dc  0.7v
*vn         104       vee       dc         0v
.model    dlim      d(is=1e-15)
.ends
```

This is a operational amplifier subcircuit.

- **SOLAR CELL**

```
.SUBCKT SolarCell       1       4

IPH1     4       3      DC     0.42
D1         3      5      D1N4002
D2         5       6     D1N4002
D3         6      4      D1N4002
Rp         3      4      800
```

```
Rs      3    1    0.1

.MODEL D1N4002 D (IS=14.11E-9 N=1.984 RS=33.89E-3 IKF=94.81 XTI=3
+ EG=1.110 CJO=51.17E-12 M=.2762 VJ=.3905 FC=.5 ISR=100.0E-12
+ NR=2 BV=100.1 IBV=10 TT=4.761E-6)

.ENDS
```

This subcircuit corresponds with this circuit:

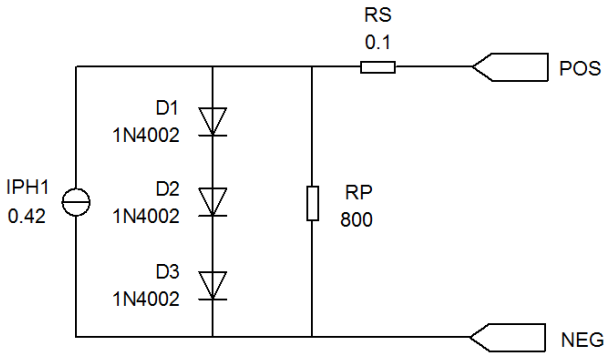


Figure 2.20. Solar Cell subcircuit.

The above circuit models a solar cell with 2.2 V and 0.4 A. Can see a deeper solar cell analysis at the next chapter.

- **REGULATORS**

  - **<u>LM2936_5V</u>**

    Due the fact that LM2936 is a linear regulator, this model has been done following this graph to model the linear output and the short-circuit current, in this case, equal to 250 mA.

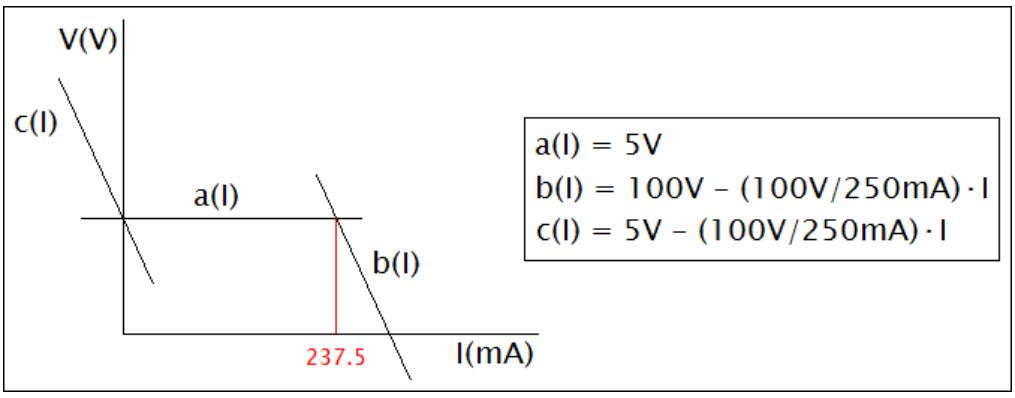


Figure 2.21. LM2936 behavior curves.

This graph is transcribed to the LM2936 model after do the following study to achieve the expected result:

From now, *'a(I)'* will be write as *'a'*, to simplify writing.

The expresion which follows the expected graph is:

$$\max(c, \min(a, b)); \text{ where:}$$

$$\min(a, b) = \frac{1}{2} \times (a + b - |a - b|)$$

$$\max(c, d) = \frac{1}{2} \times (c + d + |c - d|)$$

The absolute value could be:

$$|a - b| = \begin{cases} a - b & \rightarrow \ a > b \\ b - a & \rightarrow \ a < b \end{cases}$$

So, for the $\min(a, b)$, if:

$$a < b \ \rightarrow \ \frac{1}{2} \times \big(a + b - (b - a)\big) = \frac{1}{2} \times 2 \times a = a$$

$$a > b \ \rightarrow \ \frac{1}{2} \times \big(a + b - (a - b)\big) = \frac{1}{2} \times 2 \times b = b$$

And, for the $\max(c, d)$, if:

$$c < d \ \rightarrow \ \frac{1}{2} \times \big(c + d + (d - c)\big) = \frac{1}{2} \times 2 \times d = d$$

$$c > d \ \rightarrow \ \frac{1}{2} \times \big(c + d + (c - d)\big) = \frac{1}{2} \times 2 \times c = c$$

To resume:

$$\begin{cases} a & \rightarrow \ a < b \\ b & \rightarrow \ a > b \\ c & \rightarrow \ c > d \\ d & \rightarrow \ c < d \end{cases}$$

Finally, for $\max(c, \min(a, b))$:

$$\frac{1}{2} \times \left(c + \frac{1}{2} \times (a + b - |a - b|) + \left|c - \frac{1}{2} \times (a + b - |a - b|)\right|\right)$$

In our model, this is achieved with a non linear voltage source:

```
bdc     5 4 v=0.5*(
+ (0.5* (5+(100-100/250m*i(vdc)) - abs(5-(100-100/250m*i(vdc)))) ) + (5-100/250m*i(vdc)) +
```

+ abs((0.5*(5+(100-100/250m*i(vdc))-abs(5-(100-100/250m*i(vdc)))))-(5-100/250m*i(vdc))))

The following, is the circuit diagram handwritten at the model:

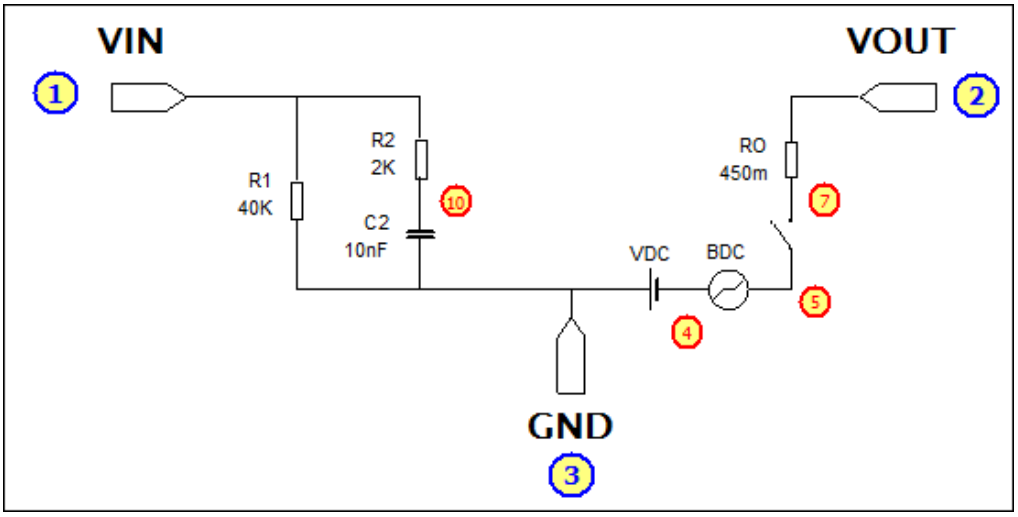


Figure 2.22. LM2936 subcircuit.

At this model, also it is took in account the input current, the output voltage peaks due the switching, deleted by a input filter, the load regulation, shaped with a output resistor of 450 mΩ, obtained of the datasheet, and the dropout voltage, 200 mV, modeled with a switch.

The voltage source VDC = 0 V, is needed because it is useful to know the current across of this line, required for the non linear source. VDC source does not have another purpose.

The maximum and minimum voltage input values are not limited at this model and the line regulation is not modeled.

The following is the handwritten model:

```
.subckt lm2936_5V     1 2 3
**********************************************************************
*Vin    1
*Vout   2
*GND    3
**********************************************************************
*model done by eduardo molla
*this subckt does not take care some datasheet params.:
*-line regulation (30mv)
*-max and min input limited values (4v to 40v)
**********************************************************************

*r1, for achieve the datasheet input current
```

```
r1      1 3 40k
*r2, c2 filter to model the delay and eliminate the output voltage peaks when the
*switch closes
r2  1 10 2k
c2  10 3 10n

*vdc 0v
vdc     3 4 dc 0

*bdc, non linear dependent source, to achieve the max short circuit current 250 ma
bdc     5 4 v=0.5*(
+       (0.5* (5+(100-100/250m*i(vdc)) - abs(5-(100-100/250m*i(vdc)))) ) + (5-100/250m*i(vdc)) +
+ abs(  (0.5* (5+(100-100/250m*i(vdc)) - abs(5-(100-100/250m*i(vdc)))) ) - (5-100/250m*i(vdc)) ) )

*s1, switch
s1  5 7 10 3 smod

*ro, to model the load regulation
ro 7 2 450m

*smod, switch model vt=5.2, the 0.2v is the dropout
.model smod  sw (ron=0  roff=1.0e8  vt=5.2v   vh=5v)


.ends
```

- **LM4128_3V**

The LM4128 is also a linear regulator, so its model has been done by following the same graph of LM2936 regulator with other values for the linear output and the short-circuit current, in this case equal to 75 mA.

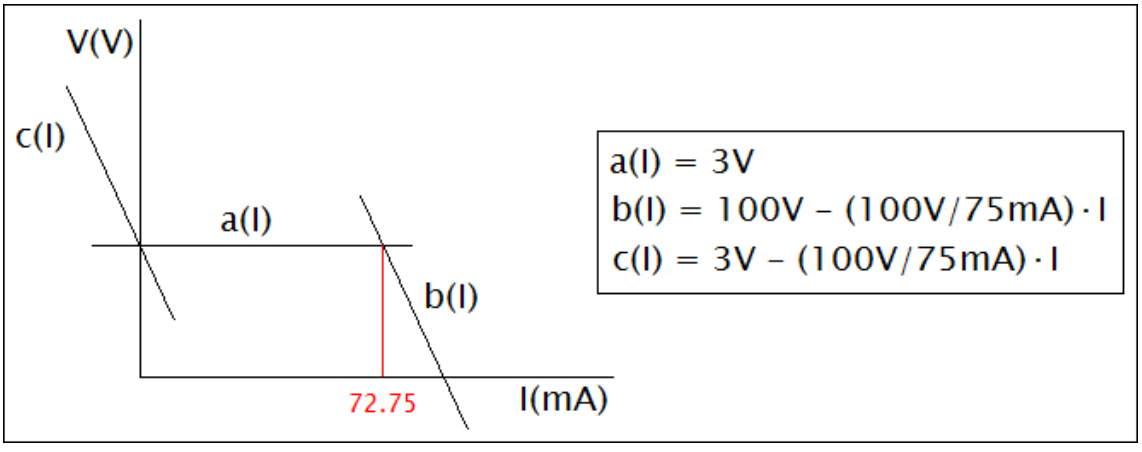


Figure 2.23. LM4128 behavior curves.

The method used to reach the: $\max(c, \min(a, b))$ expression is the same of LM2936, just changing the output voltage and short-circuit current values.

The following, is the circuit diagram handwritten at the model:

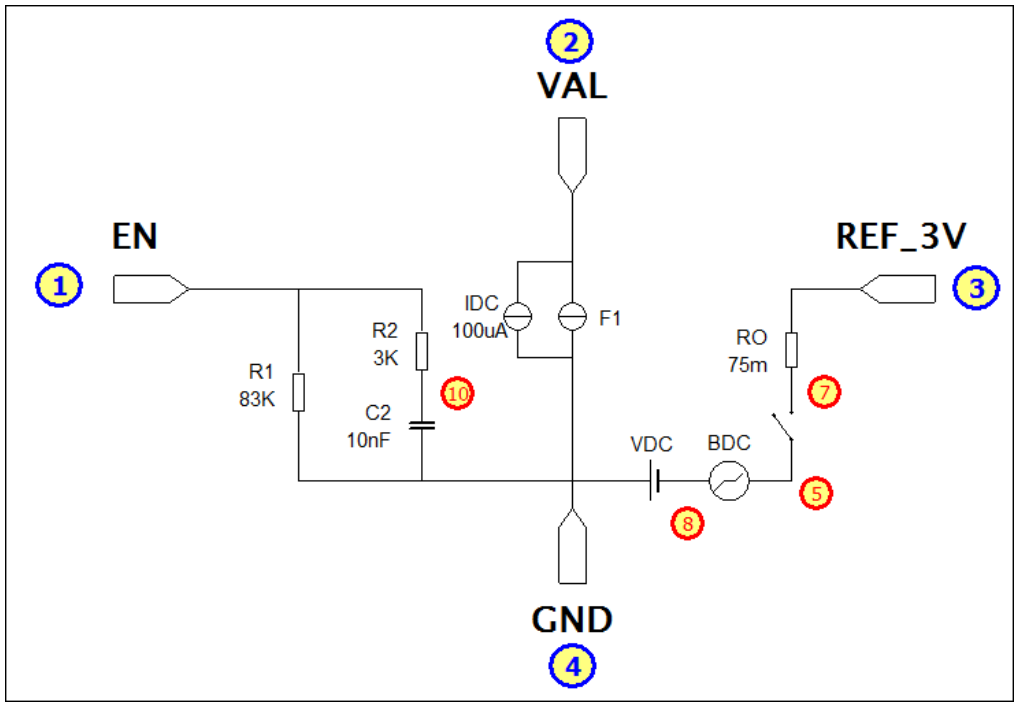


Figure 2.24. LM4128 subcircuit.

At this model, also it is took in account the input current, 60 µA for 5 V (at our project it is used as regulator of 5 V input voltage), the output voltage peaks due the switching, deleted by a input filter, the load regulation, shaped with a output resistor of 75 mΩ, obtained of the datasheet as $25ppm/mA \times 3V = \frac{75\mu V}{mA} = 75m\Omega$, and the enable function, modeled with a switch.

The voltage source VDC = 0 V, is needed because it is useful to know the current across of this line, required for the non linear source. Also it is used by the current controlled current supply. VDC source does not have another purpose.

IDC and F1 are DC current source and current controlled current source, respectively, they are needed to model the worst-case no load supply current.

The maximum and minimum voltage input values are not limited at this model, the line regulation and the dropout voltage are not modeled.

The following is the handwritten model:

```
.SUBCKT LM4128_3V     1 2 3 4
**********************************************************************
*EN     1
*VIN    2
*VREF   3
*GND    4
**********************************************************************
```

```
*MODEL DONE BY EDUARDO MOLLA
*THIS SUBCKT DOES NOT TAKE CARE SOME DATASHEET PARAMS.:
*-LINE REGULATION
*-DROPOUT VOLTAGE
*-MAX AND MIN INPUT LIMITED VALUES (-0.3V TO 6V)
**********************************************************************

*R1, FOR ACHIEVE THE DATASHEET ENABLE CURRENT INPUT: 60uA FOR 5V
R1      1 4 83K

*R2, C2 FILTER TO MODEL THE DELAY AND ELIMINATE THE OUTPUT VOLTAGE PEAKS
*WHEN THE SWITCH CLOSES
R2  1 10 4K
C2  10 4 10N

*Idc 1OOu, WORST CASE NO LOAD SUPPLY CURRENT
Idc     2 4 DC 100u

*Vdc 0V, IT IS NEEDED FOR THE F1
Vdc     4 8 DC 0

*Bdc, NON LINEAR DEPENDENT SOURCE, TO ACHIEVE THE MAX SHORT CIRCUIT
*CURRENT 75 mA
Bdc     5 8 V=0.5*(
+       (0.5* (3+(100-100/75M*I(Vdc)) - abs(3-(100-100/75M*I(Vdc)))) ) + (3-100/75M*I(Vdc)) +
+ abs(  (0.5* (3+(100-100/75M*I(Vdc)) - abs(3-(100-100/75M*I(Vdc)))) ) - (3-100/75M*I(Vdc)) ) )

*F1, CURRENT CONTROLLED CURRENT SOURCE
F1      2  4   Vdc     1.0

*S1, SWITCH
S1  5 7 10 4 SMOD

*RO, TO MODEL THE LOAD REGULATION
RO 7 3 75M

*SMOD, SWITCH MODEL, CLOSED FOR 65% VOLTAGE OF ENABLE INPUT VOLT. (OUR
*CASE 5V): AND OPENED FOR 35% OF 5V

.MODEL SMOD  SW (RON=0  ROFF=1.0E8  VT=3.25V   VH=1.75V)


.ENDS
```

- **TPS5450**

  This is the functional block diagram found at the datasheet of the regulator TPS5450 [7].

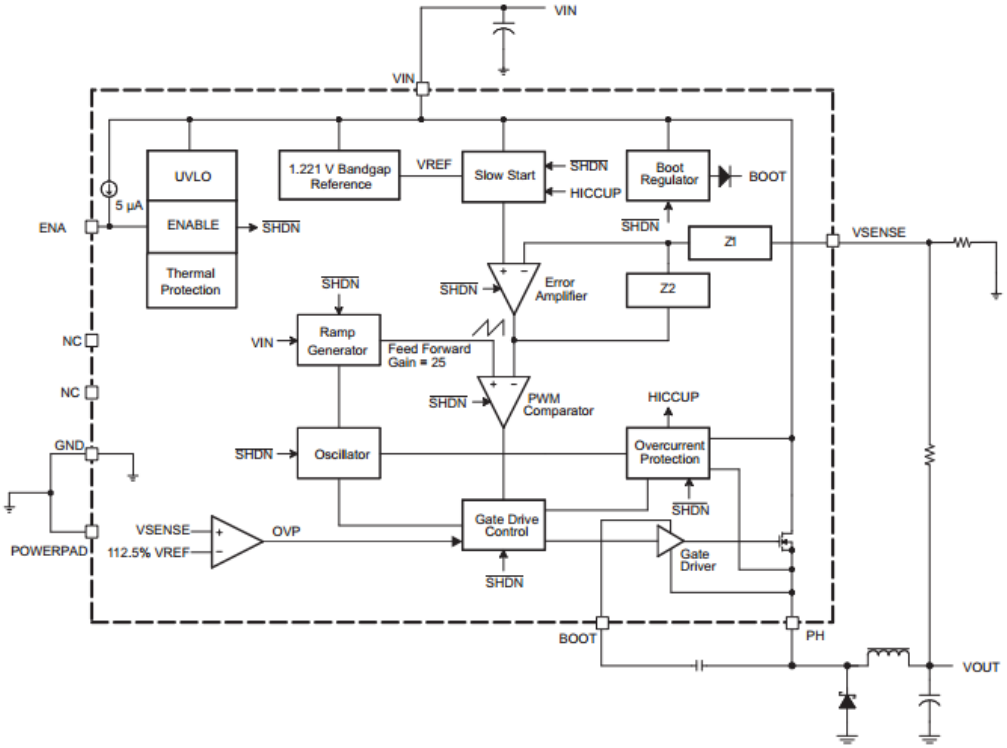


Figure 2.25. TPS5450 block diagram.

Because there is not the subcircuit of this regulator on internet, it is created by hand, simplifying the above circuit.

The following, is the simplified circuit diagram handwritten at the model.

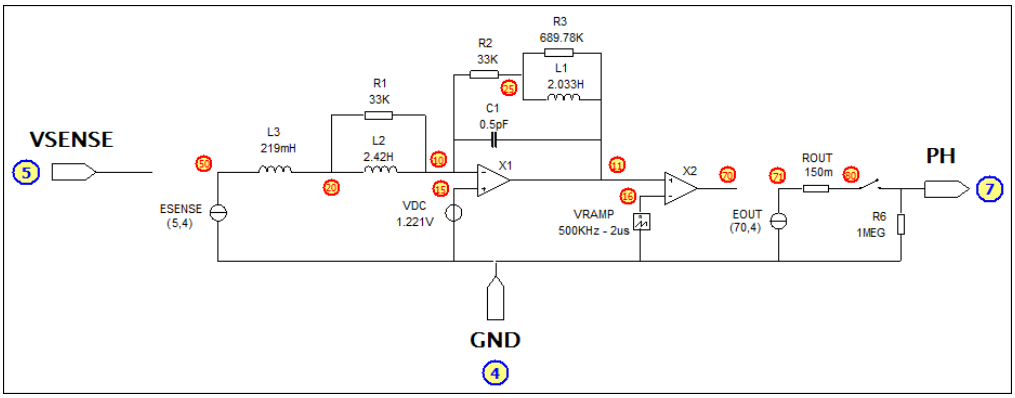


Figure 2.26. TPS5450 subcircuit.

With the aim to understand better the subcircuit, the whole system will be explained section by section. For our simplification it has been taken into account the Z1, Z2, VREF 1.221V, OA Error Amplifier, OA PWM Comparator and Ramp Generator of 500kHz blocks.

- **Z1 and Z2**

These blocks correspond with the internal compensation of the TPS5450. Taking the poles and zeros frequencies of the datasheet and these two configurations for the Z1 and Z2 blocks, the values for the several components are calculated.

Poles and zeros:

- Fp0 = 2165 Hz, Fz1 = 2170 Hz, Fz2 = 2590 Hz
- Fp1 = 24 kHz, Fp2 = 54 kHz, Fp3 = 440 kHz

Z1 and Z2 configurations:

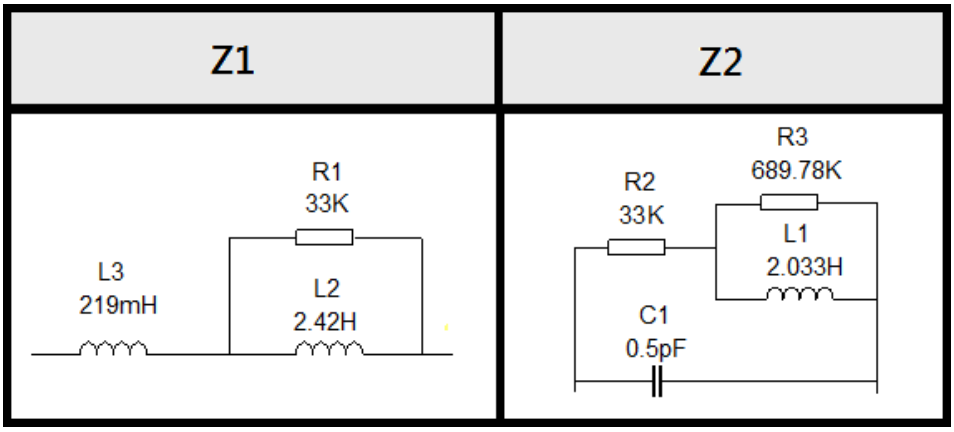


Figure 2.27. Z1 and Z2 configurations.

And the values have been calculated by this way (taking R1 as a prefixed value):

$R1 = 33\ k\Omega$

$$fz1 = \frac{R1}{2\pi \cdot L2} \rightarrow L2 = \frac{R1}{2\pi \cdot fz1} = 2.42\ H$$

$$fp1 = \frac{R1}{2\pi \cdot L3} \rightarrow L3 = \frac{R1}{2\pi \cdot fp1} = 0.219\ H$$

$$fp0 = \frac{R2}{2\pi \cdot L2} \rightarrow R2 = 2\pi \cdot fp0 \cdot L2 \cong 33\ k\Omega$$

$$fz2 = \frac{R2}{2\pi \cdot L1} \rightarrow L1 = \frac{R2}{2\pi \cdot fz2} = 2.033\ H$$

$$fp2 = \frac{R3}{2\pi \cdot L1} \rightarrow R3 = 2\pi \cdot fp2 \cdot L1 = 698.78\ k\Omega$$

$$fp3 = \frac{1}{2\pi \cdot C3 \cdot (R2 + R3)} \rightarrow C3 = \frac{1}{2\pi \cdot (R2 + R3) \cdot fp3} = 0.5\ pF$$

The values of inductors are high, but it is a model, not a real circuit, so are valid.

- **OA Error Amplifier, OA PWM Comparator**

  The OA Error Amplifier has as inputs the VREF = 1.221 V and the signal at node 10.
  The OA PWM comparator has as inputs the VRAMP of 500 kHz and the output of OA Error Amplifier.

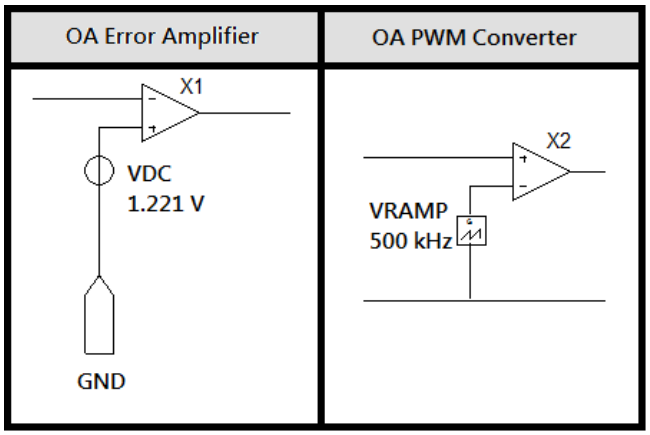


Figure 2.28. OA Error Amplifier and OA PWM Converter configurations.

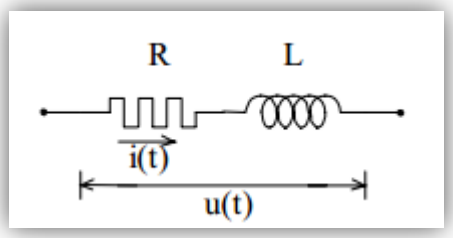
The following is the subcircuit of TPS5450. The ESENSE and EOUT are two voltage-controlled voltage sources for isolate the currents. R1G is a resistor to achieve the enable current input, and R2G and C2G are components used as a filter. The last section to expose before show the subcircuit, is the switch S1, to model the enable function, when the signal is below 0.5 V the device stops switching.

```
.SUBCKT TPS5450     1 2 3 4 5 6 7
**********************************************************************
*Vin        1
*ENA        2
*PowerPAD   3
*GND        4
*Vsense     5
*Boot       6
*PH         7
**********************************************************************
*MODEL DONE BY EDUARDO MOLLA
**********************************************************************
*R1G, FOR ACHIEVE THE DATASHEET ENABLE CURRENT INPUT: 60uA FOR 5V
R1G      2 4 83K
*R2G, C2G FILTER TO MODEL THE DELAY AND ELIMINATE THE OUTPUT VOLTAGE
*PEAKS WHEN THE SWITCH CLOSES
R2G  2 40 4K
C2G  40 4 10N
**********************
```

```
*Z1
**********
ESENSE 50 4 5 4 1.0
L3 50 20 0.219
R1 20 10 33K
L2 20 10 2.42
**********
*Z2
**********
R2 10 25 33K
R3 25 11 689.78K
L1 25 11 2.033
C3 10 11 0.5P
**********
Vdc 15 4 DC 1.221
Vramp 16 4 DC 0 PULSE (5 0 1N 0.999U 0.999U 1N 2.0U)
**********
X1 15 10 VCC 4 11 MYOPAMP
X2 11 16 VCC 4 70 MYOPAMP
EOUT 71 4 70 4 1.0
ROUT 71 80 150m
**********
*VDC10, to supply with 10 V the OA
**********
VDC10 VCC 4 DC 10

R6  7 4 1MEG

*S1, SWITCH
S1  80 7 40 4 SMOD1

.MODEL SMOD1  SW (RON=0  ROFF=1.0E8  VT=1.3V   VH=0.5V)

.ENDS
```

2.3.2 – Problem 2: real inductor model

Due that the real inductor is not only a ideal inductor [12], it has been created a subcircuit composed by a inductor and a series resistor, because this resistor could carry some disturbances at the entire behavior of the circuit. The voltage $u(t)$ drops at the ohmic drop $R \cdot i(t)$ and at the reactive drop $L\frac{di(t)}{dt}$.



$$u(t) = R \cdot i(t) + L\frac{di(t)}{dt}$$

Figure 2.29.Real inductor subcircuit and voltage equation.

This is the subcircuit:

```
.SUBCKT REAL_INDUCTOR     1   2
L1 1 3 33U
R1 3 2 87.5M
.ENDS
```

2.3.3 – Problem 3: set Mentor Graphics component properties

Using the Mentor Graphics software, it has been needed to set several properties to get the necessary Netlist of the circuits and the subsequent simulation.

On the one hand, for the resistances and capacitors, it was set the VALUE, MODEL and ORDER properties. Some of these components, had repeated the VALUE property, and was necessary to cancel one of them. At the ORDER property, was wrote VALUE$ MODEL$, to make visible these properties at the Netlist and that the software may understand correctly all the features in order to perform the simulations.

On the other hand, the rest of components like diodes, that use pspice models or operational amplifiers, regulators or another kind of components that require a subcircuit, have been set the above properties by different way, now the VALUE and ORDER gaps must be empty (or ORDER can be fill with the MODEL$ feature), because the value of the several items are defined inside of the subcircuit.

To know the syntax used at models, I did that table:

MODEL NAME	COMPONENT	COMPONENT PREFIX
R	Resistor	R
C	Capacitor	C
L	Inductor	L
D	Diode	D
NPN	npn Bipolar Junction Transistor	Q
PNP	pnp Bipolar Junction Transistor	Q
NMOS	n-Channel MOSFET	M
PMOS	p-Channel MOSFET	M
-	Subcircuit	X

Table 2.11. Pspice syntax.

The subcircuits have to named starting by X. Throughout this chapter we have seen some subcircuit examples.

2.3.3.1 – MEG problem

To set features of components, as the value or simulation model for resistors, capacitors, inductors… It is more convenient write these characteristics at Part Editor of such component. In some cases was included some feature at Symbol Editor because this was common to all parts referenced to it.

Another problem was that some resistor had a Megohm value, but the Part Editor of the resistors does not accept the 'MEG' keyword for these kind of resistors. And the Part Editor only accepted the 'M' keyword. The problem when doing the Netlist was that a 'M' at Value Property, the software takes a milliohm value. The solution was keep empty the gap property at the Part Editor for these resistors and introduce the MEG values by hand at Mentor Graphics program.

The following are the Spice accepted suffixes:

SPICE SUFFIX	UNIT	MULTIPLIER
F	femto	10^{-15}
P	pico	10^{-12}
N	nano	10^{-9}
U	micro	10^{-6}
M	milli	10^{-3}
K	kilo	10^{3}
MEG	mega	10^{6}
G	giga	10^{9}
T	tera	10^{12}

Figure 2.30. Spice suffixes.

When it is done some change of some component could happen two things. If the change was done at Symbol Editor, to update this change, it is needed to click *Update Libraries* at *Tools* menu, and after, press right button of the mouse at component to update and press *Update Symbol*. If the change was done at Part Editor did not works the previous way, it is needed to delete the old component and replace the same of the Library, after to *Update Libraries*.

2.3.3.2 – Several problems

- The Test Probes (TP), gave problems at the simulations, the solution was change the model of them for resistors of 1 Ω.
- Pay attention to the name of the components, because it is important the first letter, depending of the component it is different, could be a cause of a problem at simulations.
- Inside of the Reusable Block, the wires must have the same name of the PINs.

- The nets of the subcircuit of a component and the schematic nets must keep a relationship. Because it is possible have a subcircuit but set the inputs/outputs with a wrong order, and it will not work correctly.

- The name of the subcircuits cannot start by a number. So, it was renaming the Reusable Blocks starting by Bk.

- The grounds of the Reusable Blocks was renamed as DGND and AGND, depending if these were digital ground or analog ground, respectively. At circuit which uses Reusable Blocks, the DGND is connected to global GND and the AGND to global AGND. If it is named some ground as GND at a Reusable Block, it will give problems at future simulations.

2.3.3.3 – Switches

Another element used at regulators are the switches, and these gave us problems. For a correct work this must be called like:

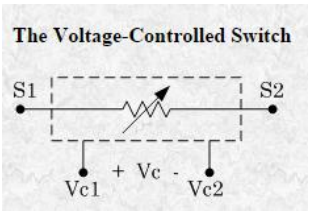


Figure 2.31. Switch circuit.

Where the name of the voltage-controlled switch must begin with the letter S. The following two names/numbers are the physical nodes (S1, S2), and the last two names/numbers are the two nodes across which the controlling voltage, Vc, is applied (Vc1, Vc2). The last item in the list is the model name. It is needed a .MODEL statement for the device. There are only four parameters: *Ron*, the resistance of the switch when it is on; *Roff*, the resistance of the switch when it is off; *VT*, the threshhold voltage for turning the switch on; and *VH*, the threshhold voltage for turning the switch off.

```
S1  5  7  10  4  SMOD
.MODEL SMOD  SW (RON=0  ROFF=1.0E8  VT=3.25V   VH=1.75V)
```

In this example, the switch is connected between nodes 5 and 7. The voltage between nodes 10 and 4 is used to control the switch. When this control voltage is 3.25V (*Von*) or greater, the switch resistance is 0 Ω (*Ron*). When the control voltage is 1.75 (*Voff*) or less, the switch resistance is 1.0E8 Ω (*Roff*). The resistance varies linearly with the control voltage when the voltage is between *Von* and *Voff*. *SW* is the model type for a voltage-controlled switch while *SMOD* is the model name assigned by the user. You can change any of the model parameters.

To conclude this section, I am going to comment the dependent and independent sources. These were studied and configured along of the thesis.

2.3.3.4 – Independent sources

- **Voltage source**:

Name	*Node +*	*Node-*	*(Optional)*	*Value*
V1	*1*	*2*	*DC*	*10V*

- **Current source**, the same structure, but the name starts with the letter I.
- **Pulse source**:

Name	*N+*	*N-*	*Type*	*V1*	*V2*	*Td*	*Tr*	*Tf*	*Pw*	*Per.*
Vs	*1*	*0*	*PULSE*	*(0V*	*3.3V*	*0s*	*100ns*	*100ns*	*2us*	*20us)*

The parameters for the pulse (to be entered in the order given) are [13]:

- $\mathbf{V_1}$ is the value when the pulse is not "on." This can be zero or negative as required. For a pulsed current source, the units would be "amps" instead of "volts."
- $\mathbf{V_2}$ is the value when the pulse is fully turned on. This can also be zero or negative. (Obviously, V_1 and V_2 should not be equal.) Again, the units would be "amps" if this were a current pulse.
- $\mathbf{T_d}$ is the time delay. The default units are seconds. The time delay may be zero, but not negative.
- $\mathbf{T_r}$ is the rise time of the pulse. PSpice allows this value to be zero, but zero rise time may cause convergence problems in some transient analysis simulations; i.e., there is a very good reason for the existence of this parameter. The default units are seconds.
- $\mathbf{T_f}$ is the fall time in seconds of the pulse. Zero value is not recommended to use.
- $\mathbf{P_w}$ is the pulse width. This is the time in seconds that the pulse is fully on.
- **Period** is the total time in seconds of the pulse. Be aware that the pulse repeats if the simulation time exceeds the period.

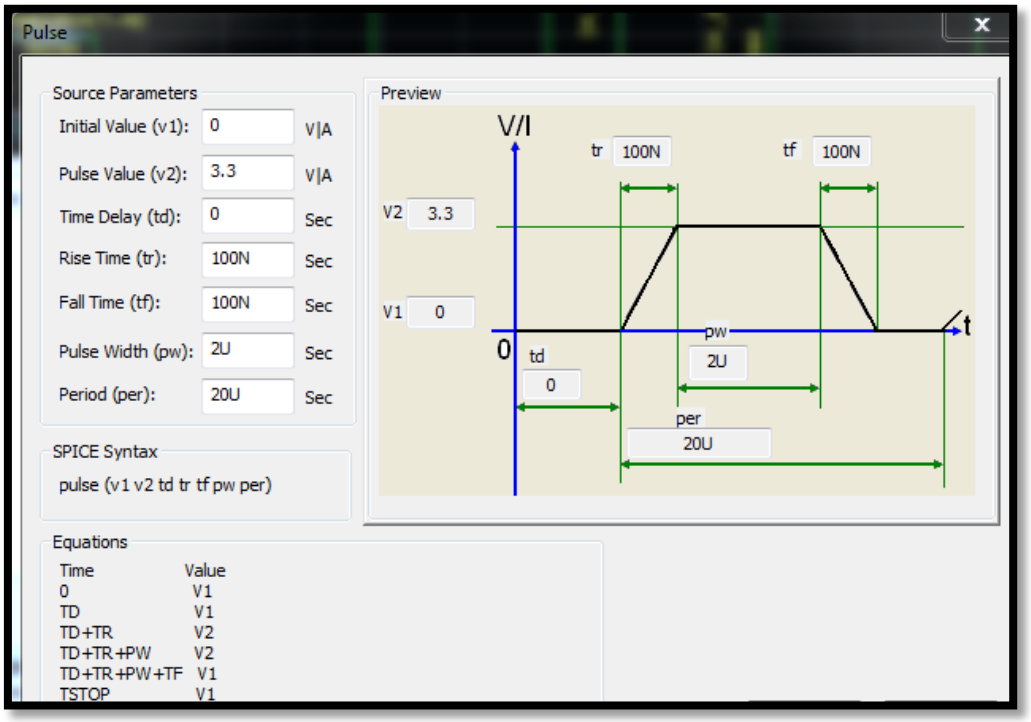


Figure 2.32. Simulation sources.

To create a **triangular source**, just it is necessary take a *Tr* and *Tf* appropriate values to achieve that *Tr + Tf = Period.*

It is possible set more kinds of independent sources, but I am not going to expose more types because is not the main goal at my thesis, and these three are the independent sources that I performed.

2.3.3.5 – Dependent sources

- **Exxx : Voltage-controlled voltage source (VCVS)**

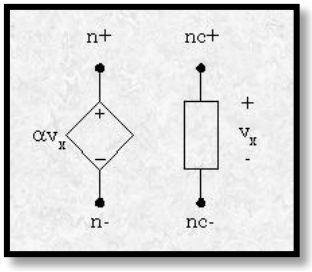


Figure 2.33. Voltage-controlled Voltage source.

In the above figure, [14] we find the dependent source whose positive terminal is designated as "n+" and whose negative terminal is designated as "n-." The controlling voltage is a branch voltage at some other circuit location. In this case, the positive terminal of the controlling branch is designated as "nc+" while the negative terminal is designated as "nc-" The "gain" of the dependent voltage source is a, a dimensionless quantity. For example, if v_x happened to be 16.0 V while a = 4, then node "n+" would be at 64.0 V higher potential than node "n-."
The first letter of the part name for the voltage-controlled dependent voltage source is "E". This is the letter that must appear in column 1 of the *.CIR file describing the circuit. A example of the voltage-controlled dependent voltage source PSpice entries follow.

Name	*n+*	*n-*	*nc+*	*nc-*	*gain*
Ebar	17	8	42	18	24.0

- **Fxxx: Current-controlled current source (CCCS)**

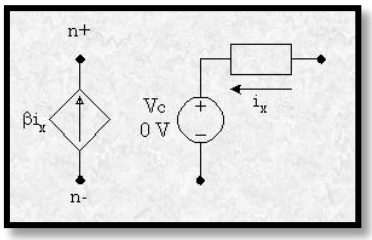


Figure 2.34. Current-controlled Current source.

The current-controlled dependent current source produces a current proportional to the controlling current, i_x, flowing in a different branch. The current gain, β, is dimensionless. Designating the control scheme is similar to setting up the current-controlled dependent voltage source. We must use a voltage source connected in series with the controlling element so that the controlling current enters the positive terminal of the independent voltage source used as an ammeter. If no voltage source is needed for its voltage, we use a zero-valued voltage source as shown in the figure.

The first letter in the part name for this dependent source is "F." The syntax for entering this part in *.CIR files is shown in several examples below.

Name	*n-*	*n+*	*Vmonitor*	*Gain*
Ftrn	81	19	Vctl	50.0
Vclt	23	12	DC	0V ; controls Ftrn

• **Gxxx: Voltage-controlled current source (VCCS)**

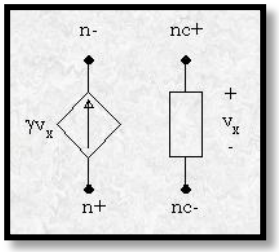


Figure 2.35. Voltage-controlled current source.

In the above voltage-controlled dependent current source a current equal to g times v_x flows from node "n+" through the source and out node "n-". γ is called the transconductance and has the dimensions of siemens (inverse ohms). For example, if the controlling branch voltage, v_x , equals 6.0 V and the transconductance, γ, is 0.25 siemens, the current produced by the dependent source is 1.5 amps.

The first letter of the part name for the voltage-controlled dependent current source is "G." Some examples of how this part is coded into the *.CIR file are shown below.

Name	*n+*	*n-*	*NC+*	*NC-*	*transconductance*
Glab	*23*	*17*	*8*	*3*	*2.5*

• Hxxx: Current-controlled voltage source (CCVS)

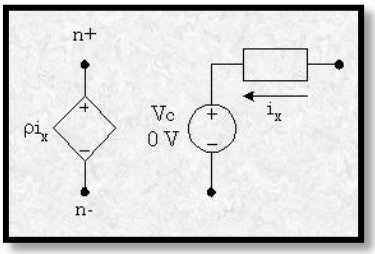


Figure 2.36. Current-controlled Voltage source.

The current-controlled dependent voltage source as shown above, produces a voltage proportional to the current, i_x, in a different branch of the network. The transresistance, ρ, in ohms is multiplied by i_x in amps to produce the dependent source voltage in volts. Unlike VCVS and VCCS, we cannot simply designate the controlling branch by its nodes. Since there could be multiple branches carrying very different currents between any pair of nodes, we must explicitly identify the branch of the controlling current. Eventually, we will be able to do this with any type of element. However, the only reliable method of doing this at present is to use an independent voltage source as an ammeter to report the current of the controlling branch to the dependent source. Usually, this means you must insert a zero-valued independent voltage source in series

with the branch containing the controlling current so that the controlling current enters the positive terminal of the independent voltage source. However, if there happens to be an independent voltage source that monitors the controlling current you can use it. If necessary, use a minus sign to get the right polarity.
The first letter of the part name for the current-controlled dependent voltage source is "H." Some examples follow for this device.

Name n+ n- Vmonitor transresistance
Hvx 20 12 Vhx 50.0
Vhx 80 76 DC 0V ; controls Hvx

2.4 – Final schematic

2.4.1 – Change 1: MPPT modification

One change of the Power Management Honeycomb was the MPPT block. This block originally was composed of three individual schematics, the following:

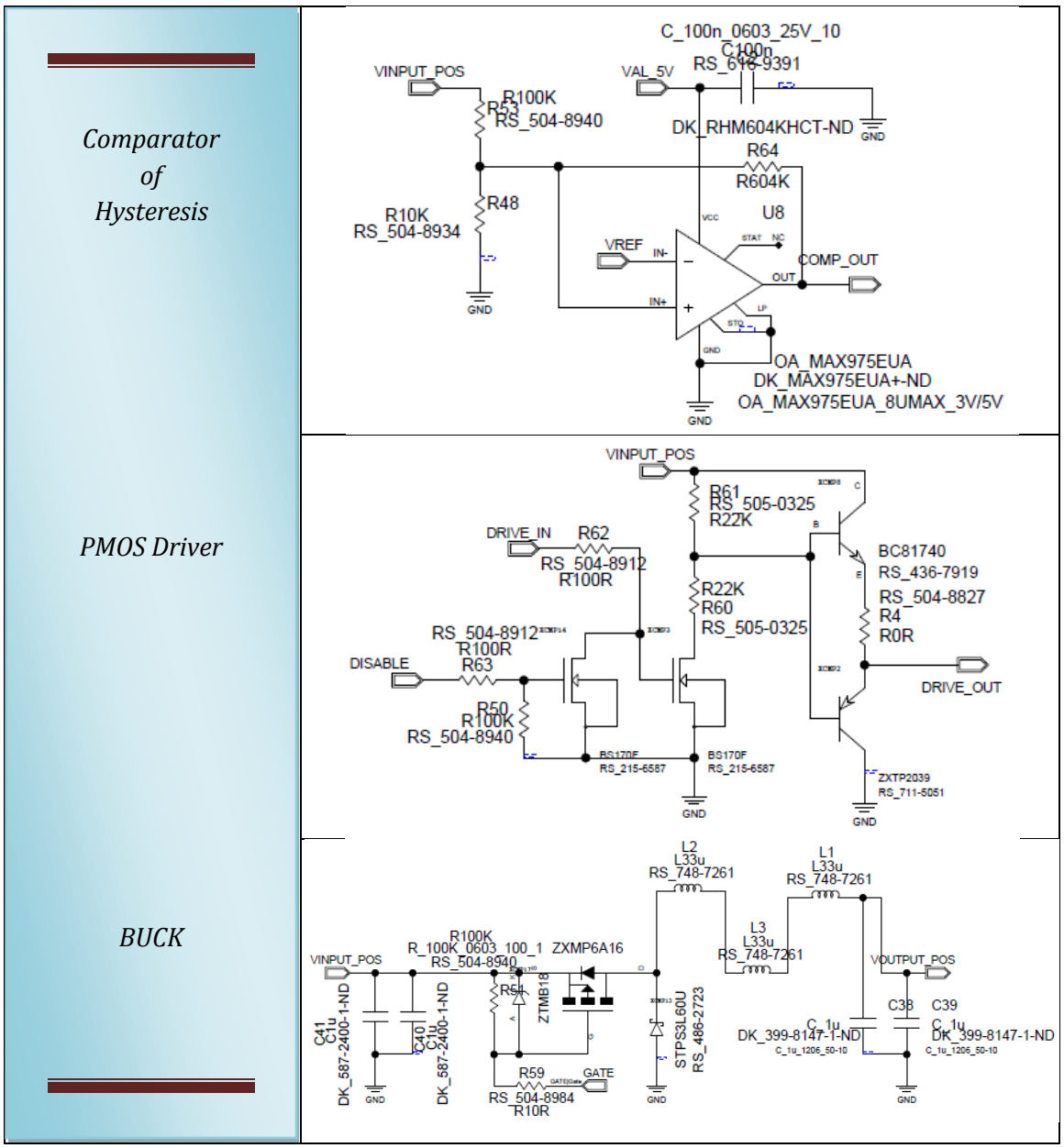


Figure 2.37. Comparator of Hysteresis, PMOS Driver and Buck schematics.

It is considered that these three blocks and the regulator, to supply 5 V to the operational amplifier MAX975, should be at the same MPPT schematic for doing a Reusable Block of it, as is shown below:

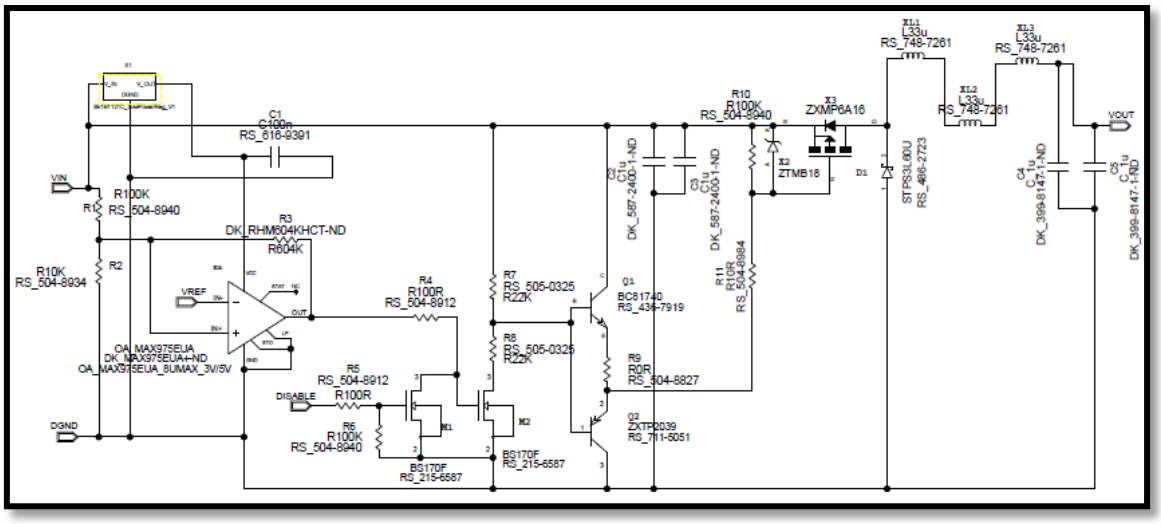


Figure 2.38. MPPT final schematic.

2.4.2 – Change 2: reusable block

At this point, the professor suggest me and the other colleagues to change the current blocks at Aramis schematics to Reusable Blocks, with the goal to can reuse the blocks created by different people for any person who needs such block. Otherwise, a physical difference between the previous blocks and the Reusable Blocks is that the previous blocks had the GND inside of them, and at the Reusable Blocks all the inputs and outputs are pins, also the GND. Both blocks are shown below:

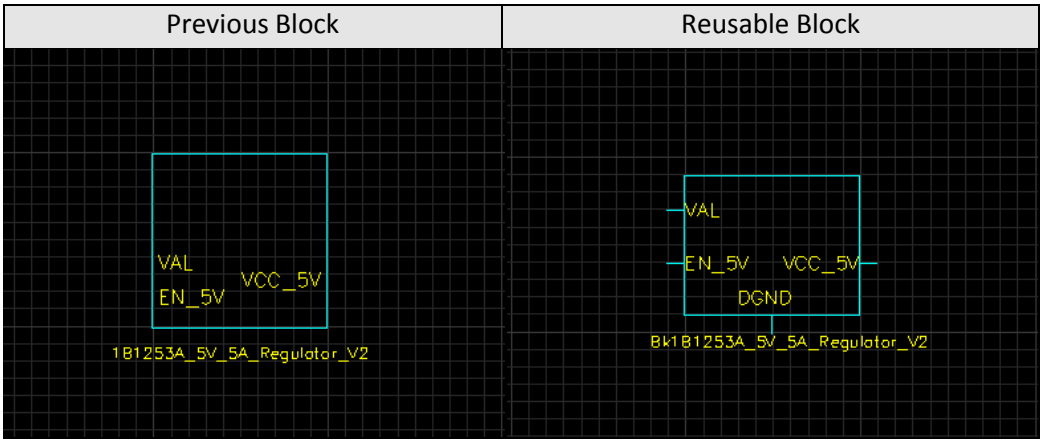


Figure 2.39. Previous and Reusable blocks.

2.5 – Future improvements

With the aim to improve the efficiency of the MPPT block are done some tests. To understand better the system it was created a local project with the solar cells connected to the appropriate inputs as is shown below.

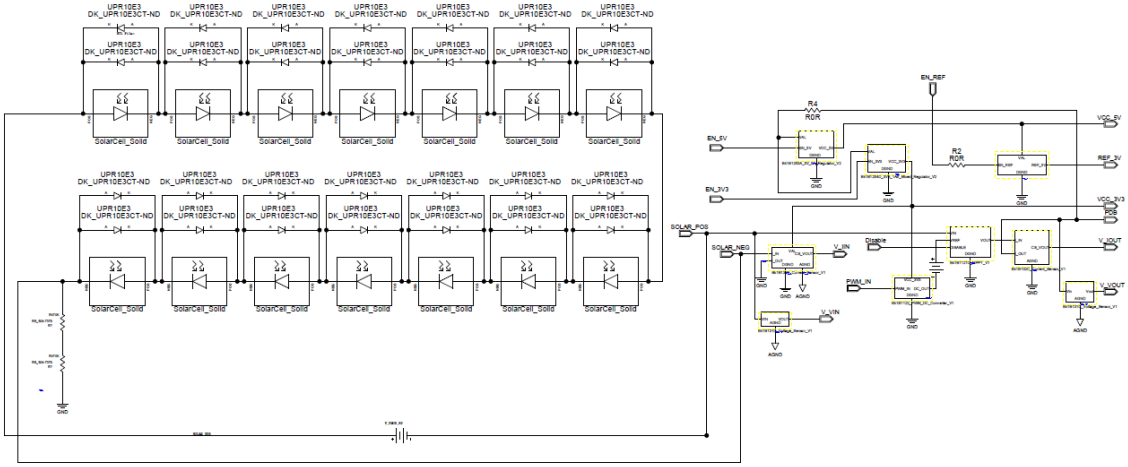


Figure 2.40. MPPT with solar cells local schematic.

And doing a zoom:

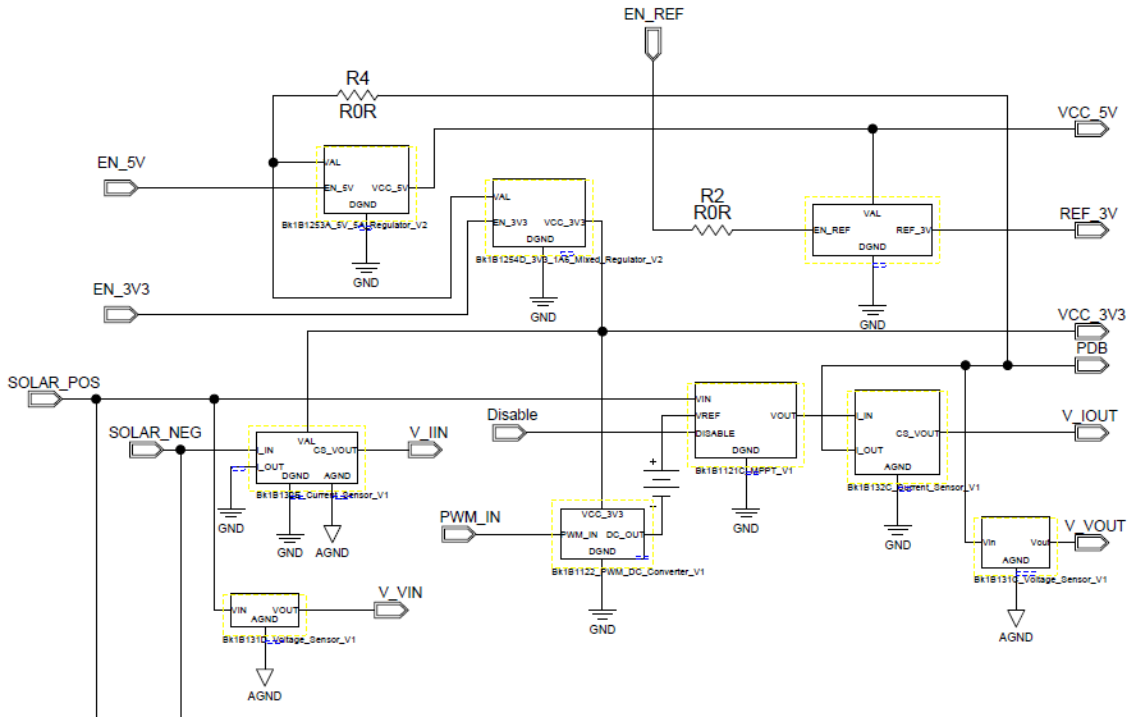


Figure 2.41. MPPT zoom at local schematic.

This is a local project, created doing some modifications regard to the original one. At the project there are two jumpers to choose between two possible different inputs, at our local version was chosen R4 and R2 to enable the VAL of 5 V and 3.3 V regulator inputs through PDB and EN_REF 3.0 V input through EN_REF pin, respectively.

The following inputs were set to carry out the simulations:

PWM_IN → Square wave of 50 kHz frequency, so period equal to 20 µs. Voltage initial value: 0 V and voltage pulse value: 3.3 V. Time delay: 0 s, rise time: 100 µs, fall time: 100 µs.

EN_5V → DC voltage of 5 V.

EN_3V3 → DC voltage of 3.3 V.

DISABLE → DC voltage of 0 V.

EN_REF → Was set as square wave, but it did not matter to this study. Period: 1 ms, voltage initial value: 0 V and voltage pulse value: 5 V, time delay: 0 s, rise time: 100 µs, fall time: 100 µs. Duty cycle: 50%.

To start trying to improve the MPPT efficiency, it is possible change the duty cycle (D.C.) of the PWM_IN input. To observe the wave results and compare all of them, it is needed to connect a small load between the PDB output and the ground, and letting the rest of outputs without connected load. After having done several simulations with different values for the PDB load, it is chosen a 10 Ω.

The first simulations were so much slow. With the objective to perform them quicker, it was changed the value of the capacitor C3 of the PWM_DC_Converter, the original value was 0.47 µF and the value used at our simulations come 0.047 µF. From the Probe_PSB_76 to Probe_PSB_84 the C3(PWM) was the original one, after these simulations, the C3(PWM) was changed.

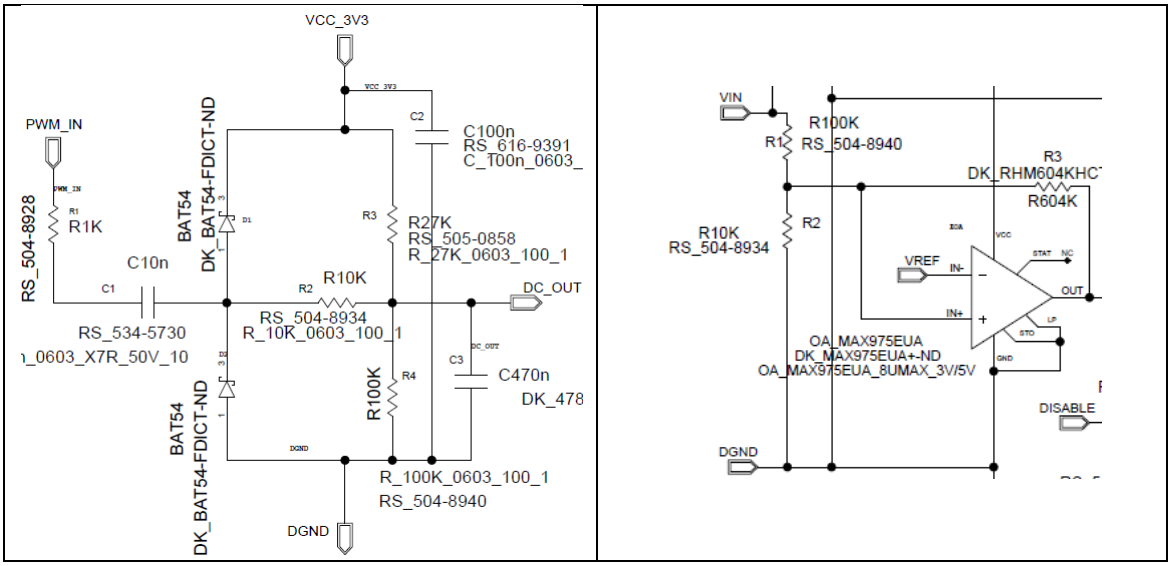


Figure 2.42. PWM schematic and MPPT interesting area.

The following is the table which collects the simulations more significant to evaluate the MPPT efficiency. These two are the fixed values to all simulations:

C3(PWM)=0.047 µF (unless the Probe_PSB_76 to Probe_PSB_84)

R_LOAD_PDB=10 Ω

TMAX: Step of simulation.

Probe_PSB_(num)	D.C.(PWM_IN)(%)	R2(MPPT)(KΩ)	R2(PWM)(KΩ)	TMAX (ns)
76	50	10	10	10
78	50	10	10	10
79	99	10	10	10
81	1	10	10	10
83	25	10	10	10
84	10	10	10	10
86	10	10	10	10
87	90	10	10	10
88	50	10	10	10
89	75	10	10	10
90	25	10	10	10
91	85	10	10	10
92	99	10	10	10
93	99	10	10	1
94	95	10	10	1
97	1	10	10	5
98	75	10	10	5
99	90	9.2	10	5
100	90	9.2	10	5
101	80	9.09	10	5
102	80	9.09	9.01	5
103	80	9.09	20	5
104	80	9.09	8.55	5
105	80	9.09	2	5
106	80	9.09	5.5	5
107	80	10	10	10
108	80	2	10	5
109	80	8.7	10	5
110	80	9.09	10	5
111	80	9.2	10	10

Table 2.12. Simulations to improve the efficiency.

Analyzing the simulations:

- From Probe_PSB_76 to Probe_PSB_84: changing the D.C. of PWM_IN input, but these were so much slow.
- From Probe_PSB_86 to Probe_PSB_98: changing the D.C. of PWM_IN input with the new value for C3(PWM).
- Probe_PSB_99 and Probe_PSB_100: with 90% D.C. and changing R2(MPPT) it is observed that the SOLAR_POS signal changes.

After these simulations, it is chosen a 80% of D.C. and a 9.09 kΩ to R2(MPPT) to calculate the best R2(PWM).

- From Probe_PSB_101 to Probe_PSB_106: changing R2(PWM). The voltage under study is the output PWM to DC converter voltage.

After these simulations, it is chosen a 80% of D.C. and a 10 kΩ to R2(PWM) to calculate the best R2(MPPT).

- From Probe_PSB_107 to Probe_PSB_111: changing R2(MPPT). The voltage under study is the SOLAR_POS voltage.

These are some graphics:

The several PDB voltages, with C3(PWM) = 0.047 µF, R2(MPPT) = 10 kΩ, R2(PWM) = 10 kΩ, PDB LOAD = 10 Ω and different duty cycle.

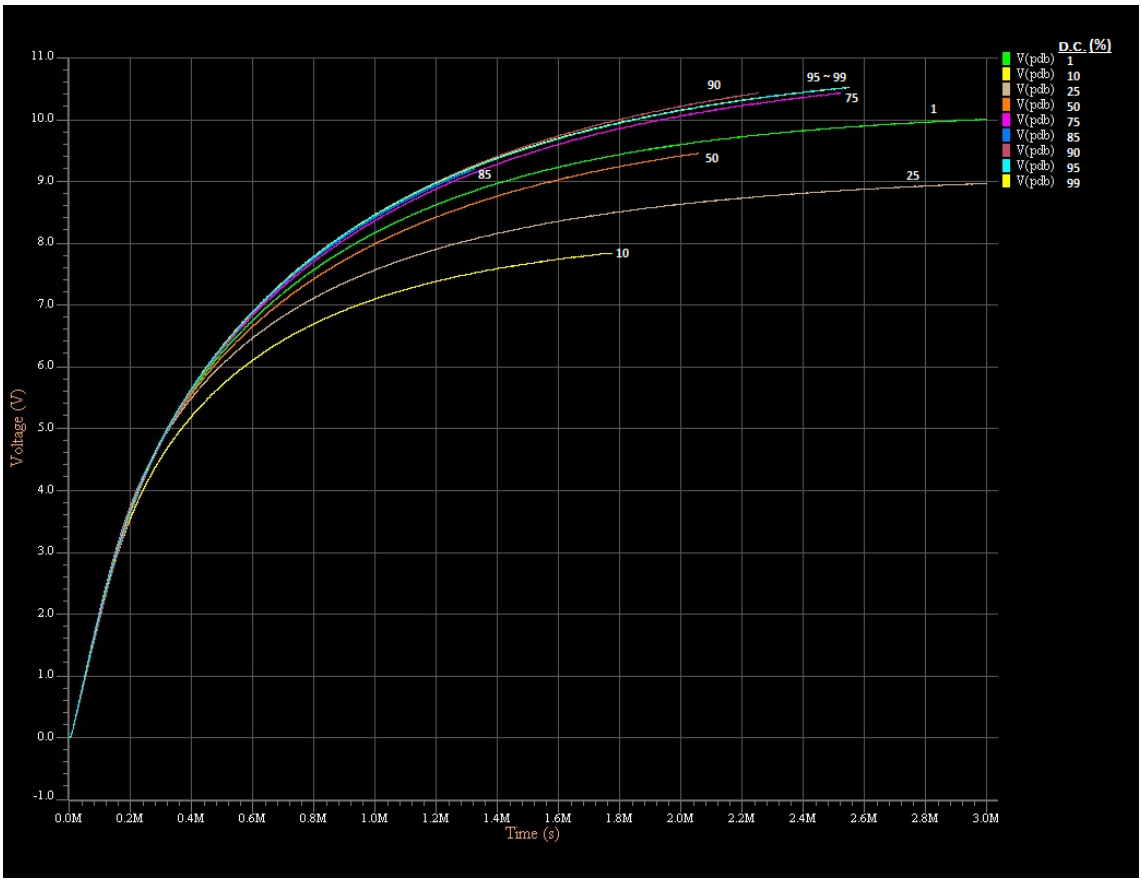


Figure 2.43. PDB voltages, with different duty cycles.

The several SOLAR_POS voltages, with C3(PWM) = 0.047 µF, R2(MPPT) = 10 kΩ, R2(PWM) = 10 kΩ, PDB LOAD = 10 Ω and different duty cycle.

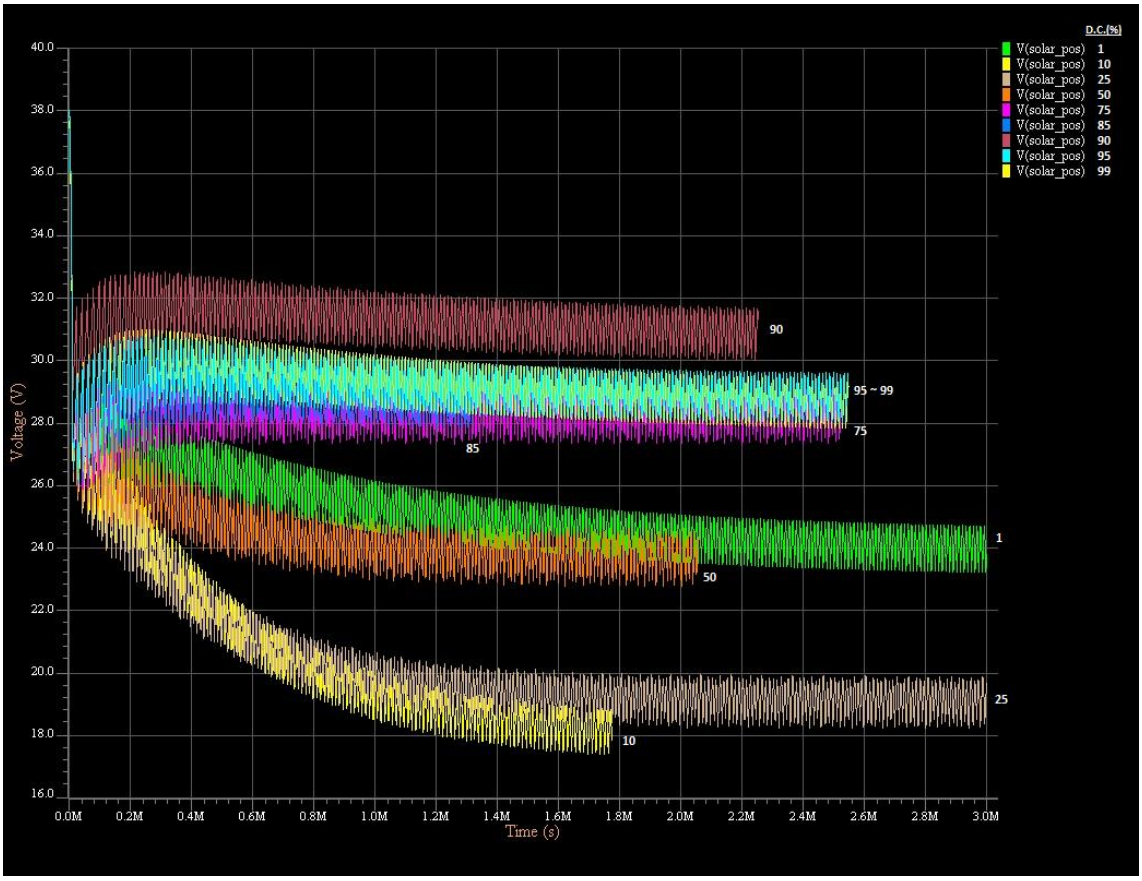


Figure 2.44. SOLAR_POS voltages, with different duty cycles.

We can see that changing the duty cycle, the PWM output changes, and also changes the SOLAR_POS, due that uses the PWM output. Our goal is to maximize the power of the PDB, to achieve that, it is suitable carry the point of work of the solar cells to the maximum point of power, it is about 32 V of SOLAR_POS voltage.

A deeper study of the solar cells will be exposed at the following chapter, it is going to explain the maximum point of work and all issues about solar cells.

So first, it must to study all about changing the duty cycle of the PWM input, and after decide to replace some component in order to improve the efficiency.

The several PWM output voltages, with C3(PWM) = 0.047 µF, R2(MPPT) = 10 kΩ, R2(PWM) = 10 kΩ, PDB LOAD = 10 Ω and different duty cycle.

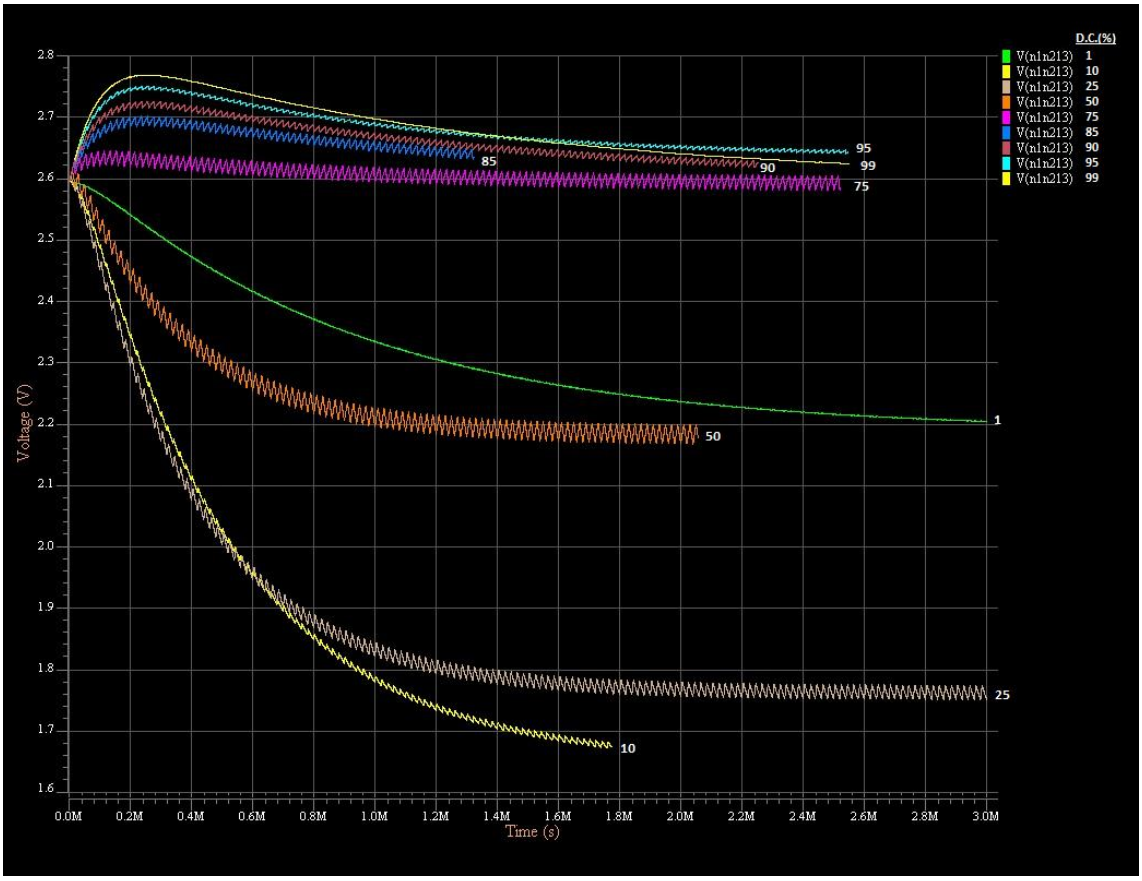


Figure 2.45. PWM output voltages, with different duty cycles.

Now, we can see how the PWM output changes varying the duty cycle on the PWM input. For low duty cycles the response tends to decrease the output voltage below 2.6 V, and for greater duty cycles the output voltage start to increase but after some milliseconds the output voltage is stabilized around 2.6 V.

At future studies, have been chosen two duty cycles with different responses, with the aim to observe what happens changing some value of some components. These two duty cycles chosen are 20% and 80%.

Later we will can see the result of the several simulations.

Graph of Probe _PSB_87 and Probe_PSB_99, which these features: duty cycle: 90%, C3(PWM) = 0.047 µF, R2(PWM) = 10 kΩ, and PDB LOAD = 10 Ω. Probe _PSB_87 with R2(MPPT) = 10 kΩ and Probe _PSB_99 with R2(MPPT) = 9.2 kΩ.

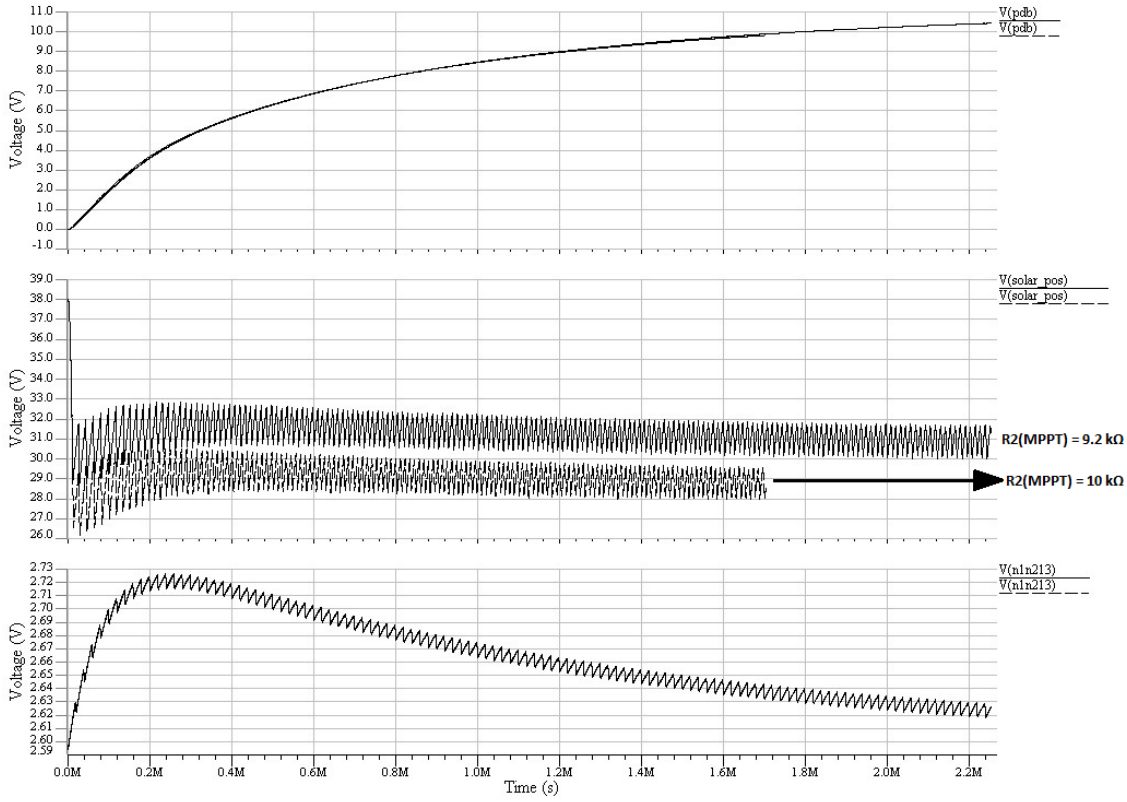


Figure 2.46. Probe _PSB_87 and Probe_PSB_99 graphs.

Having these two cases, where all parameters and all components are the same for both simulations, except the value of R2(MPPT), we can note for the first time that having the same PWM output, it means that the MPPT inputs are the same at both cases, changing the value of R2(MPPT) it is get two different SOLAR_POS voltages.

Analyzing:

- For the original value of R2(MPPT) = 10 kΩ, it is obtained around 28 V at SOLAR_POS.

- For the new value of R2(MPPT) = 9.2 kΩ, it is obtained around 31 V at SOLAR_POS.

We can conclude that decreasing the R2(MPPT) value, it is increased the SOLAR_POS voltage. It is interesting to know that the maximum point of work for the solar cells is 32 V, so in a future study, it will search the suitable R2(MPPT).

The several PWM output voltages, with C3(PWM) = 0.047 µF, R2(MPPT) = 9.09 kΩ, duty cycle = 80%, PDB LOAD = 10 Ω and different R2(PWM).

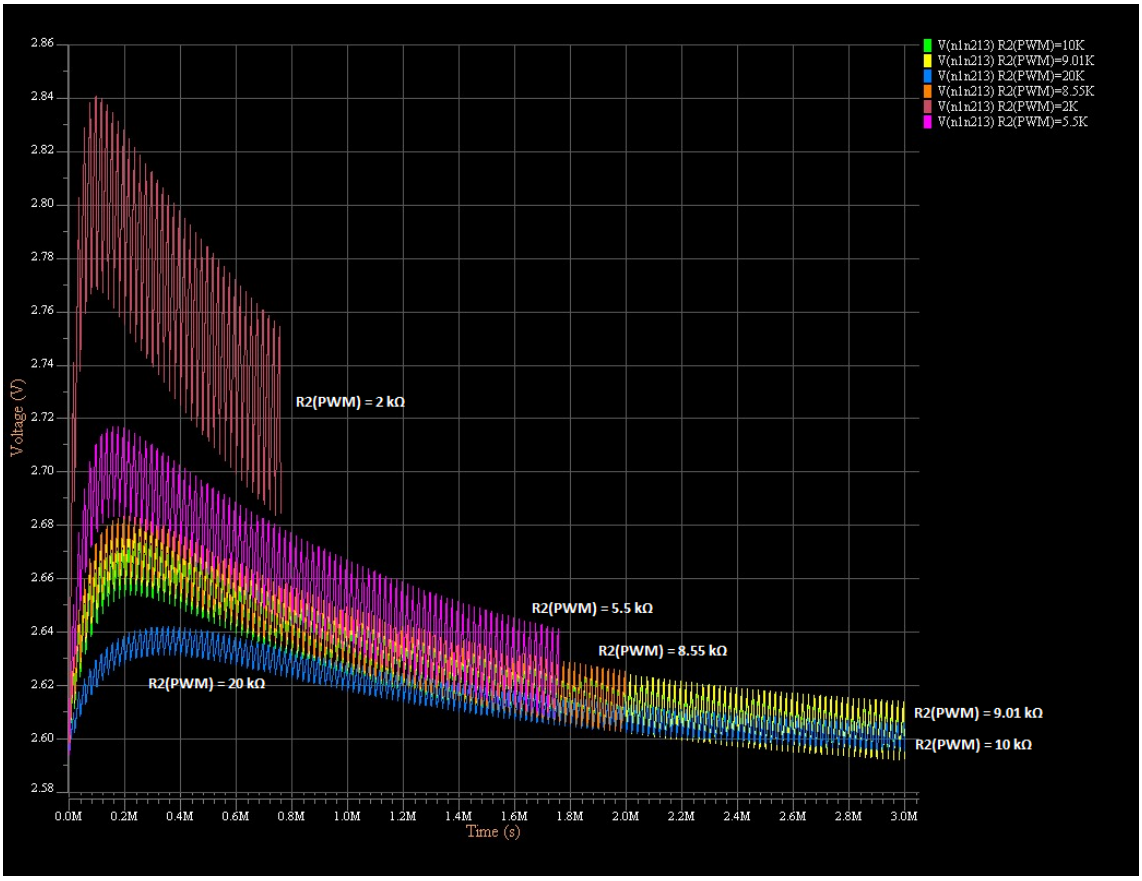


Figure 2.47. PWM output voltages with different R2(PWM).

This time, we can see, that for the components above wrote, for 80% duty cycle for the PWM input and changing the R2(PWM), we expect a voltage around 2.6 V – 2.7 V as in the graph of all PWM outputs. Furthermore, taking in account that now all simulations are with D.C. = 80%, all values more or less will be similar.

So, after see the curves, we can resume that:

- If R2(PWM) is big, the output varies slowly.
- If R2(PWM) is small, the output varies faster.

Always working at acceptable values, between 2.5 V to 2.9 V.

Then, for the last efficiency study it is take in account two values to observe the results, these values are 2 kΩ and 10 kΩ.

The several SOLAR_POS voltages, with C3(PWM) = 0.047 µF, R2(PWM) = 10 kΩ, duty cycle = 80%, PDB LOAD = 10 Ω and different R2(MPPT).

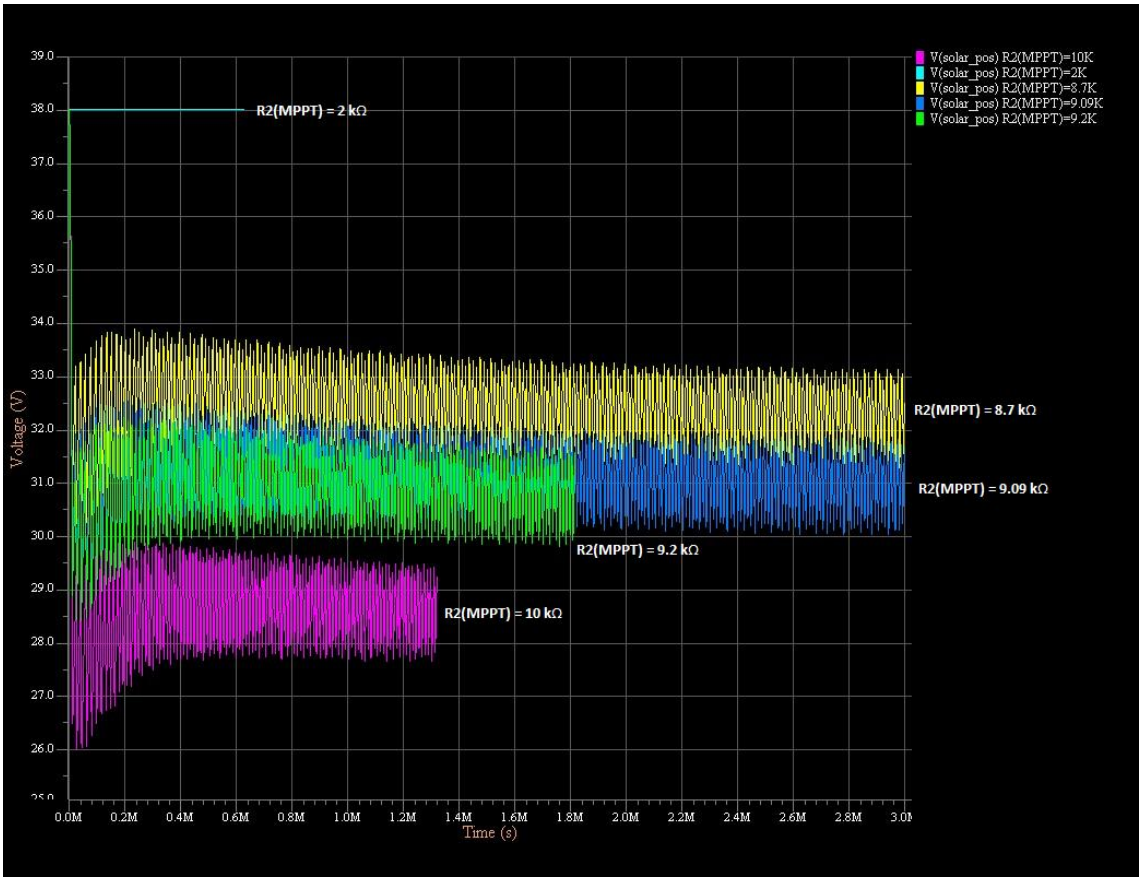


Figure 2.48. SOLAR_POS voltages with different R2(MPPT).

It can see that for the originally value of R2(MPPT) = 10 kΩ, the SOLAR_POS voltage is around 28 V – 29 V, and it is possible raise this value until 32 V. Due that the maximum voltage that the solar cells can work well is 32 V. So, the new value under study for R2(MPPT) is 9.09 kΩ, because it is the closest value to achieve 32 V at SOLAR_POS.

- $R2(MPPT) \approx 10\ k\Omega \ \rightarrow \ \mathrm{SOLAR_{POS}} \approx 27 - 29\ V$
- $R2(MPPT) \approx 9\ k\Omega \ \rightarrow \ \mathrm{SOLAR_{POS}} \approx 32 - 30\ V$
- $R2(MPPT) \approx 8.7\ k\Omega \ \rightarrow \ \mathrm{SOLAR_{POS}} \approx 33.5 - 31\ V$

After these simulations and studying the waves for the different cases, it is observed that:

- The PWM output varies changing the duty cycle of the PWM_IN.
- The SOLAR_POS varies according the R2(MPPT) value.

Now it is time to see which is the best case to improve the efficiency of the MPPT block. Our goal is to maximize the power of the PDB, or what is the same, maximize the voltage of the PDB. So, our choose to observe this, are two different duty cycles to check how are distant each other, these are D.C. = 80% and D.C. = 20%.

After several simulations, the suitable value for R2(MPPT) is 9.09 kΩ. For R2(PWM) it is take in account two cases, 2 kΩ and 10 kΩ. And the last resistor modification was the R1(PWM), originally was 1 kΩ and it is probe changing the value to 330 Ω.

The following is the resume table which the resistors for this study:

Probe_PSB_(num)	D.C.(PWM_IN)(%)	R2(MPPT)(KΩ)	R2(PWM)(KΩ)	R1(PWM)(Ω)
101	80	9.09	10	1 k
105	80	9.09	2	1 k
115	20	9.09	2	1 k
116	20	9.09	10	1 k
118	80	9.09	10	330
119	80	9.09	2	330
123	20	9.09	10	330
124	20	9.09	2	330

Table 2.13. Efficiency study.

And the graph is shown below.

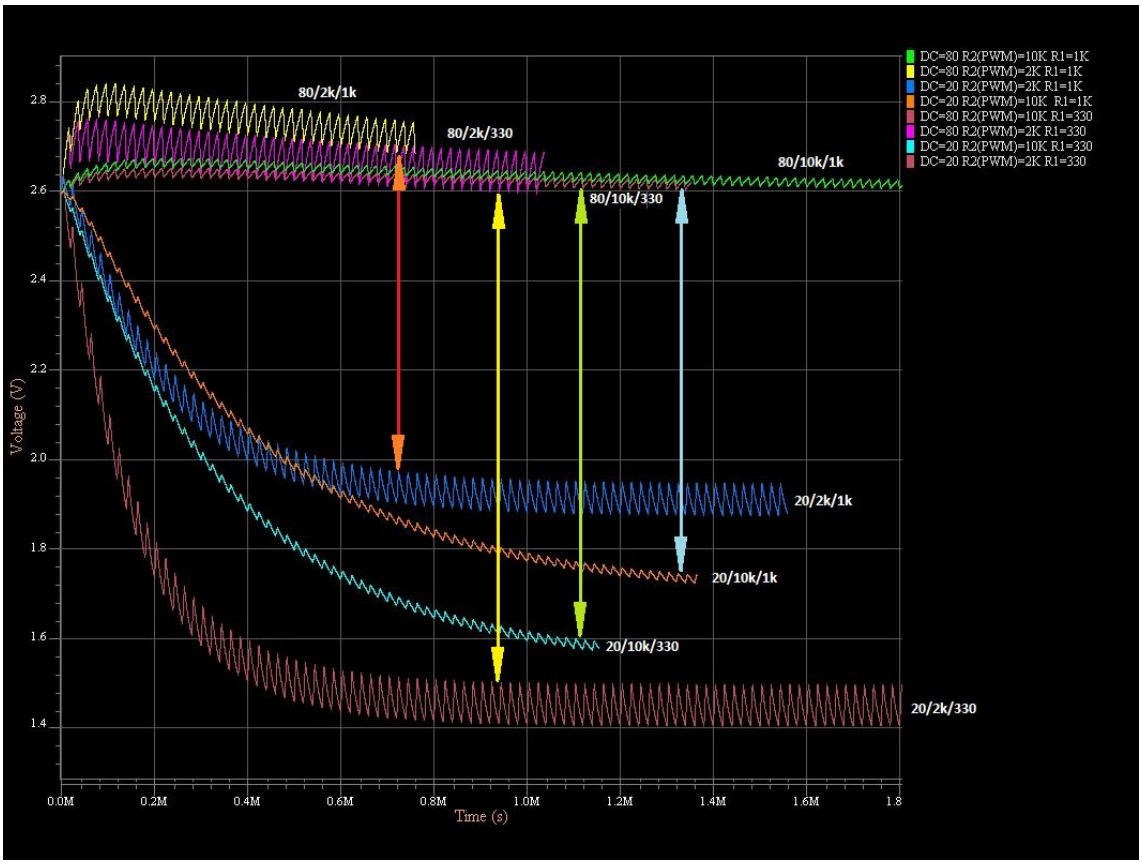


Figure 2.49. Efficiency graph.

To conclude this section we can observe that comparing the difference between the pair of curves (D.Cs.: 20% and 80%) for R2(PWM) = 2 kΩ and R1(PWM) = 1 kΩ, and the difference between the pair of curves for R2(PWM) = 2 kΩ and R1(PWM) = 330 Ω (red and yellow differences). We can see that for yellow case, the difference is bigger, so with R1(PWM) = 330 Ω, it is achieved maximize the voltage of PDB.

Observing the other two differences, for R2(PWM) = 10 kΩ and R1(PWM) = 330 Ω is bigger than for R2(PWM) = 10 kΩ and R1(PWM) = 1 kΩ.

So, to conclude this chapter, in a new version of PWM_DC_Converter and MPPT, the new values to applied these improvements and work at maximum point of work to maximize the efficiency, it must place this resistor values:

- R1(PWM) = 330 Ω.
- R2(MPPT) = 9.09 kΩ.
- R2(PWM) = 2 – 10 kΩ, depending the desired response.

Chapter 3

Testing tools

The Honeycomb Tile measures 16.5x33.0 cm^2, with 10 mm thick honeycomb structure for more rigid and larger structures, in comparison with the CubeSat Standard Tile [15]. Each tile hosts 14 solar cells and two lithium ion batteries.

1B111C_Solar_Panel_HoneyComb is a solar panel array that consists of 14 triple junction, GaAs solar cells (2.2 V each) and protection diodes. It converts the solar power to electrical power used by the satellite subsystems. The 14 solar cells are connected in series to achieve an output voltage of approximately 30.8 V with 0.4 A current and 12.32 W output power.

To get the electrical power that our solar cells convert from the solar energy, a PSpice subcircuit is created composed by a DC current source, three diodes and two resistances.

3.1 – Solar cell simulation

The following are the subcircuit and the schematic of the simulated solar cell.

```
.SUBCKT SolarCell 1 4

IPH1 4 3 DC 0.42
D1 3 5 D1N4002
D2 5 6 D1N4002
D3 6 4 D1N4002
Rp 3 4 800
Rs 3 1 0.1

.MODEL D1N4002 D (IS=14.11E-9
N=1.984 RS=33.89E-3 IKF=94.81 XTI=3
+ EG=1.110 CJO=51.17E-12 M=.2762
VJ=.3905 FC=.5 ISR=100.0E-12
+ NR=2 BV=100.1 IBV=10 TT=4.761E-6)

.ENDS
```

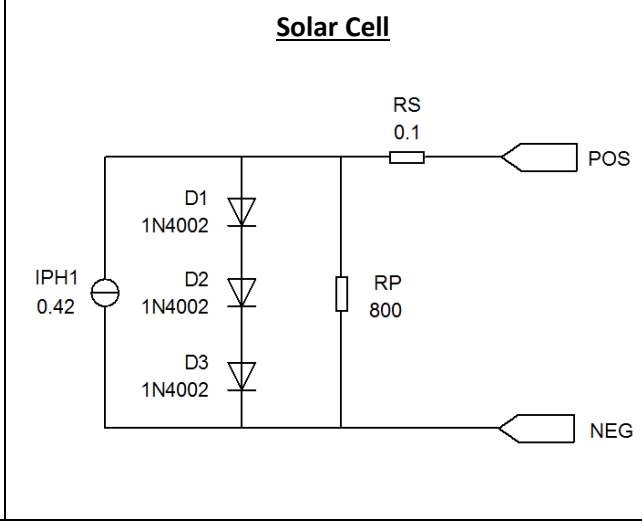


Figure 3.1. Solar cell subcircuit and schematic.

This is the symbol of a solar cell at Mentor Graphics software, with two protection diodes.

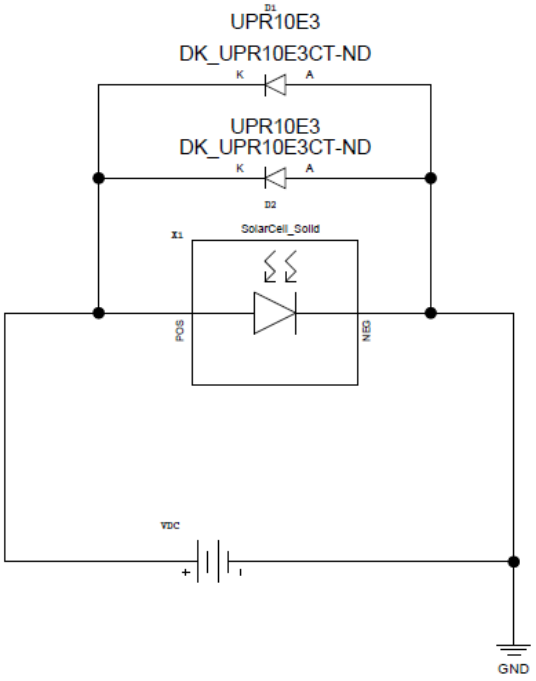


Figure 3.2. Solar cell symbol with two protection diodes.

And this is the Voltage/Current characteristic:

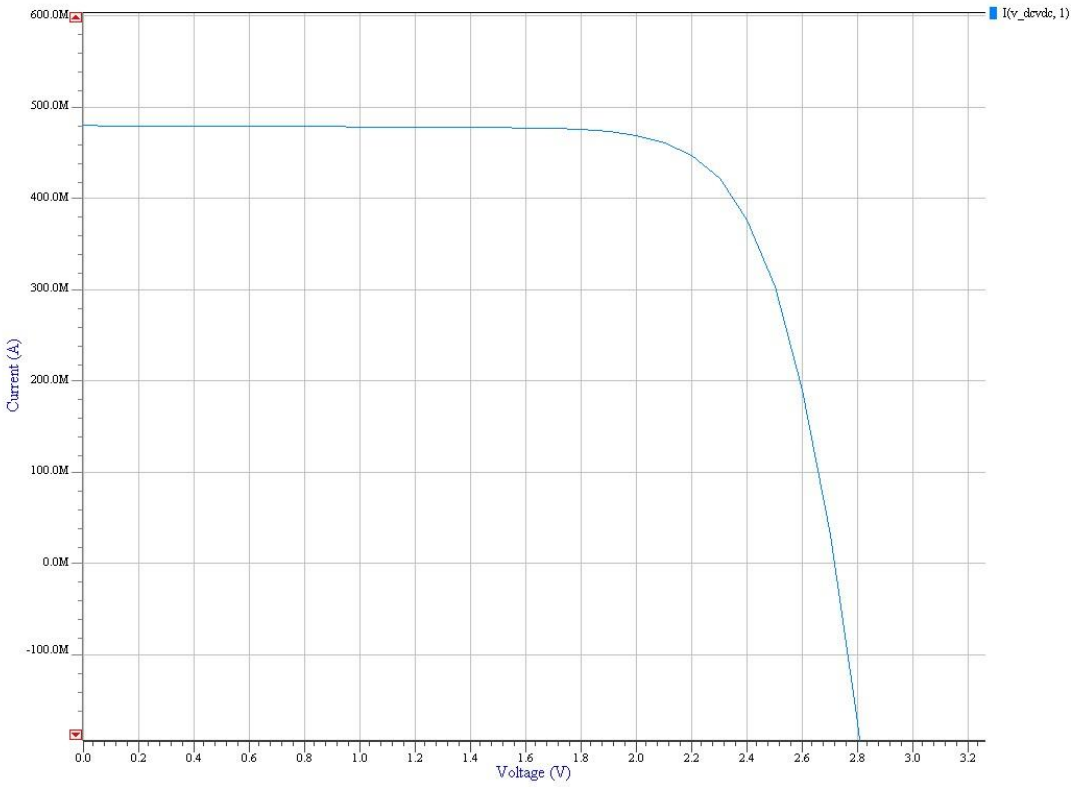


Figure 3.3. Solar cell Voltage/Current characteristic.

We can observe a constant current around 0.48 A, and a good work voltage until 2.2 V, approximately.

Also, the schematic of two solar cells in series is done to check if the simulation results were as expected.

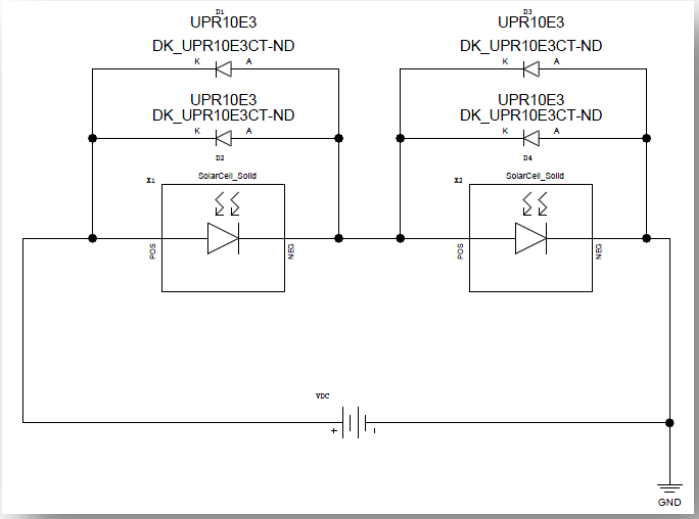


Figure 3.4. Two solar cells schematic.

The Voltage/Current characteristic is shown below:

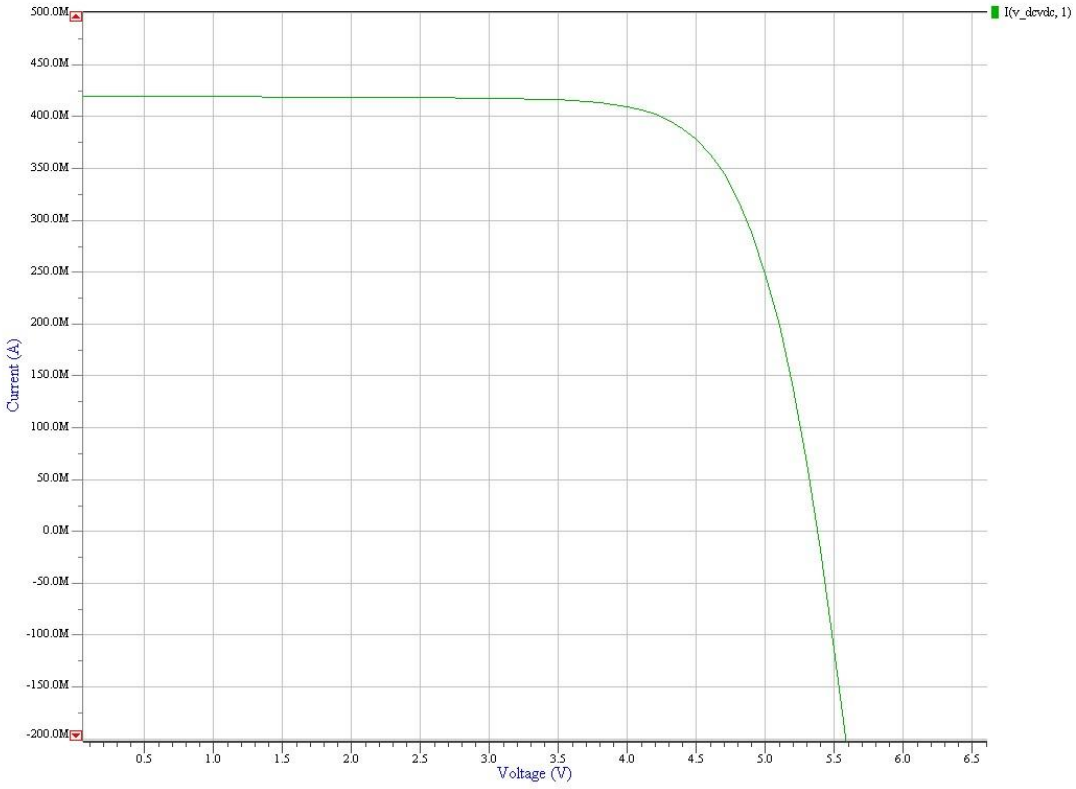


Figure 3.5. Two solar cells Voltage/Current characteristic.

Now, the current decreases until 0.42 A and the maximum voltage for an acceptable work is equal to 4.4 V. Finally, fourteen solar cells in series are connected as the schematic shows below.

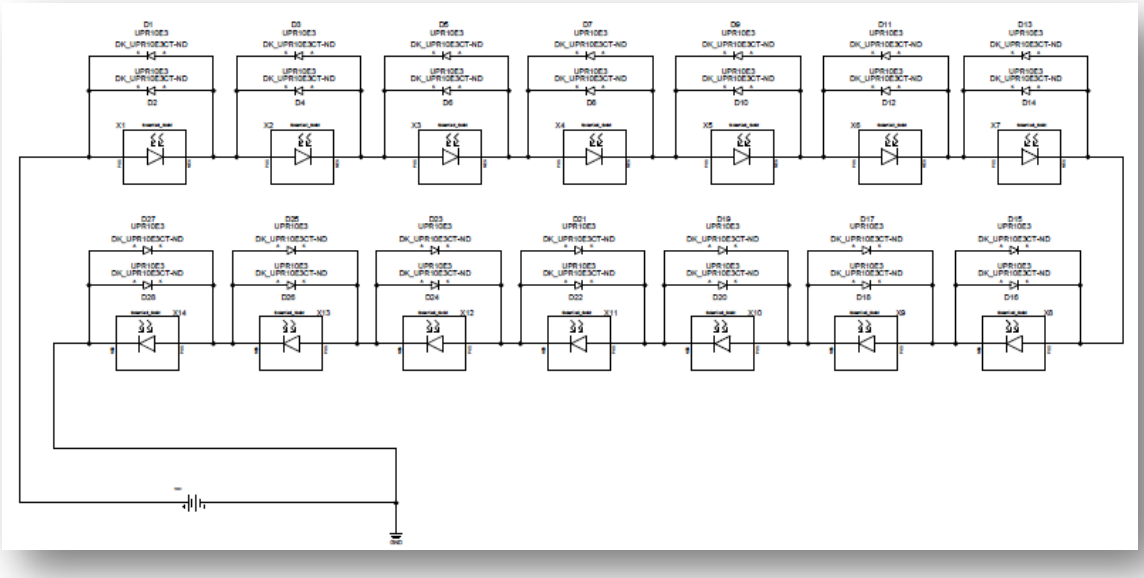


Figure 3.6. Fourteen solar cells schematic.

The Voltage/Current characteristic curve is shown at the following graph. As it is expected, the fourteen solar cells present a current at linear area of 0.482 A, approximately. Besides, the maximum point of power is around 32 V.

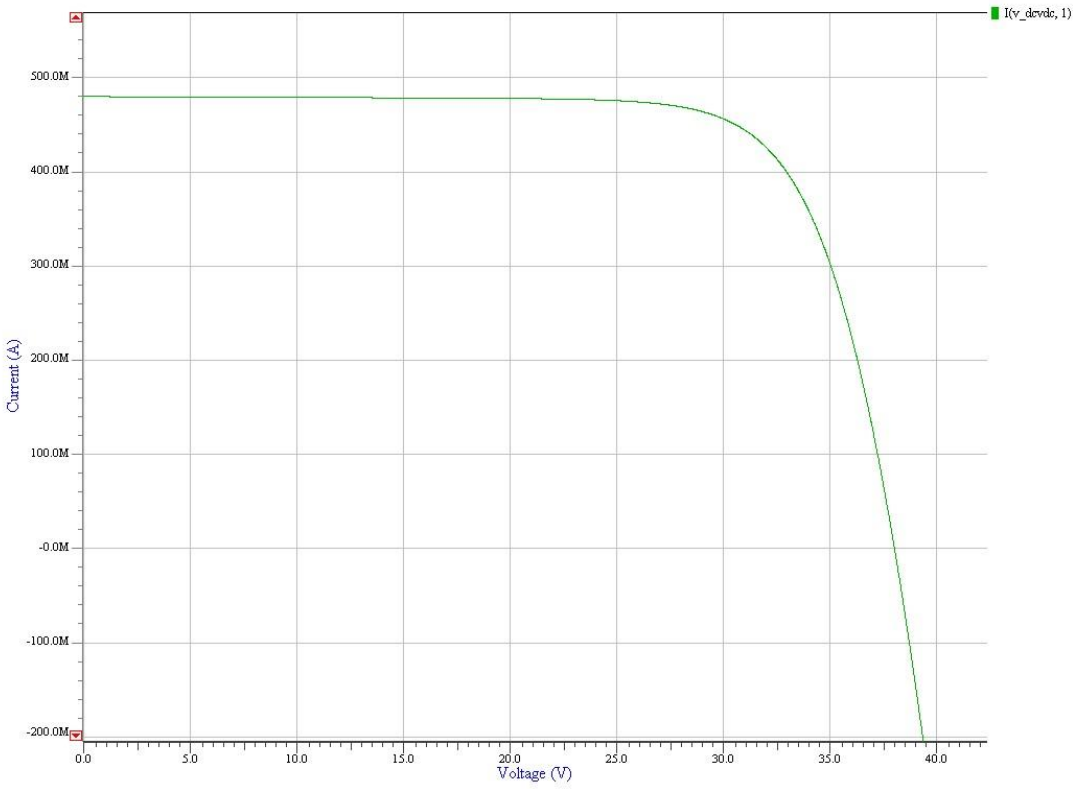


Figure 3.7. Fourteen solar cells Voltage/Current characteristic.

Due that for implement physically this solar cell model are needed twenty eight resistances, forty two diodes and twenty eight protection diodes, it is decided to implement physically another model to achieve approximately the same Voltage/Current curve using less components.

In the next point, it is going to explain the new solar cell model.

3.2 – Solar cell physical model

The new solar cell model is composed by two resistances and a NPN transistor.

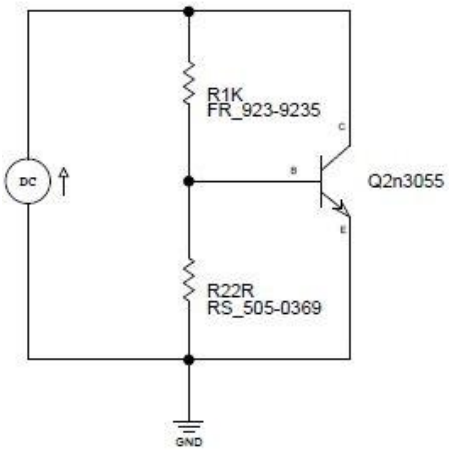


Figure 3.8. Fourteen solar cells physical subcircuit.

This is the Voltage/Current characteristic curve of the new solar cell model approximation.

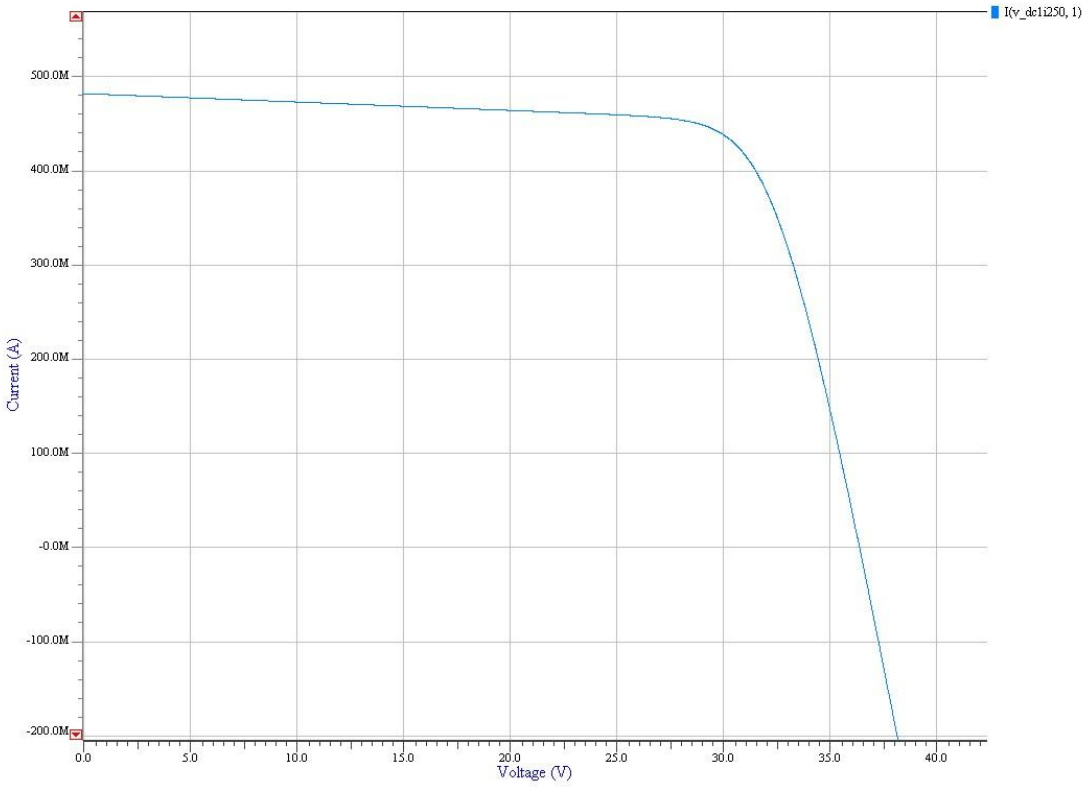


Figure 3.9. Fourteen solar cells physical model Voltage/Current characteristic.

We can see that the curve is almost equal to the previous one. Nevertheless, the current is not a straight line, but it is acceptable. Moreover, the voltage is a little bit more limited.
Observing the approximation models, both curves are plotted at the same graph.

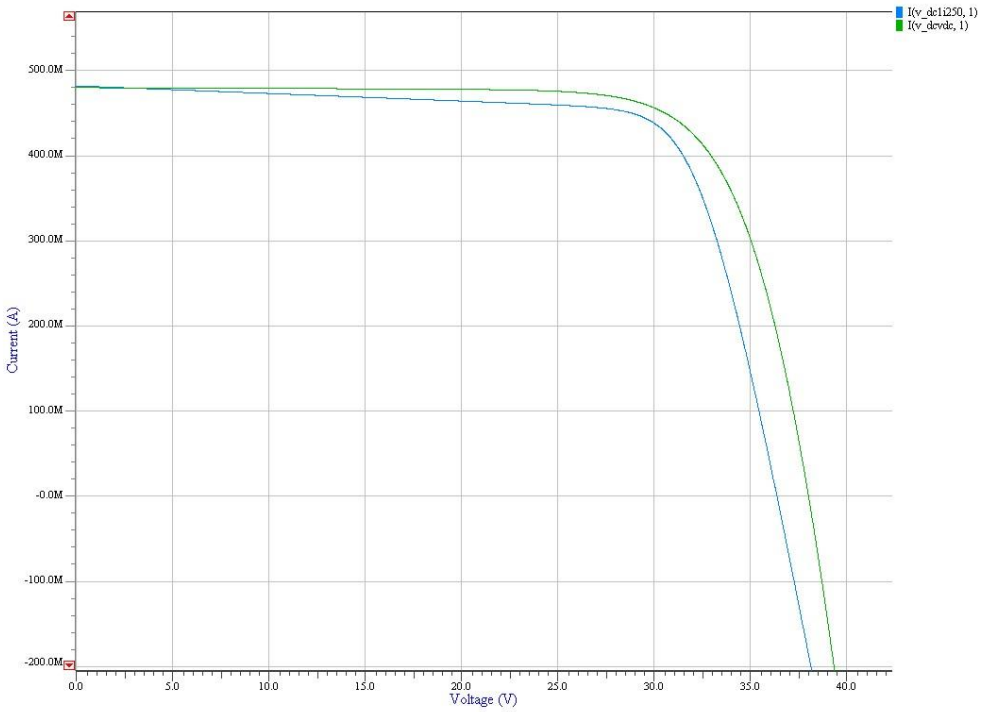


Figure 3.10. Fourteen solar cells simulated model and physical model Voltage/Current characteristics.

As it is shown, both curves are similar, the blue one is the physical implemented curve, which achieves a little bit less power than the solar cell simulation model. But it is enough for our purpose.
The following are the top and the bottom views of the created solar cell from the physical model.

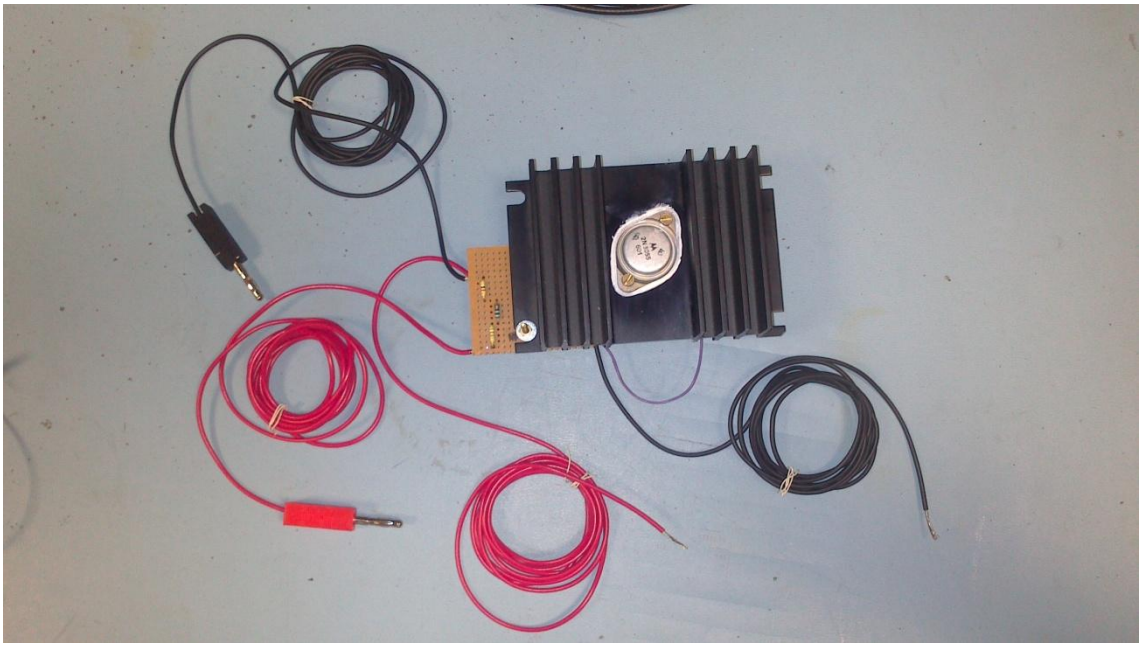


Figure 3.11. Fourteen solar cells physical model top view.

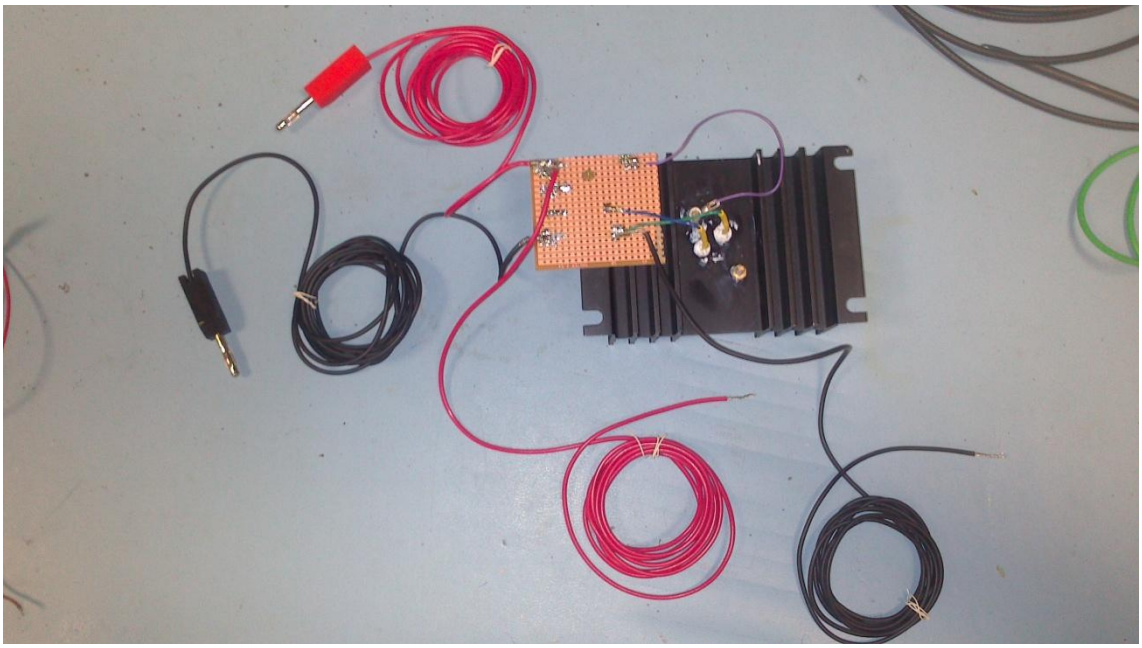
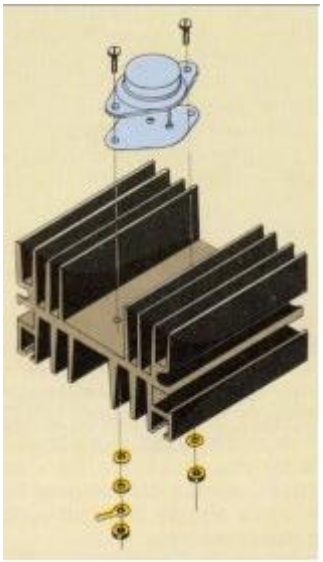
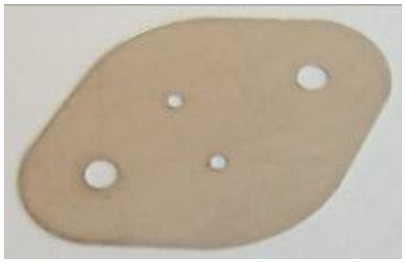


Figure 3.12. Fourteen solar cells physical model bottom view.

The fabrication procedure of this solar cell simulator was the following. First, a board is taken to solder the resistors. Once done, the transistor is placed on the heat sink. Between the transistor and heat sink, an insulating mica is placed, and thermal insulating paste is put at the two faces of the insulating mica. Then, the transistor is screwed to the heat sink. The next step, is to screw the board with the resistors at the heat sink to make a solid solar cell simulator. The last step is to solder the wires for doing the proper connections, and place the last insulators at the emitter and base of the transistor with heat shrinkable tubes.



a)



b)

c)

Figure 3.13. a)Transistor mounting procedure; b)Insulating mica; c)Thermal insulating paste.

This is the solar cell plugged at the real satellite. The dimensions are 40mm x 70mm.

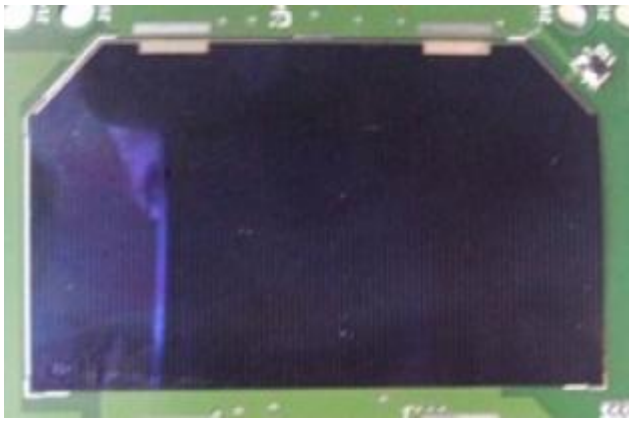


Figure 3.14. Real solar cell.

3.3 – Characterization of the solar cell with programmable load

To characterize the solar cell implemented physically, a programmable load is used, available at hardware laboratory. Taking the solar cell and plugging the DC power supply with around 40 V and 0.48 A and the programmable load, we have the system ready for the characterization. The test starts with a 500 Ω load, and its value is decreasing.

The graph result of the collected data of the test is plotted with Maltlab tool. Also, some points of the solar cell simulation model curve are taken and are plotted both curves.

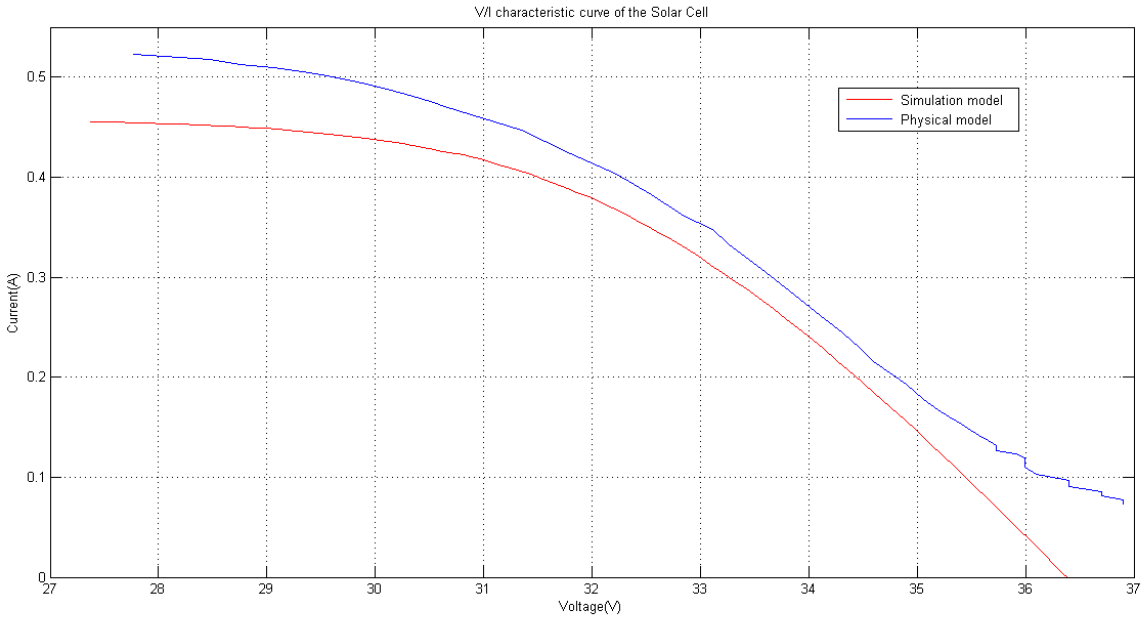


Figure 3.15. Characterization of the solar cell with programmable load.

We can observe that the real solar cell model have a similar behavior as expected. We want to comment that when the load was lower than 54Ω, the programmable load and the supply voltage start working poor.

For this reason, the graph covers from 27.5 V to 36.5 V, approximately. This is the region where the current leaves the linear behavior and begins to decrease. At this area, it is found the maximum point of power, around 32 V.

With the power supply set up with 40 V and 0.48 A plugged to the solar cell model, and this connected to the programmable load, starting with 500 Ω, is obtained at the output 36.90 V and 0.073 A, and for the lower programmable load value, 54 Ω, is obtained at the output 27.77 V and 0.523 A.

We can note that, lower is the load, lower is the voltage and greater is the current.

The tables with the test values and the voltage and current points (which were taken from the simulation of the solar cell) used for the previous graph, are available at the Appendix B.

The following, is the block diagram to characterize the solar cell behavior.

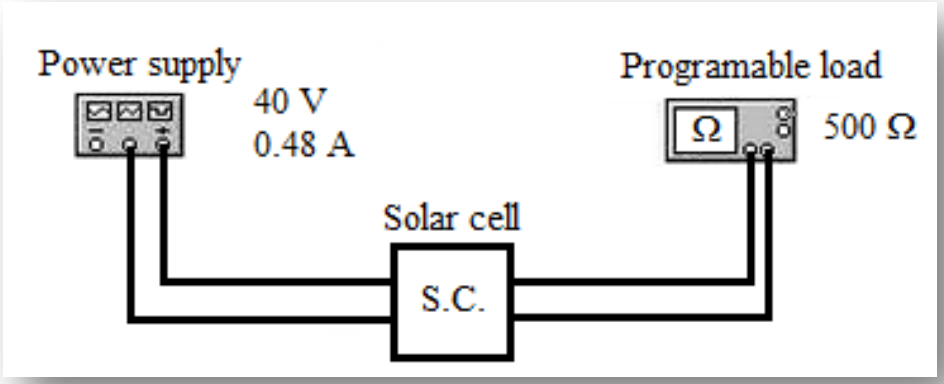


Figure 3.16. Characterization solar cell block diagram.

The information and pictures about the equipments used for the measurements are added at the Appendix C.

3.4 – Simulation of several number of solar cells connected in series

At this point was carried out a study to model a several cases of solar cells connected in series. In our study was taken into account the model of 2, 4, 6, 8, 10, 12 and 14 solar cells.

Below, the graph of the result:

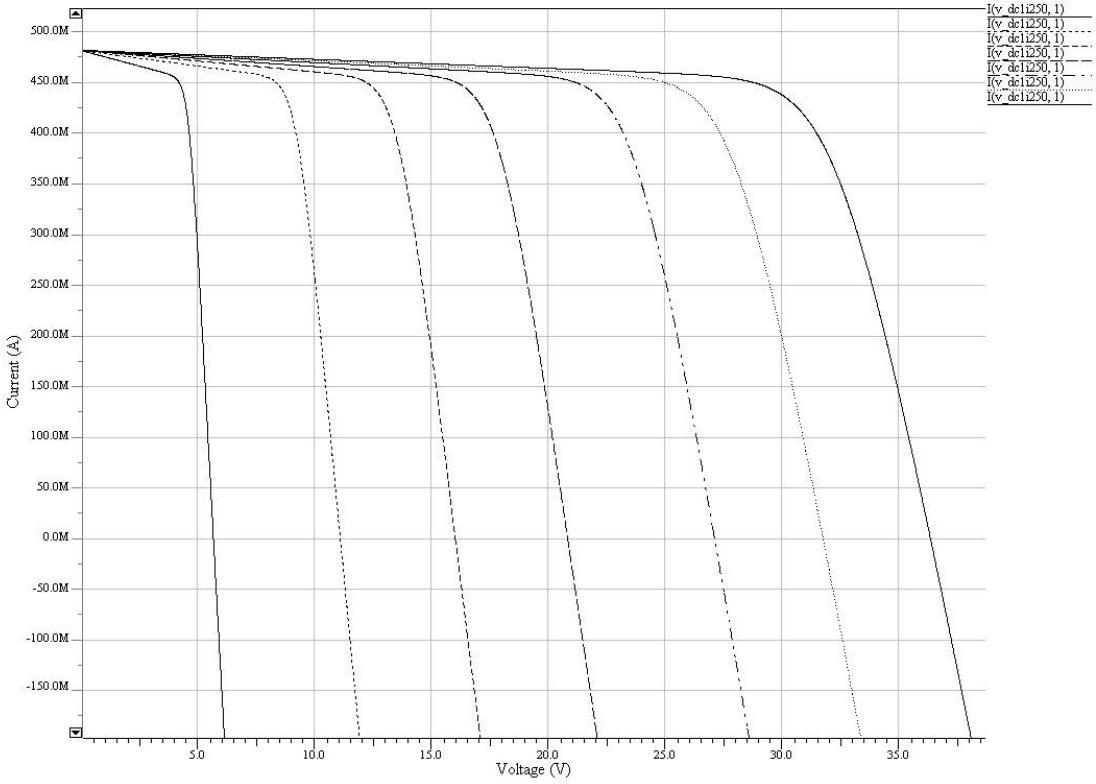


Figure 3.17. Different curves for 2, 4, 6, 8, 10, 12 and 14 solar cells connected in series.

Our proposal is to maintain the transistor and a resistor, and to only change the value of the another resistor. We have set the value of R1 = 1 kΩ and vary the R2 value. Then, interpolating R2 values, it has to find the voltage values calculated below.

Then, if the maximum point of work for 14 solar cells (SC) is around 32 V, for the rest of cases are:

$$V_{X\_SC} = \frac{32V}{14\ SC} \times n^{\underline{o}}\ SC$$

$$V_{2\_SC} = \frac{32V}{14\ SC} \times 2\ = 4.6\ V\ \ \rightarrow\ \ R1 = 140\ \Omega \div 150\ \Omega$$

$$V_{4\_SC} = \frac{32V}{14\ SC} \times 4\ = 9.2\ V\ \ \rightarrow\ \ R1 = 300\ \Omega$$

$$V_{6\_SC} = \frac{32V}{14\ SC} \times 6\ = 13.7\ V\ \ \rightarrow\ \ R1 = 450\ \Omega$$

$$V_{8\_SC} = \frac{32V}{14\ SC} \times 8\ = 18.3\ V\ \ \rightarrow\ \ R1 = 600\ \Omega$$

$$V_{10\_SC} = \frac{32V}{14\ SC} \times 10\ = 22.9\ V\ \ \rightarrow\ \ R1 = 800\ \Omega$$

$$V_{12\_SC} = \frac{32V}{14\ SC} \times 12\ = 27.4\ V\ \ \rightarrow\ \ R1 = 900\ \Omega$$

$$V_{14\_SC} = \frac{32V}{14\ SC} \times 14\ = 32\ V\ \ \rightarrow\ \ R1 = 1\ k\Omega\ \div 1.2\ k\Omega$$

To select the suitable R1 for 14 solar cells, three graphs are plotted, corresponding with $R1 = 1\ k\Omega$, $R1 = 1.1\ k\Omega$ and $R1 = 1.2\ k\Omega$.

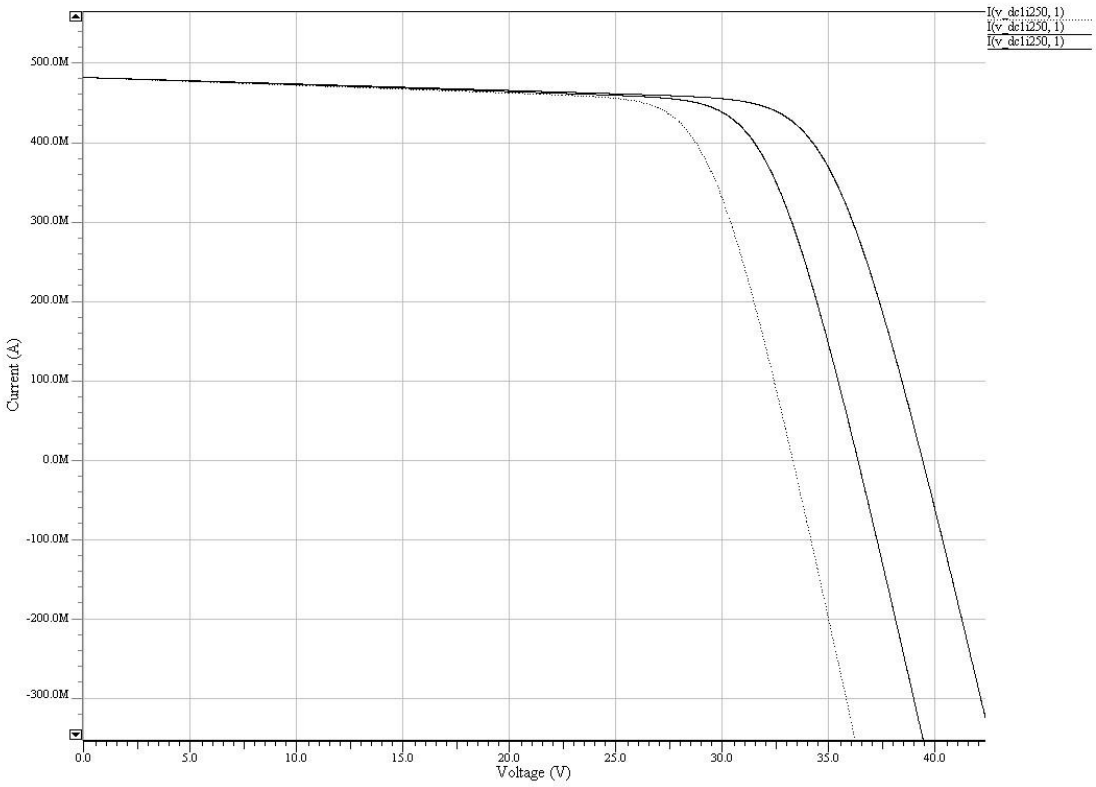


Figure 3.18. Different curves for R1=1 kΩ, R1=1.1 kΩ and R1=1.2 kΩ.

The graph with lower point of work is for $R1 = 1\ k\Omega$ and the greater point of work is for $R1 = 1.2\ k\Omega$. To our purpose, the suitable R1 would be $R1 = 1.1\ k\Omega$.

Chapter 4

Simulations results

After achieve all the Spice models and solve the simulations problems, it is possible to simulate the sensors, the regulators, the PWM to DC converter and the MPPT blocks. Doing that, the behavior of the blocks is checked.

Firstly, the individual blocks are simulated, once done that, the entire primary switching buck block can be checked. In the next chapter, the collected data regarding the primary switching buck block will be exposed.

4.1 – Reusable block simulations

To check the sensor behavior, a DC SWEEP simulation is done, verifying that the operation range is as expected.

Moreover, for the regulators, the PWM to DC converter and the MPPT, a TRANSIENT analysis is done to check if these blocks had a good performance.

Voltage sensors

They convert, through a voltage divider, the input voltage between input pin VIN and analog ground AGND to an output voltage between pin VOUT and analog ground AGND.

For the voltage sensors, the input voltage shall range between 0 and a maximum value which depends on the specifications of Bk1B131_Voltage_Sensor (see tagged value INPUT_RANGE), while output voltage is in the range 0 to OUTPUT_RANGE.

Output voltage is given by:

$$V(VOUT) = V(VIN) \times SENS\_VOUT$$

Current sensors

They convert positive current flowing from pin I_IN to pin I_OUT into an output voltage between pin CS_VOUT and analog ground AGND.

For the current sensors, input current shall be in a range which depends on the specification of Bk1B132_Current_Sensor (see tagged value INPUT_RANGE), while output voltage is in the range 0 to OUTPUT_RANGE.

Output voltage is given by:

$$V(CS\_VOUT) = I(I\_IN) \times SENS\_CS\_VOUT$$

where I(I_IN) is the current entering from pin I_IN and exiting I_OUT, while SENS_CS_VOUT depends on the specification of Bk1B132_Current_Sensor.

4.1.1 – Bk1B132C_Current_Sensor_V1

Seeing the specifications of this sensor:

INPUT_RANGE = 2.5

SENS_CS_VOUT = 1

OUTPUT_RANGE = 2.5

For the maximum value:

$$V(CS\_VOUT) = I(I\_IN) \times SENS\_CS\_VOUT = 2.5 \times 1 = 2.5\,V$$

It means that for 2.5 A input current, 2.5 V output voltage is got. The maximum value of the range is taken to give an example.

This is a SWEEP analysis set to 0 from 2.5 A at I_IN input.

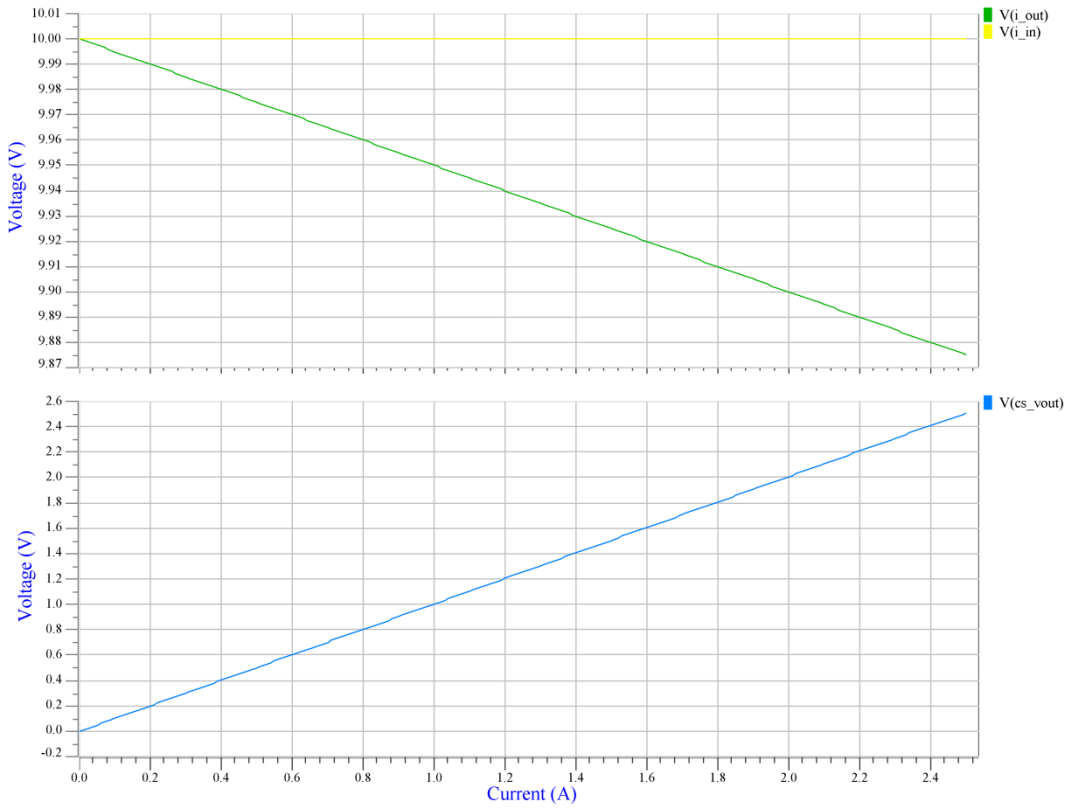


Figure 4.1. Bk1B132C_Current_Sensor_V1 simulation.

We can see the result as expected, to 0 from 2.5 A at I_IN input, to 0 from 2.5 V is achieved at CS_VOUT output.

Also, a temperature SWEEP analysis was done between -40ºC to 125ºC, the operating range of the sensor.

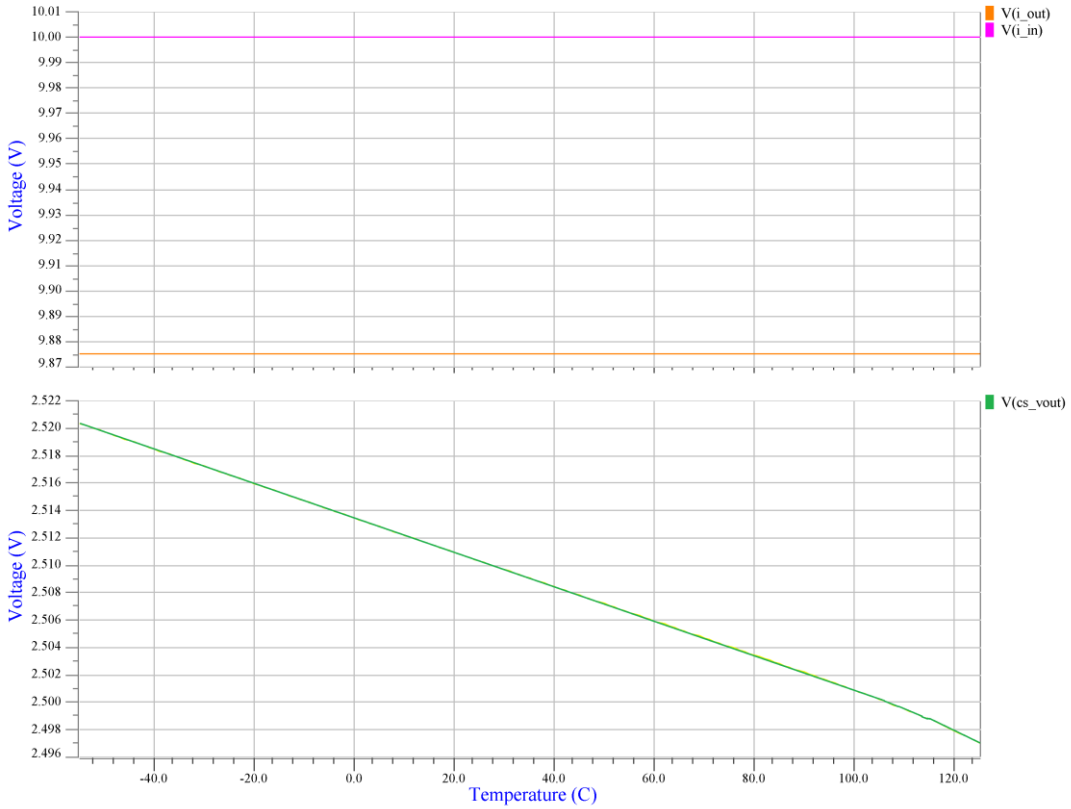


Figure 4.2. Bk1B132C_Current_Sensor_V1 temperature sweep.

A good performance is obtained for the temperature SWEEP, with around 2.5 V output during all the sweep.

4.1.2 – Bk1B132E_LowSideCurrentSensor_V1

Seeing the specifications of this sensor:

INPUT_RANGE = 0.4

SENS_CS_VOUT = 7.5

OUTPUT_RANGE = 3

For the maximum value:

$$V(CS\_VOUT) = I(I\_IN) \times SENS\_CS\_VOUT = 0.4 \times 7.5 = 3\,V$$

It means that for 0.4 A input current, 3 V output voltage is got. The maximum value of the range is taken to give an example.

The following is the SWEEP analysis set to 0 from 0.4 A at I_IN input.

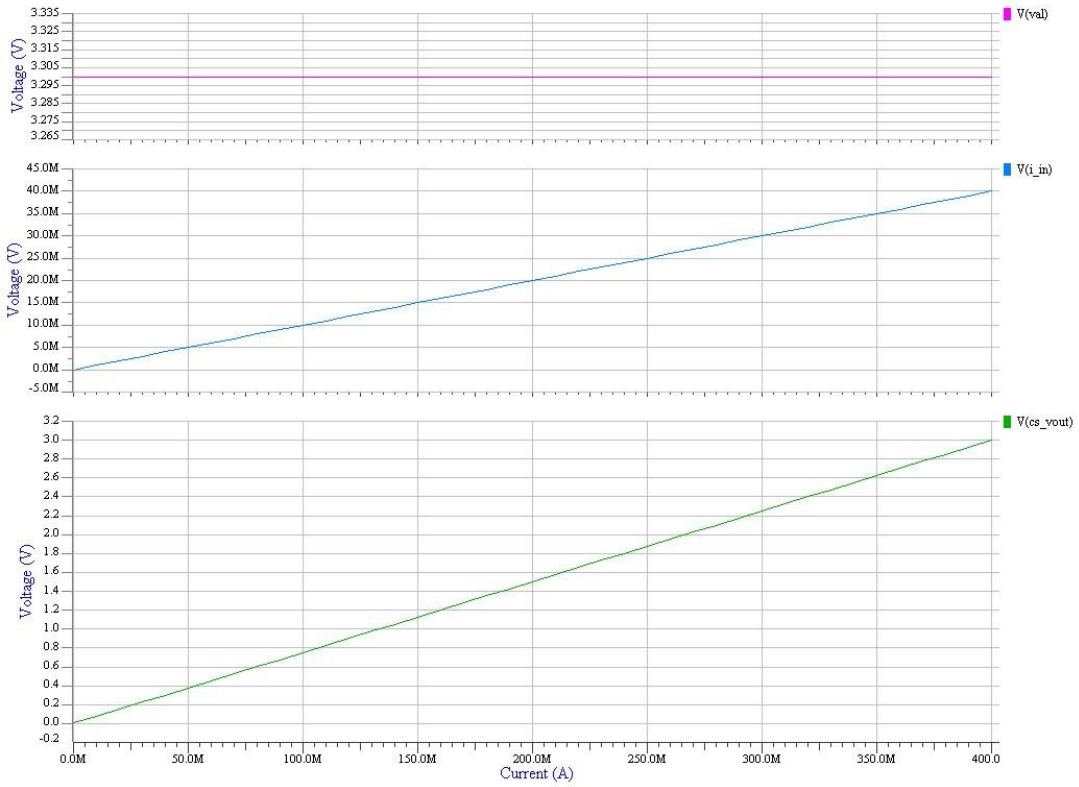


Figure 4.3. Bk1B132E_LowSideCurrentSensor_V1 simulation.

The sensor has a performance as expected, like we can see at graph to 0 from 0.4 A at I_IN input, to 0 from 3 V is obtained at CS_VOUT output.

4.1.3 – Bk1B131D_Voltage_Sensor_V1

Seeing the specifications of this sensor:

INPUT_RANGE = 40

SENS_VOUT = 0.0643

OUTPUT_RANGE = 2.5

For the maximum value:

$$V(VOUT) = V(VIN) \times SENS_{VOUT} = 40 \times 0.0643 \approx 2.5\,V$$

It means that for 40 V input voltage, 2.5 V output voltage is got. The maximum value of the range is taken to give an example.

The following is the SWEEP analysis set to 0 from 40 V at I_IN input.

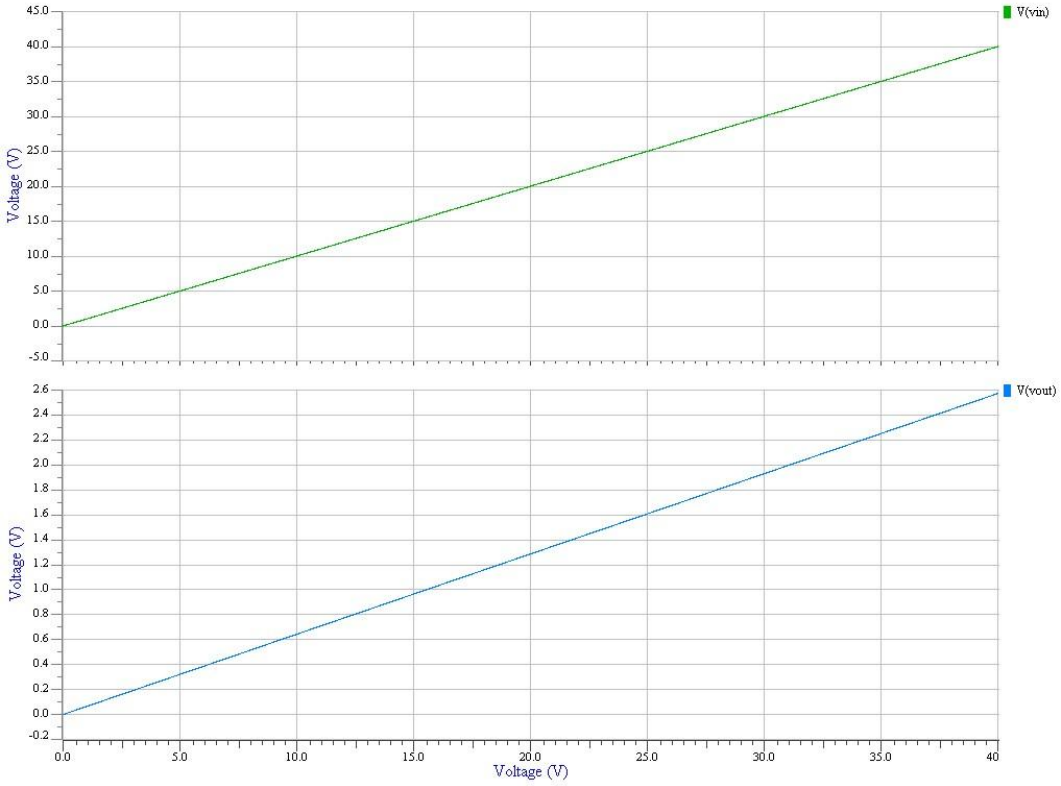


Figure 4.4. Bk1B131D_Voltage_Sensor_V1 simulation.

The sensor has a performance as expected, like we can see at graph to 0 from 40 V at I_IN input, to 0 from 2.5 V is obtained at CS_VOUT output.

4.1.4 – Bk1B131C_Voltage_Sensor_V1

Seeing the specifications of this sensor:

INPUT_RANGE = 20

SENS_VOUT = 0.1277

OUTPUT_RANGE = 2.5

For the maximum value:

$$V(VOUT) = V(VIN) \times SENS_{VOUT} = 20 \times 0.1277 \approx 2.5\,V$$

It means that for 20 V input voltage, 2.5 V output voltage is got. The maximum value of the range is taken to give an example.

The following is the SWEEP analysis set to 0 from 20 V at I_IN input.

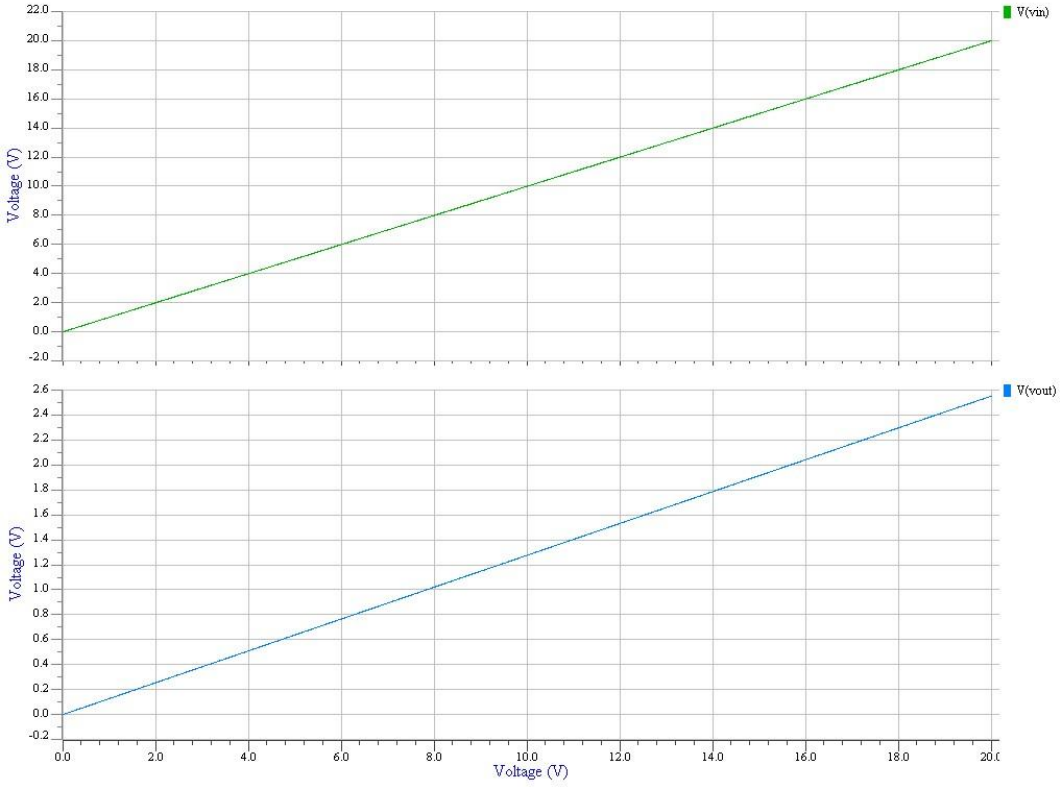


Figure 4.5. Bk1B131C_Voltage_Sensor_V1 simulation.

The sensor has a performance as expected, like we can see at graph to 0 from 20 V at I_IN input, to 0 from 2.5 V is obtained at CS_VOUT output.

4.1.5 – Bk1B1253A_5V_5A_Regulator_V2

To check the regulator behavior, the input signals was set as following picture:

Sources

	Name	Type (V / I)	Node+	Node-	Resistance	DC Value	Freq. Magnitude	Freq. Phase	Time
☑	V1	V	VAL	0		8			None
☑	V2	V	EN_5V	0		5			None
☑	V3	V	DGND	0		0			None
☑	V4	V	VCC_5V	0	1K	0			None

Figure 4.6. Sources.

The output source was set connected to ground through a 1 kΩ resistor.

The simulation results are shown below:

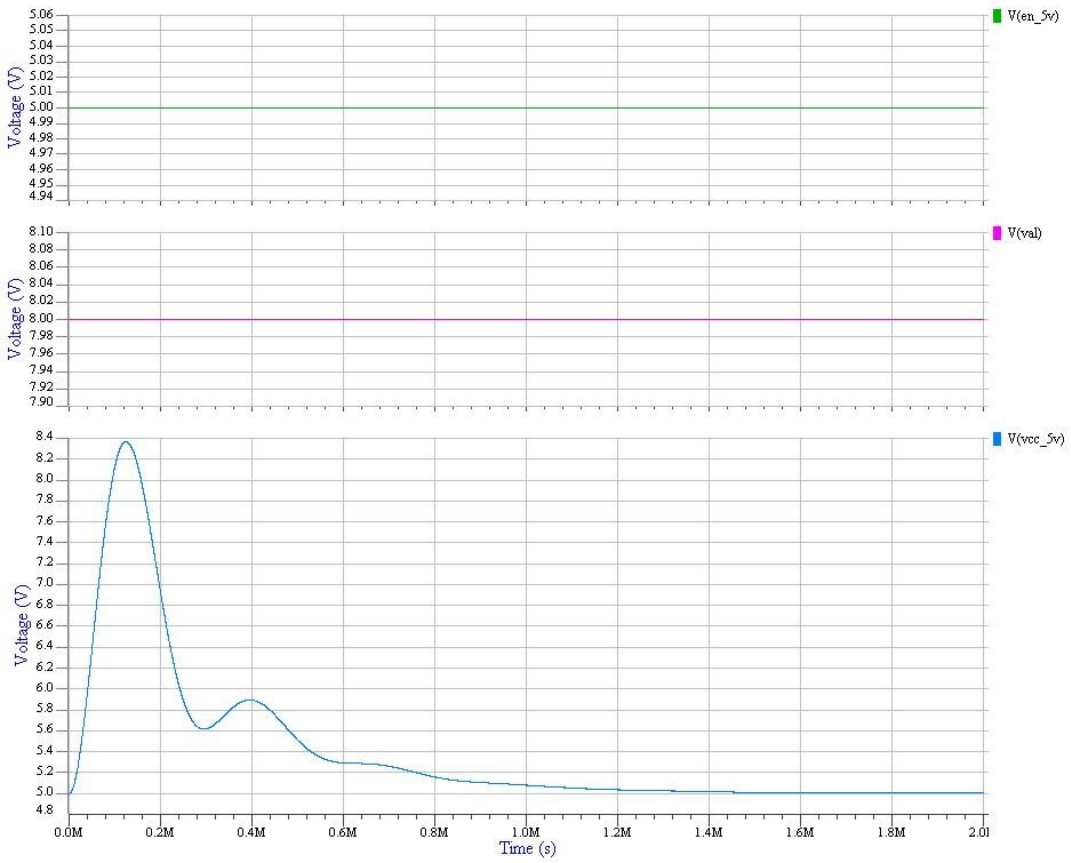


Figure 4.7. Bk1B1253A_5V_5A_Regulator_V2 simulation.

We can see that after a 1.2 milliseconds, approximately, the output voltage achieves the 5 V as is expected.

4.1.6 – Bk1B1254D_3V3_1A6_Mixed_Regulator_V2

The regulators was simulated for several cases, this time is shown the VAL input set as a pulse between 5 V and 20 V. Before, this regulator was checked with a continuous VAL input, and the result was the same output signal.

Input signals:

- $V1 \rightarrow between\ VAL\ and\ 0\ nodes \rightarrow 5V - 20\ V,\ pulse\ source$
- $V2 \rightarrow between\ EN\_3V3\ and\ 0\ nodes \rightarrow 3.3\ V,\ DC\ source$
- $V3 \rightarrow between\ DGND\ and\ 0\ nodes \rightarrow 0\ V,\ DC\ source$
- $V4 \rightarrow between\ VCC\_3V3\ and\ 0\ nodes \rightarrow 0\ V, DC\ source, internal\ resistance: 1k\Omega$

The output source was set connected to ground through a 1 kΩ resistor.

Figure 4.8. Bk1B1254D_3V3_1A6_Mixed_Regulator_V2 simulation.

As we already know, the Bk1B1254D_3V3_1A6_Mixed_Regulator_V2 is composed by two regulators. At graphics above, we can see V(PH) and V(VCC_3V3), the first is the output voltage of the Bk1B1255B_4V_5A_Regulator_V2, and it is working well, because we get 4 V after 1.2 milliseconds, more or less. The second voltage is the Bk1B1254E_3V3_1A6_LDO_Regulator_V1 output, and we can see that it achieves 3.3 V, after 1.5 milliseconds approximately, as it is expected.

4.1.6.1 – Bk1B1255B_4V_5A_Regulator_V2

This time, the 4 V, 5 A regulator behavior is checked. The inputs and the graph results are shown below.

Input signals:

- $V1 \rightarrow between\ VAL\ and\ 0\ nodes \rightarrow 8\,V,\ DC\ source$
- $V2 \rightarrow between\ EN\_4V\ and\ 0\ nodes \rightarrow 4\,V,\ DC\ source$
- $V3 \rightarrow between\ DGND\ and\ 0\ nodes \rightarrow 0\,V,\ DC\ source$
- $V4 \rightarrow between\ VCC\_4V\ and\ 0\ nodes \rightarrow 0\,V, DC\ source, internal\ resistance: 1k\Omega$

The output source was set connected to ground through a 1 kΩ resistor.

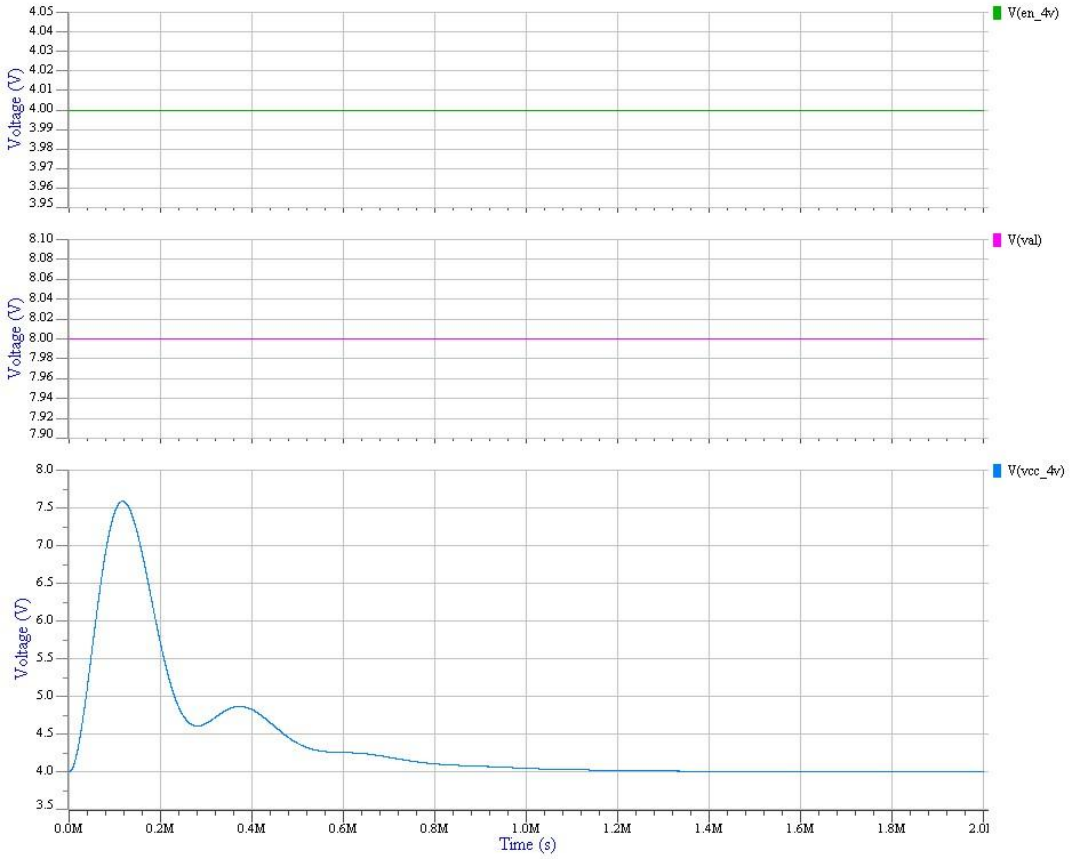


Figure 4.9. Bk1B1255B_4V_5A_Regulator_V2 simulation.

We can see that for the set inputs, the regulator achieves the expected output 4 V, after 1.2 milliseconds, approximately.

4.1.6.2 – Bk1B1254E_3V3_1A6_LDO_Regulator_V1

Now, the 3.3 V, 1.6 A regulator behavior is checked. The inputs and the graph results are shown below.

Input signals:

- $V1 \rightarrow between\ VAL\ and\ 0\ nodes \rightarrow 7\ V,\ DC\ source$
- $V2 \rightarrow between\ EN\_3V3\ and\ 0\ nodes \rightarrow 3.3\ V,\ DC\ source$
- $V3 \rightarrow between\ DGND\ and\ 0\ nodes \rightarrow 0\ V,\ DC\ source$
- $V4 \rightarrow between\ VCC\_3V3\ and\ 0\ nodes \rightarrow 0\ V, DC\ source, internal\ resistance: 1k\Omega$

The output source was set connected to ground through a 1 kΩ resistor.

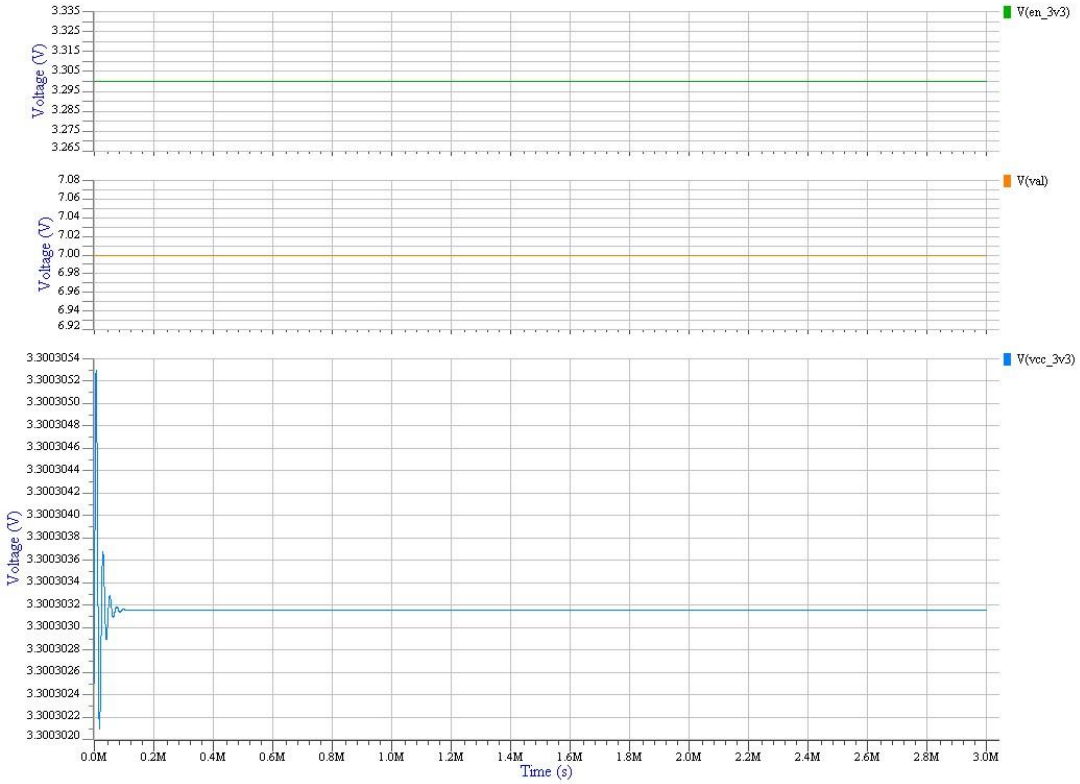


Figure 4.10. Bk1B1254E_3V3_1A6_LDO_Regulator_V1 simulation.

We can see that for the set inputs, the regulator achieves the expected output 3.3 V, after 0.1 milliseconds, approximately.

4.1.7 – Bk1B1252A_3V0_1000ppm_Reference_V1

The last regulator, the reference 3 V voltage is checked. The inputs and the graph results are shown below.

Input signals:

- $V1 \rightarrow between\ VAL\ and\ 0\ nodes \rightarrow 5\ V,\ DC\ source$
- $V2 \rightarrow between\ EN\_REF\ and\ 0\ nodes \rightarrow 5\ V,\ DC\ source$
- $V3 \rightarrow between\ DGND\ and\ 0\ nodes \rightarrow 0\ V,\ DC\ source$
- $V4 \rightarrow between\ REF\_3V\ and\ 0\ nodes \rightarrow 0\ V, DC\ source, internal\ resistance: 1k\Omega$

The output source was set connected to ground through a 1 kΩ resistor.

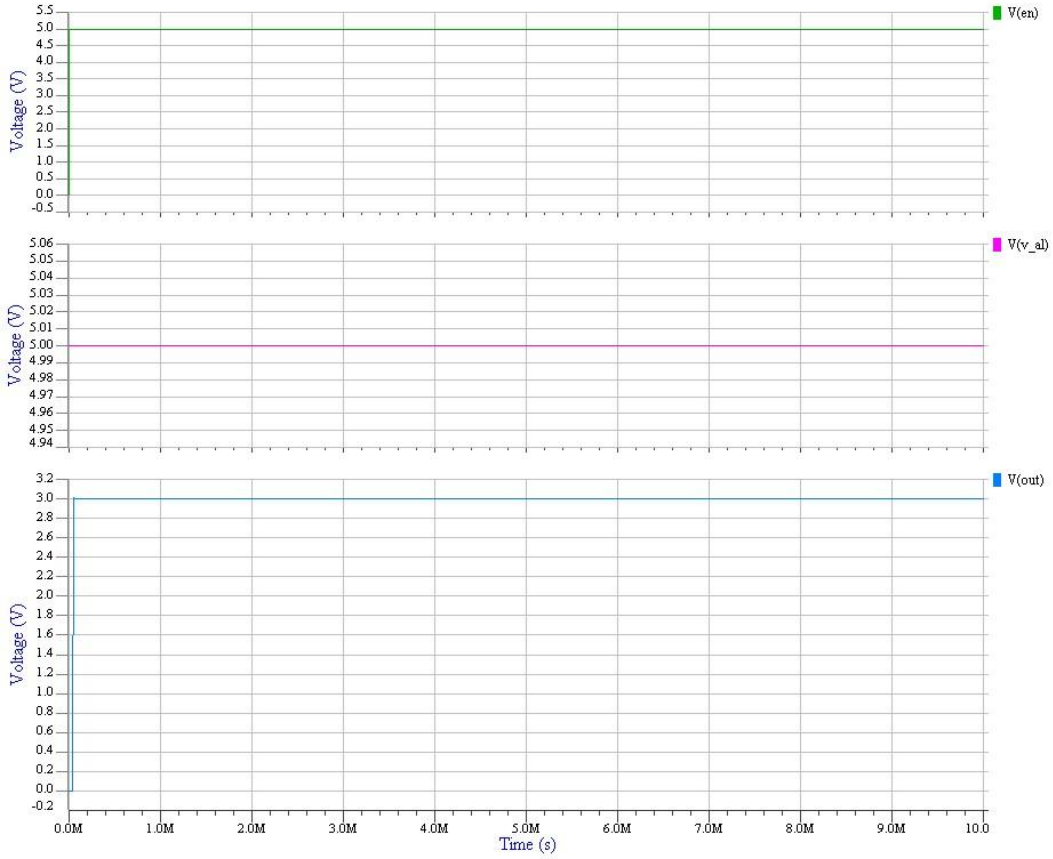


Figure 4.11. Bk1B1252A_3V0_1000ppm_Reference_V1 simulation.

We can see that for the set inputs, the regulator achieves the expected 3 V reference voltage, after 0.1 milliseconds, approximately.

4.1.8 – Bk1B1122_PWM_DC_Converter_V1

PWM to DC Converter is simulated, firstly with DC input source and after with a pulse source, to observe both outputs. The inputs and the graph results are shown below.

Input signals:

- $V1 \rightarrow between\ VCC\_3V3\ and\ 0\ nodes \rightarrow 3.3\ V,\ DC\ source$
- $V2 \rightarrow between\ PWM\_IN\ and\ 0\ nodes \rightarrow 3.3\ V,\ DC\ source$
- $V3 \rightarrow between\ DGND\ and\ 0\ nodes \rightarrow 0\ V,\ DC\ source$
- $V4 \rightarrow between\ DC\_OUT\ and\ 0\ nodes \rightarrow 0\ V, DC\ source, internal\ resistance: 1k\Omega$

The output source was set connected to ground through a 1 kΩ resistor.

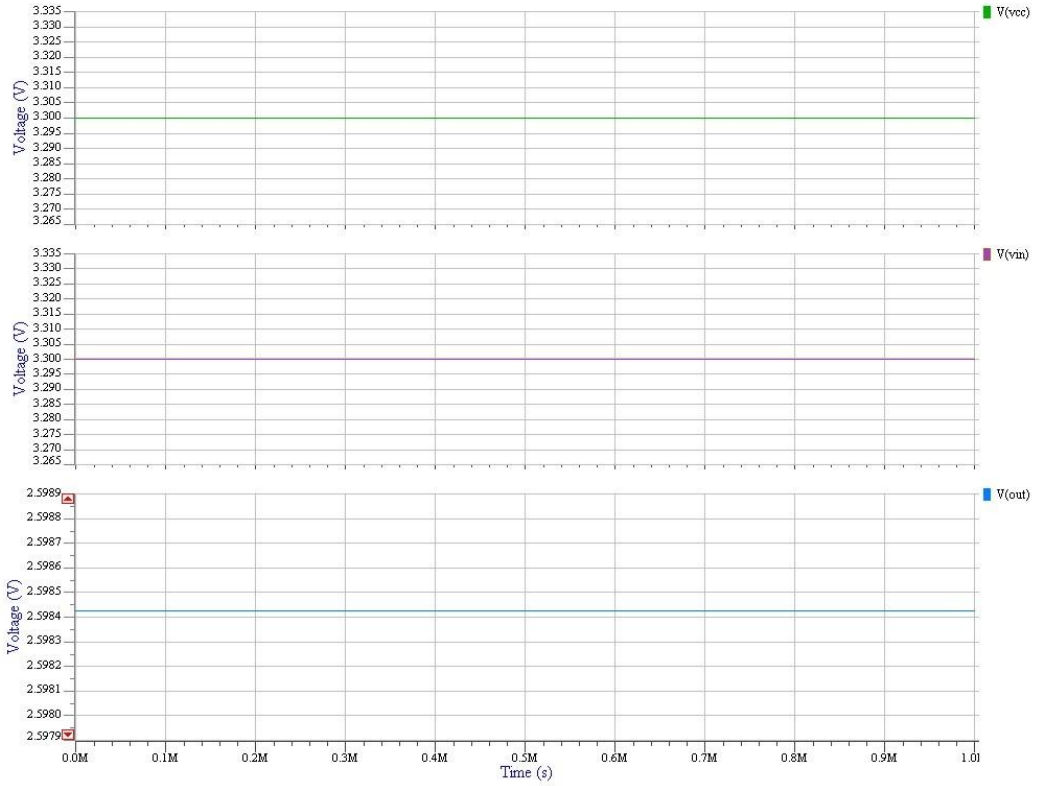


Figure 4.12. Bk1B1122_PWM_DC_Converter_V1 simulation with DC source.

We can observe a 2.6 V output voltage as it was explained at chapter 3 at points 3.1.5 1B1122_PWM_DC_Converter_V1 and 3.5 – Future improvements. For a PWM_IN set to 0 V, the same output is obtained.

The simulation graphs with a pulse input source are shown below.

Input signals:

- $V1 \rightarrow between\ VCC\_3V3\ and\ 0\ nodes \rightarrow 3.3\ V,\ DC\ source$
- $V2 \rightarrow between\ PWM\_IN\ and\ 0\ nodes \rightarrow 0\ V - 1\ V,\ pulse\ source, D.C.: 50\%$
- $V3 \rightarrow between\ DGND\ and\ 0\ nodes \rightarrow 0\ V,\ DC\ source$
- $V4 \rightarrow between\ DC\_OUT\ and\ 0\ nodes \rightarrow 0\ V, DC\ source, internal\ resistance: 1k\Omega$

The output source was set connected to ground through a 1 kΩ resistor.

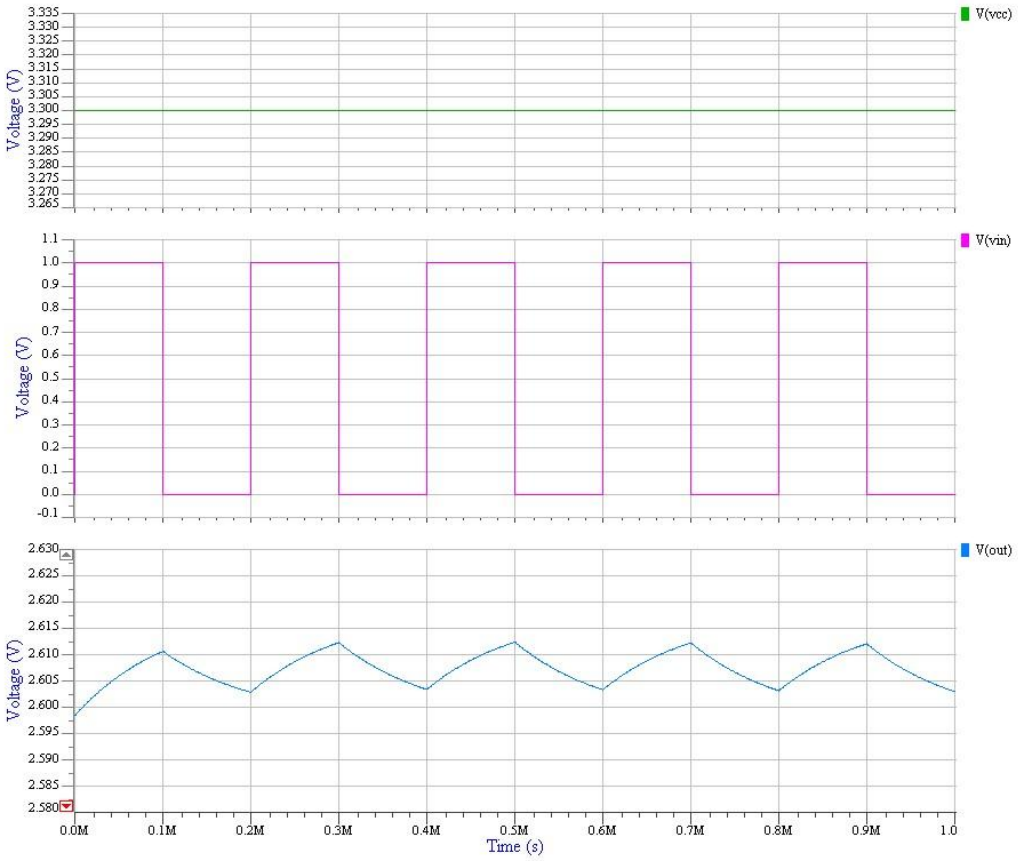


Figure 4.13. Bk1B1122_PWM_DC_Converter_V1 simulation with pulse source.

This time, the output suffers raises and drops following the input pulse signal. Anyway the output voltage is a good constant DC output.

As it is known, at points 3.1.5 and 3.5 of the chapter 3, a deeper study of this block is done. At this point, two examples are shown at above graphs.

4.1.9 – Bk1B1121C_MPPT_V1

MPPT block is simulated plugging the SOLAR_POS to the VIN pin and the PWM_DC_Converter output connected to the VREF input pin. Moreover, the rest of inputs are set as sources as is shown below.

The output of the PWM to DC Converter is a signal almost lineal around 2.6 V, it is directly connected to the negative input of the OA MAX975, used as comparator. The positive input of the comparator is the SOLAR_POS signal after pass a resistor divider. These signals are plotted at the following graphs.

Input signals:

- $V1 \rightarrow between\ Disable\ and\ 0\ nodes \rightarrow 0\,V,\ DC\ source$
- $V2 \rightarrow between\ DGND\ and\ 0\ nodes \rightarrow 0\,V,\ DC\ source$
- $V3 \rightarrow between\ VOUT\ and\ 0\ nodes \rightarrow 0\,V, DC\ source, internal\ resistance: 6.5\ \Omega$

The output source was set connected to ground through a 6.5 Ω resistor.

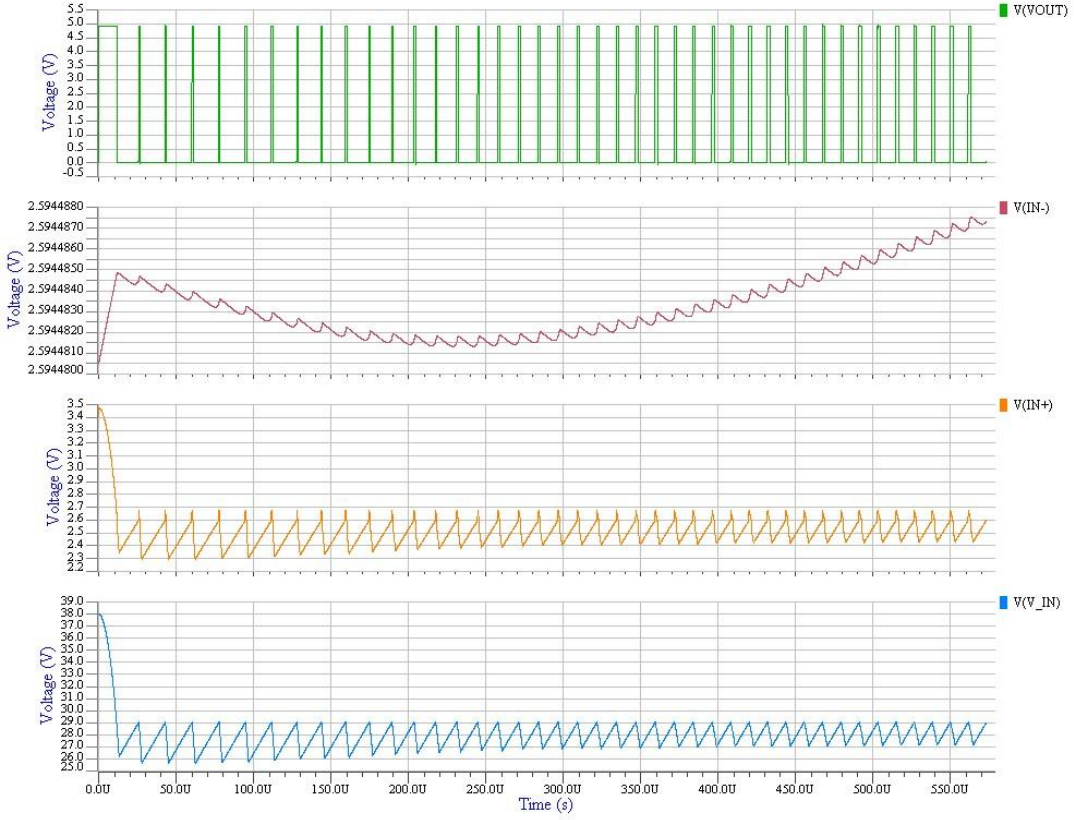


Figure 4.14. Bk1B1121C_MPPT_V1 simulation.

Explaining these signals, the blue one is the SOLAR_POS voltage coming from the solar cells, V(V_IN). The orange one, V(IN+), is the SOLAR_POS voltage after through the resistor divider and the violet one is the PWM to DC Converter output, V(IN-). Finally, the green one is the output of the comparator. At graph below we can see a deeper analysis.

Doing a zoom at the positive and negative inputs and the output of the comparator, we can see the following plot.

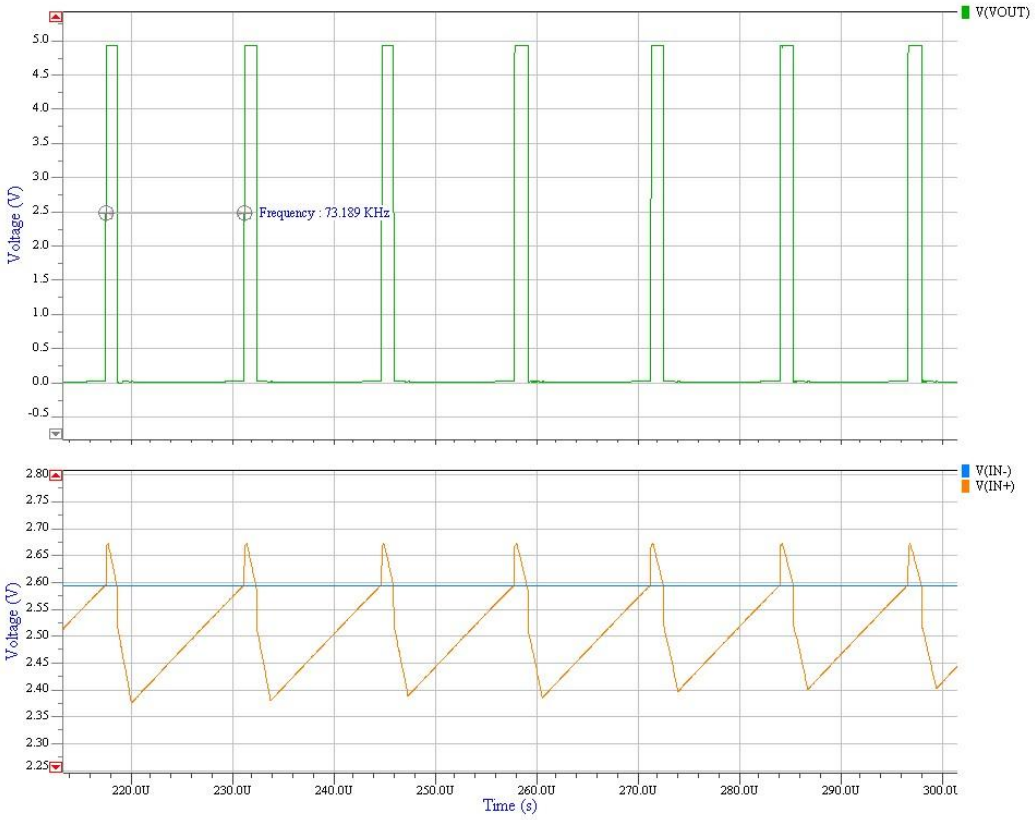


Figure 4.15. Bk1B1121C_MPPT_V1 simulation zoom.

Observing the input signals, the negative one is a lineal voltage of 2.6 V, as it is explained previously. The positive one is a particular triangular wave between 2.35 V and 2.70 V at our case.

The output voltage is a pulse, when the positive input is greater than the negative one, the output raises until 5 V approximately, it is the comparator supply by the Bk1B1121C_LowPowerReg. At the other case, the negative input is greater than the positive one, the output will be 0 V.

At our case, for this SOLAR_POS signal, this PWM to DC Converter output signal and the rest input signals set, the frequency of the output is around 73 kHz. To change the output voltage, the following input modifications are possible to set:

- Change the SOLAR_POS, to observe different scenarios, for example when increases and decreases the insolation.
- Change the duty cycle of the PWM to DC Converter, to vary the output of this block, and carrying the change to the MPPT.
- Change the MPPT load value, to see several cases.

To finish the study of the MPPT block, we can observe the output voltage and the current traversing the 6.5 Ω load.

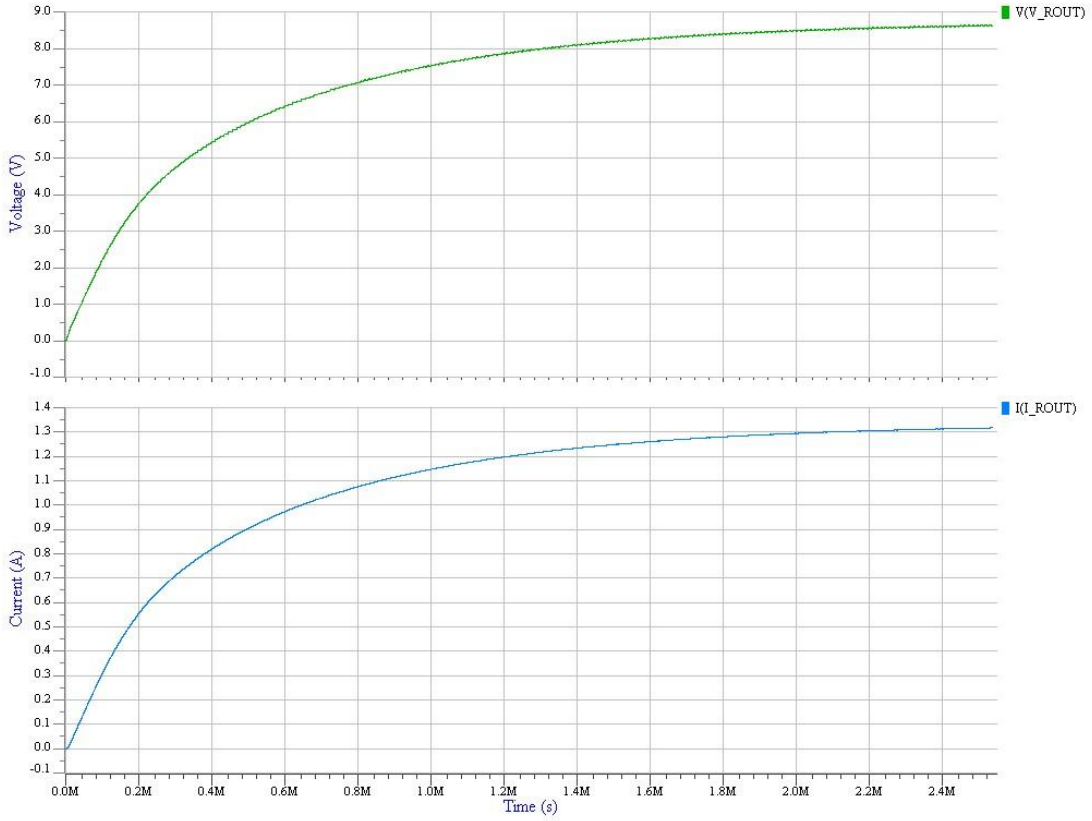


Figure 4.16. Bk1B1121C_MPPT_V1 simulation, R_OUT voltage and current.

We can check the similarity of the V(V_ROUT) signal with the waves at graph of all PDB voltages, at point 3.5 – Future improvements of the chapter 3. At our case, the MPPT output voltage is at range of voltages as we expected. Note the difference that at point 3.5 of the chapter 3, the voltages are for a 10 Ω load, and in our case the load is equal to 6.5 Ω.

The current through of the MPPT load resistor is plotted at the above figure.

To view the schematic of the MPPT go to Appendix A.

4.1.9.1 – Bk1B1121C_LowPowerReg_V1

To conclude this point, the reference 5 V voltage is checked. The inputs and the graph results are shown below.

Input signals:

- $V1 \rightarrow between\ V\_IN\ and\ 0\ nodes \rightarrow 0\ V - 40\ V,\ pulse\ source$
- $V2 \rightarrow between\ DGND\ and\ 0\ nodes \rightarrow 0\ V,\ DC\ source$
- $V3 \rightarrow between\ V\_OUT\ and\ 0\ nodes \rightarrow 0\ V, DC\ source, internal\ resistance: 1k\Omega$

V1 has this pulse source to check if at the input range of the regulator, it has a good behavior.

The output source was set connected to ground through a 1 kΩ resistor.

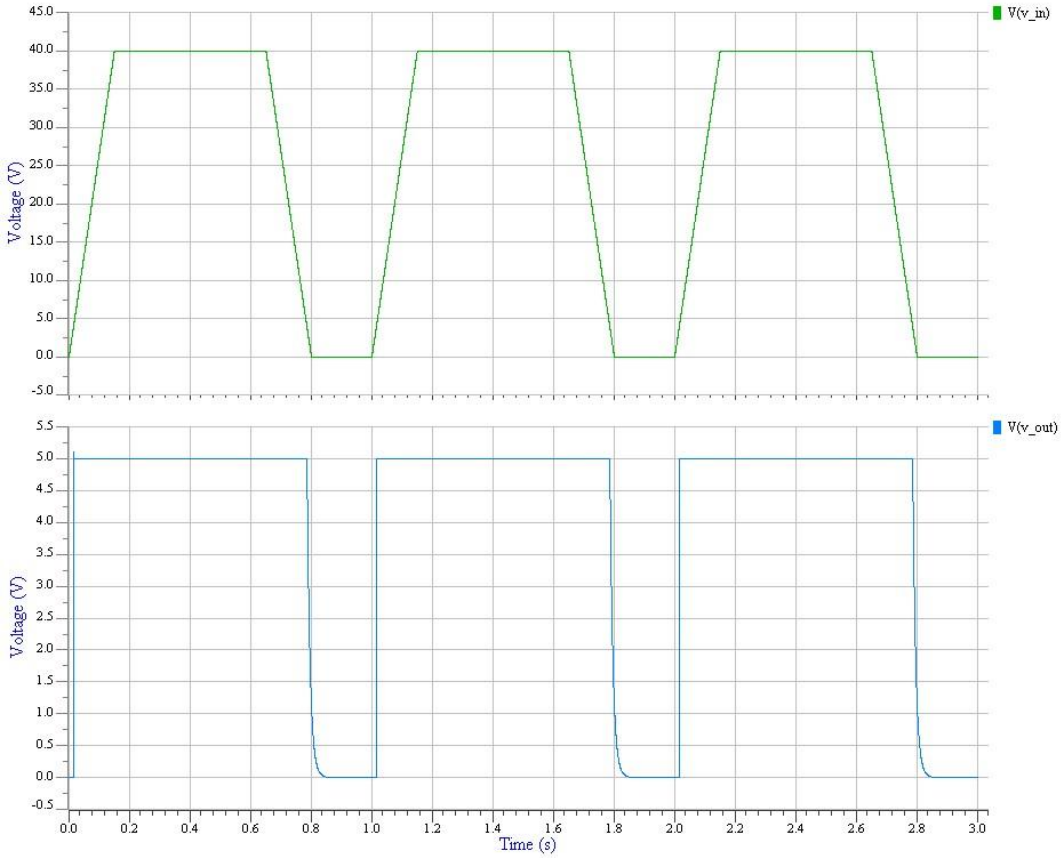


Figure 4.17. Bk1B1121C_LowPowerReg_V1 simulation.

We can see that for the set inputs, the regulator achieves the expected voltage equal to 5 V.

Also, for the input voltage range is checked that the regulator has a good performance, raising to 5 V output voltage.

4.2 – 1B1121C_Primary_Switching_Buck_V2 simulation

Once checked the good behavior of the all subsystems, the primary switching buck is ready to be simulated.

The following are the inputs source set for the simulation:

- $V1 \rightarrow between\ EN\_5V\ and\ 0\ nodes \rightarrow 5\,V,\ DC\ source$
- $V2 \rightarrow between\ EN\_3V3\ and\ 0\ nodes \rightarrow 3.3\,V,\ DC\ source$

The solar cells was plugged to the SOLAR_POS and SOLAR_NEG input pins.

These four input signals are plotted at following figure.

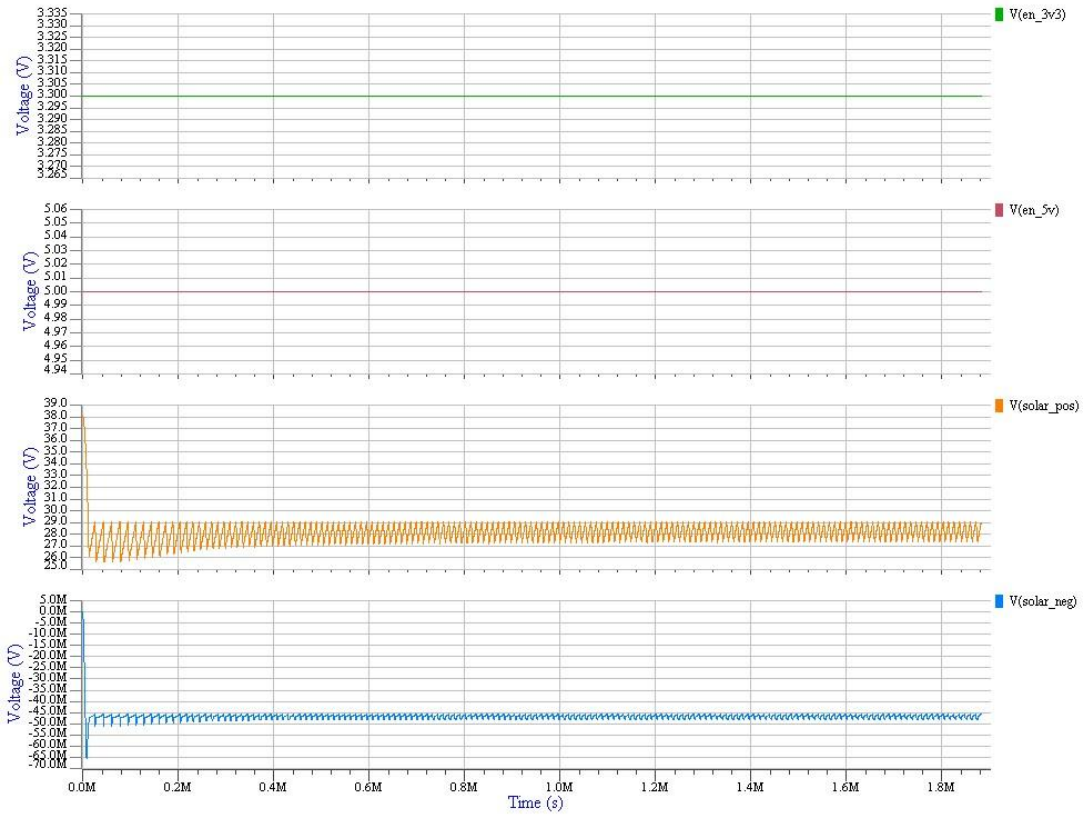


Figure 4.18. Input signals.

Also this source is connected:

- $V3 \rightarrow between\ PDB\ and\ 0\ nodes \rightarrow 0\,V, DC\ source, internal\ resistance: 6.5\ \Omega$

The output source was connected to ground through a 6.5 Ω resistor.

The graph below shown the inputs and outputs of the PWM to DC Converter and the MPPT.

- V(n1n213) is the output voltage, DC_OUT, of the PWM to DC Converter , green wave.
- The orange signal is the SOLAR_POS.
- The Disable and PWM_IN inputs are set as 0 V sources, light and dark blue, respectively. The PWM_IN is set as explained because at the physical Honeycomb Tile, this input is set from the microprocessor with 0 V.
- V(n_1n214) is the voltage at VOUT pin of the MPPT. V(PDB) is the same voltage of V(n_1n214) after pass a current sensor. Both signals are almost equal.

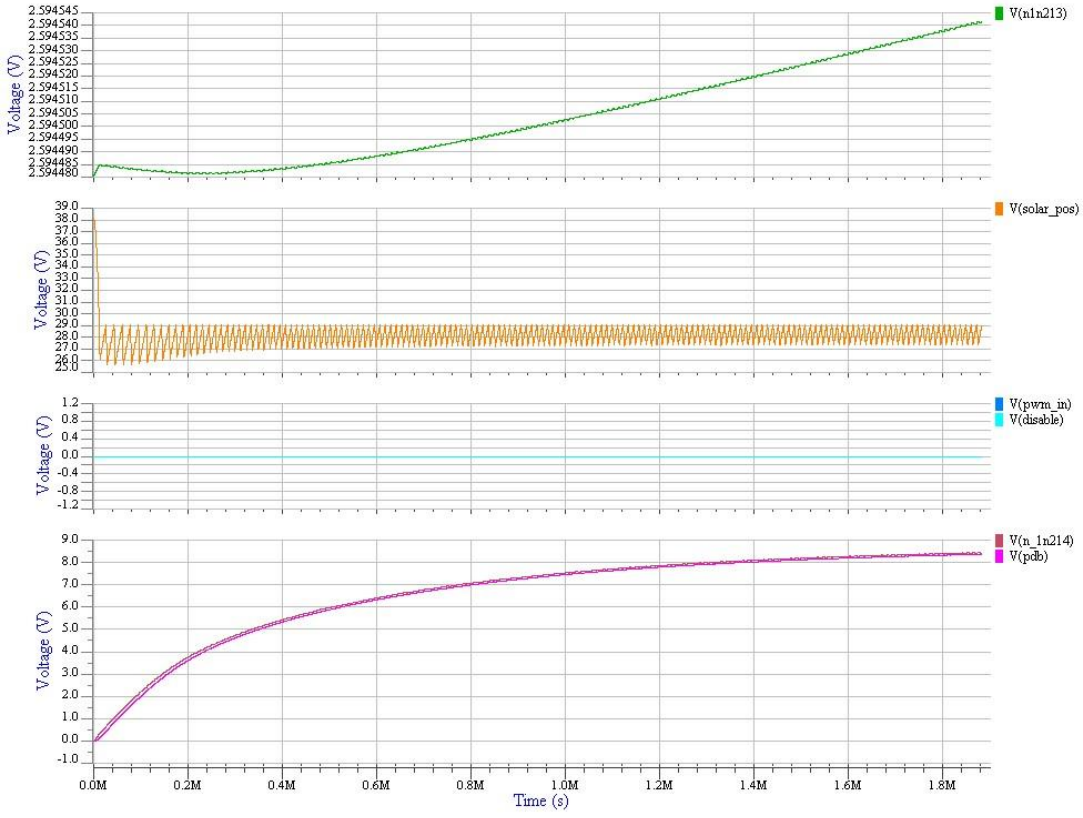


Figure 4.19. Input and output PWM to DC Converter and MPPT signals.

Following, the area of interest of the primary switching buck is shown, to understand better all waves plotted above.

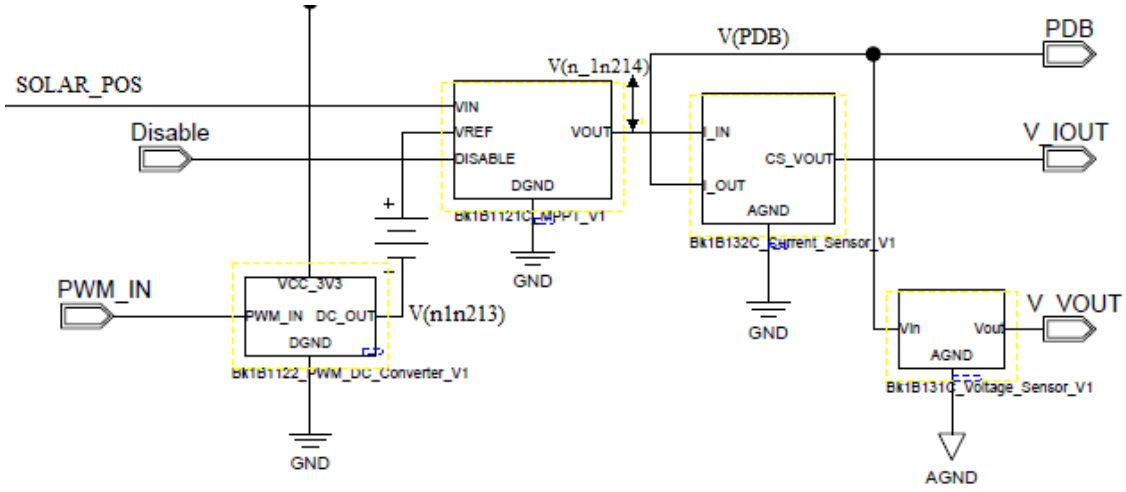


Figure 4.20. Interesting area of the primary switching buck.

Now, the four voltage outputs are plotted, these are: VCC_5V, VCC_3V3, REF_3V and PBD.

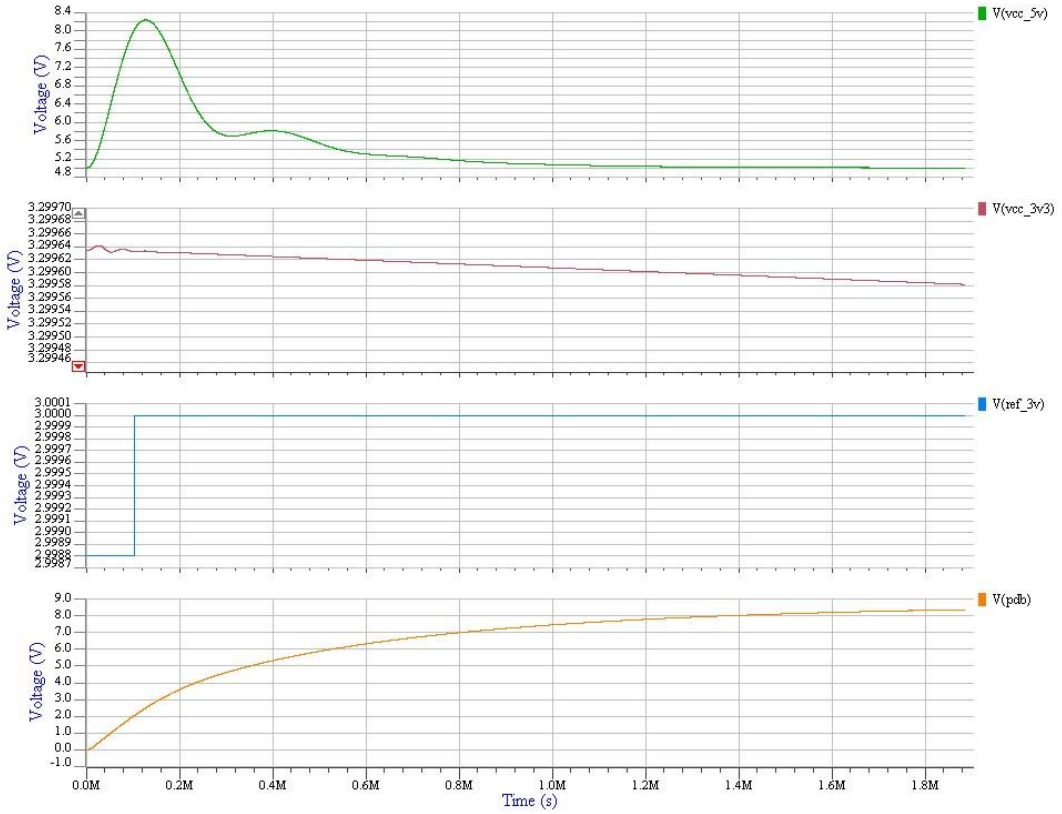


Figure 4.21. Output voltages.

As the voltages of the blocks simulated one by one, the voltages are achieved by plugging all the required inputs and solar cells.

To finish this point, the sensor outputs are shown below.

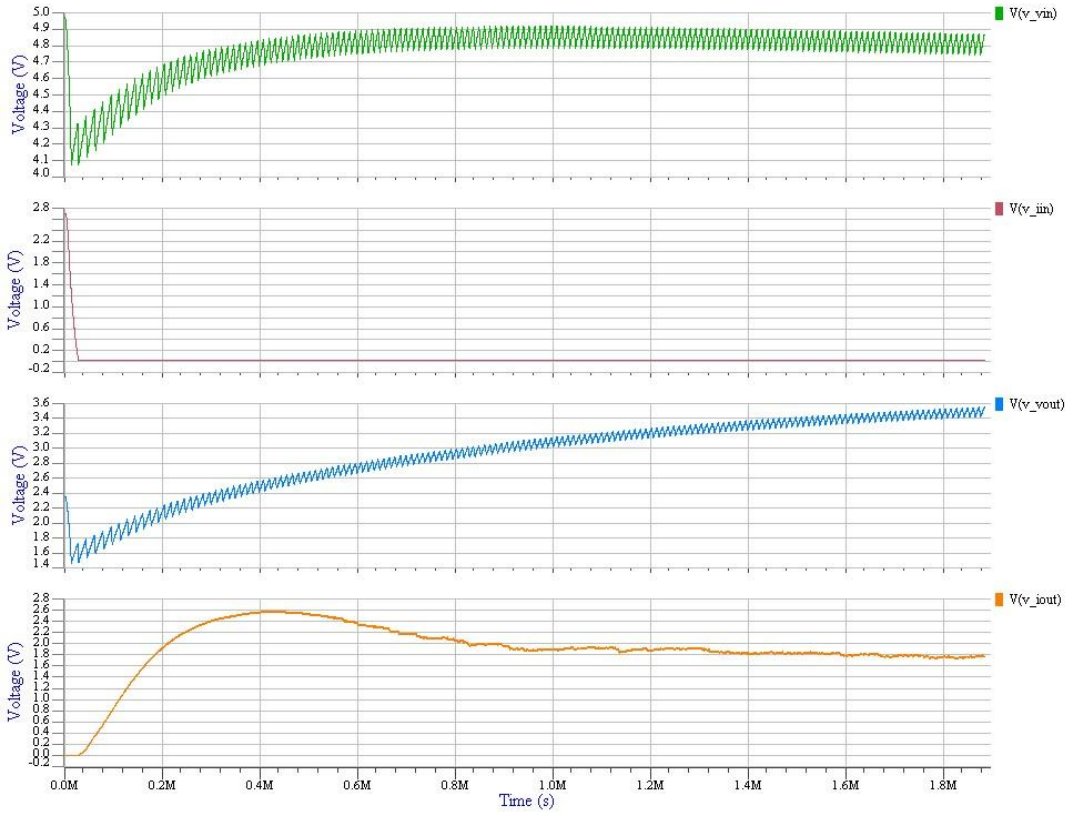


Figure 4.22. Sensor outputs.

Just comment that, more simulations with another input sources and another load values have been done, but these have not been shown at the thesis for not make it too much longer.

4.3 – Ripple of regulators

Ripple of 5 V regulator TPS5450

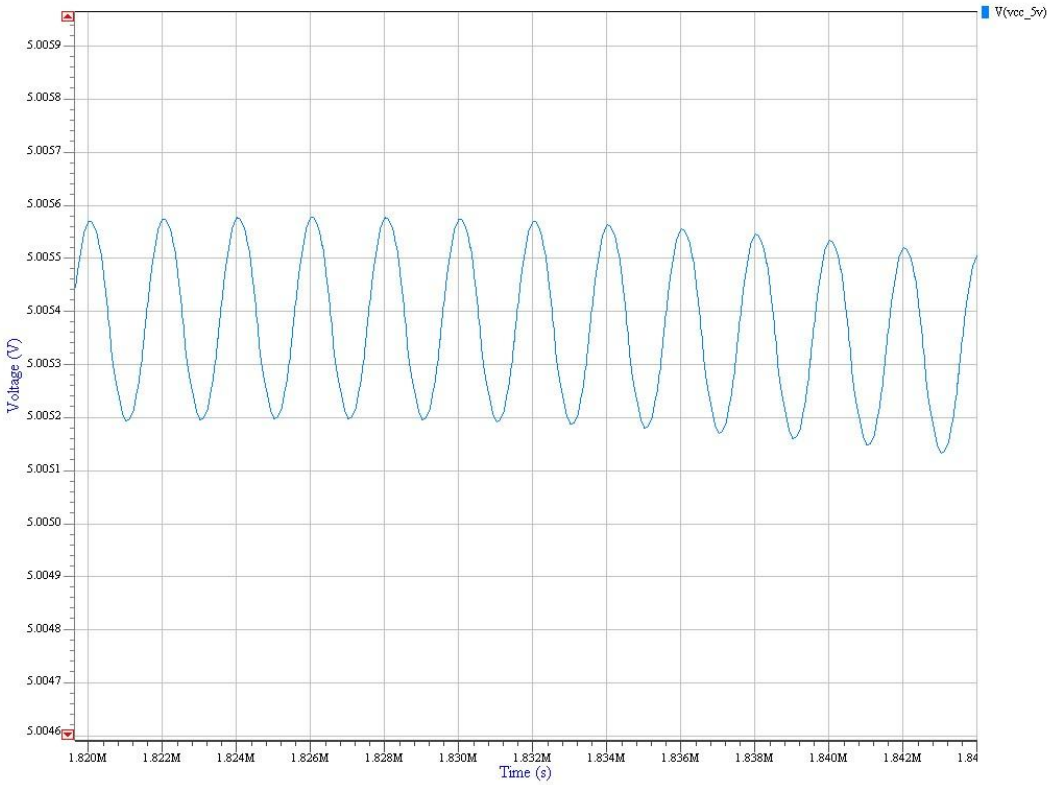


Figure 4.23. Ripple of 5 V regulator.

To calculate the peak to peak output ripple voltage, the following datasheet equations are used:

The closed-loop crossover frequency is:

$$f_{CO} = \frac{{f_{LC}}^2}{85 \times V_{OUT}} \text{; where } f_{LC} \text{ is: } f_{LC} = \frac{1}{2\pi \times \sqrt{LC}}$$

For $L = 15\ \mu H$ and $C = 220\ \mu F$, is obtained $f_{LC} \approx 2770$ Hz and $f_{CO} \approx 18$ kHz.

With these values, the peak to peak ripple voltage is:

$$V_{PP}(MAX) = \frac{ESR_{MAX} \times V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{N_C \times V_{IN(MAX)} \times L_{OUT} \times F_{SW}} \text{; where } ESR_{MAX} \text{ is: } ESR_{MAX} = \frac{1}{2\pi \times C_{OUT} \times f_{CO}}$$

Then: $ESR_{MAX} \approx 0.04$ and the $V_{p\text{-}p}(MAX) \approx 23$ mV

• N_C is the number of output capacitors in parallel. In our case $N_C = 1$.

• F_{SW} is the switching frequency. In our case $F_{SW} = 500$ kHz.

• $V_{IN(MAX)} = 36$ and $V_{OUT} = 5V$.

Finally the ripple is the following.

Output ripple voltage (calculated of equations from datasheet) = 23 mV_{p-p}

Output ripple voltage at simulation = 0.350 mV_{p-p}

Output ripple voltage (calculated of equations from datasheet) = 8.132 mV_{RMS}

Output ripple voltage at simulation = 0.124 mV_{RMS}

Ripple of 4 V regulator TPS5450

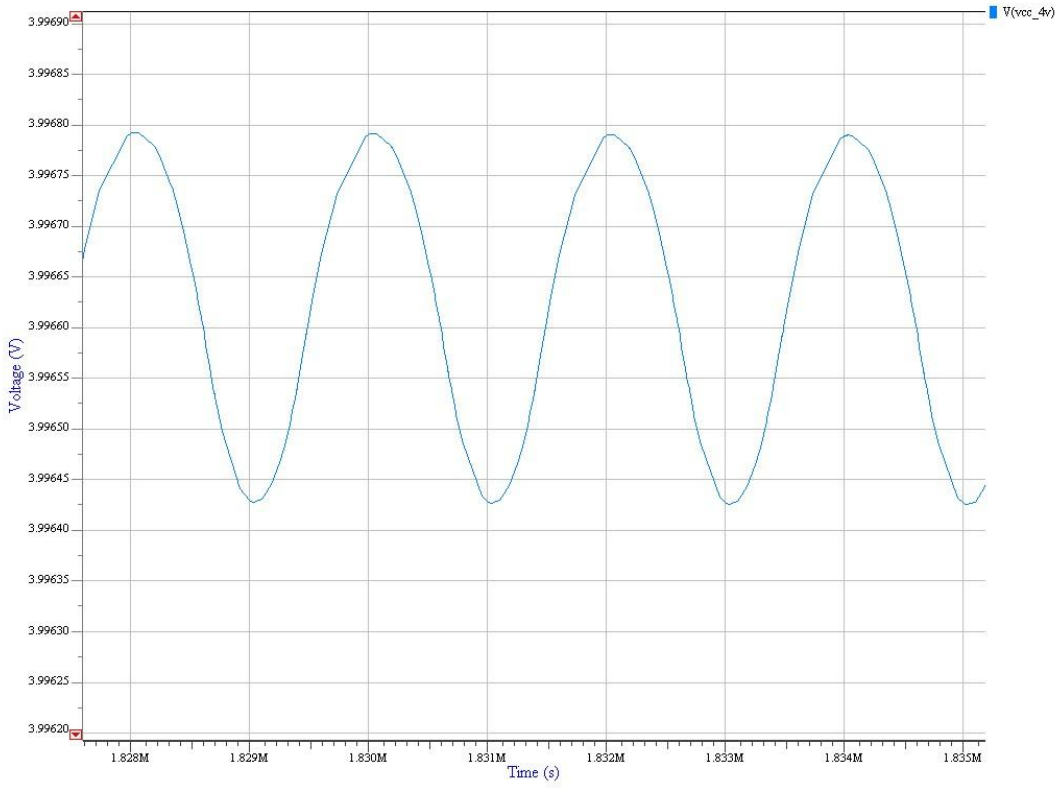


Figure 4.24. Ripple of 4 V regulator.

To calculate the peak to peak output ripple voltage, the following datasheet equations are used:

The closed-loop crossover frequency is:

$$f_{CO} = \frac{{f_{LC}}^2}{85 \times V_{OUT}}\text{; where } f_{LC} \text{ is: } f_{LC} = \frac{1}{2\pi \times \sqrt{LC}}$$

For L = *15 µH* and *C = 220 µF*, is obtained $f_{LC} \approx 2770$ Hz and $f_{CO} \approx 22.5$ kHz.

With these values, the peak to peak ripple voltage is:

$$V_{PP}(MAX) = \frac{ESR_{MAX} \times V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{N_C \times V_{IN(MAX)} \times L_{OUT} \times F_{SW}}\text{; where } ESR_{MAX} \text{ is: } ESR_{MAX} = \frac{1}{2\pi \times C_{OUT} \times f_{CO}}$$

Then: $ESR_{MAX} \approx 0.032$ and the $V_{p\text{-}p}(MAX) \approx 15.2$ mV

• N_C is the number of output capacitors in parallel. In our case $N_C = 1$.

• F_{SW} is the switching frequency. In our case $F_{SW} = 500$ kHz.

• $V_{IN(MAX)} = 36$ and $V_{OUT} = 4$V.

Finally the ripple is the following.

Output ripple voltage (calculated of equations from datasheet) = 15.2 $mV_{p\text{-}p}$

Output ripple voltage at simulation = 0.370 $mV_{p\text{-}p}$

Output ripple voltage (calculated of equations from datasheet) = 5.374 mV_{RMS}

Output ripple voltage at simulation = 0.131 mV_{RMS}

Ripple of 3.3 V regulator LT 1963

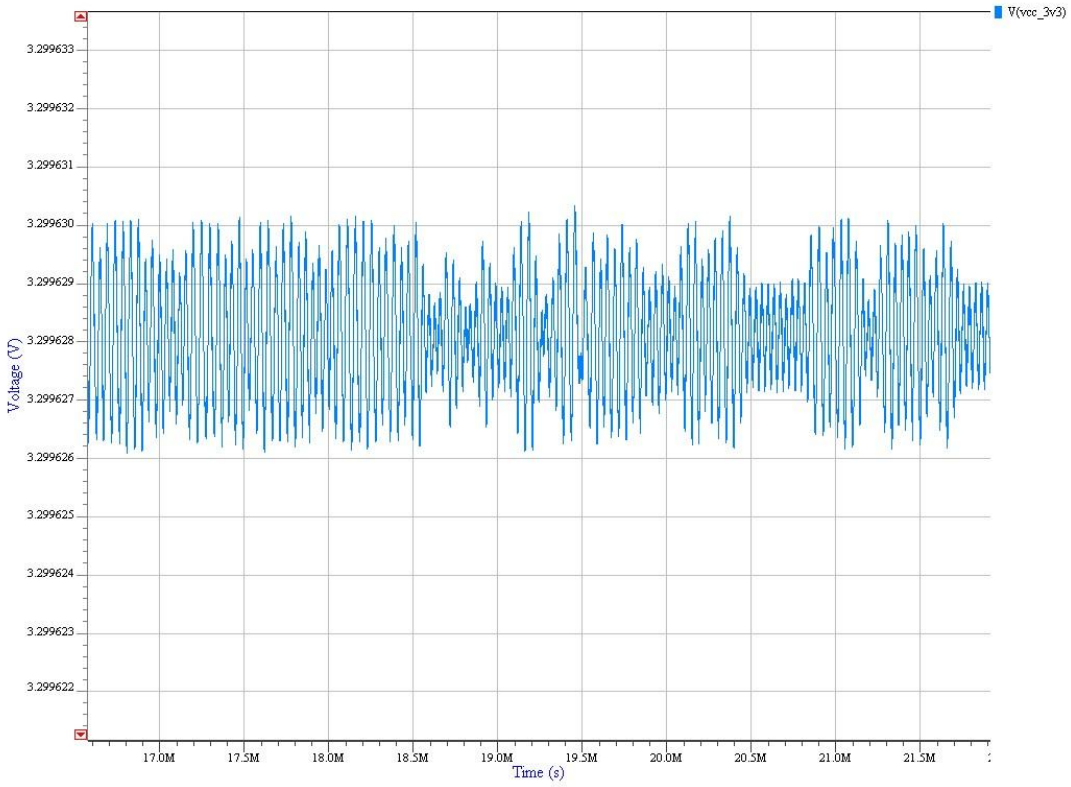


Figure 4.25. Ripple of 3.3 V regulator.

The output ripple voltage of the LT 1963 regulator is taken of the datasheet:

Output ripple voltage (datasheet) = 113.14 μV_{p-p}

Output ripple voltage at simulation = 4 μV_{p-p}

Output ripple voltage (datasheet) = 40 μV_{RMS}

Output ripple voltage at simulation = 1.414 μV_{RMS}

Ripple of 3 V regulator LM4128

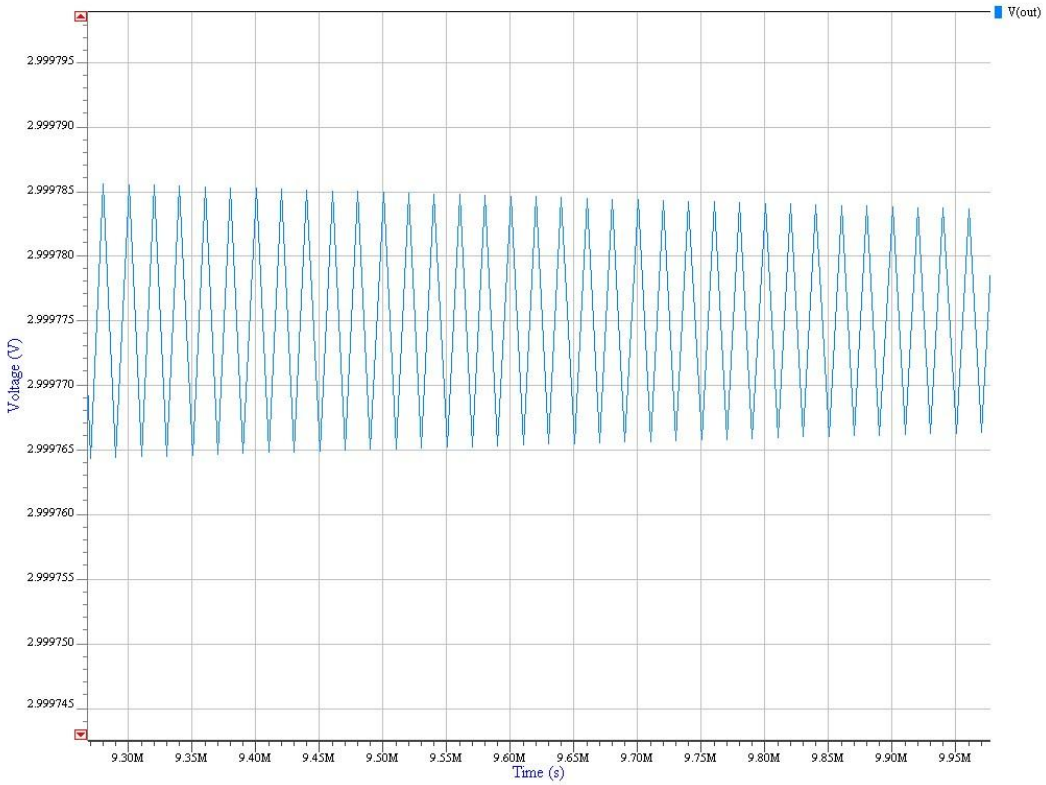


Figure 4.26. Ripple of 3 V regulator.

The output ripple voltage of the LM4128 regulator is taken of the datasheet:

Output ripple voltage (datasheet) = 285 μV_{p-p}

Output ripple voltage at simulation = 16 μV_{p-p}

Output ripple voltage (datasheet) = 100.763 μV_{RMS}

Output ripple voltage at simulation = 5.657 μV_{RMS}

Chapter 5

Testing 1B81_Power_Management_Honeycomb

Once, the theoretical study is done, the simulation problems are solved, and the simulations to check the system behavior are realized, it is time to test the Power Management Honeycomb.

This test was carried out following some steps:

- Firstly, to identify all components of the PCB, understanding where the subsystems were located and paying attention to the electrical connections of the integrated components.

- Then, to check with a multimeter if the voltage levels were achieved. Connecting a voltage supply, the 5 V, 4 V, 3.3 V and 3 V were got.

- Now, the solar cell simulator was plugged. Firstly, a 38 V and 0.482 A power supply was connected directly to the solar cell simulator, but this system did not work well at high frequency. For that, a 56 V and 0.482 A power supply was connected to the solar cell simulator through to a 50 Ω input resistor, to achieve a good behavior. A deeper study is done at point 6.2 – Testing PDB of this chapter.

- At this point, doing some measurements and due that a power supply of the laboratory did not working good, 5 V regulator was burnt. The power supply sometimes changes automatically the voltage, passing from 6 V to 30 V, among other strange behaviors. Before change the regulator, the microprocessor MSP430 was programmed with the enable input of the regulator as high impedance, to check if this was really burnt. After these tests, the TPS5450 regulator was changed, and the 5 V was obtained again. From now, another power supply was used.

- With both power supplies and the solar cell simulator connected, some expected voltage values were not achieved. These voltage differences with the simulation values were located at the PWM to DC Converter output, DC_OUT, and consequently at the MPPT. Mainly, around 2.6 V were expected at DC_OUT, but instead of this value, about 0.8 V or 0.9 V were got. Several checks to find the problem were done: the voltages of PWM to DC Converter and MPPT were checked with the multimeter and with the oscilloscope for several input signals, the value of the resistors was made sure by observing the code printed at top of them, also it was checked with the multimeter, and the layout of the Power Management Honeycomb was consulted to view the electrical connections. Once done that, we realized that the C20 capacitor and R56 resistor at schematic and at the PCB were soldered in reverse order. The first step to try get 2.6 V at DC_OUT, was change some resistors. After replacing them, were checked the voltage values, but these were the same. The second step was change the OA MAX975EUA. After done, 2.6 V were achieved and the MPPT working well. Now, the Power Management Honeycomb is ready to start the tests.

- To view the 5 V regulator behavior, the programmable load was connected to the VCC_5V output, and letting the rest of outputs without load connection. The maximum load is set, 500 Ω, and the value is decreased until the current is near to the maximum or the temperature of the regulator is too high. The measurements can be found along this chapter.

- To observe the 3.3 V regulator performance, the programmable load was plugged to the VCC_3V3 output, and letting the rest of outputs without load connection. The maximum load is set, 500 Ω, and the value is decreased until the current is near to the maximum or the temperature of the regulator is too high. The measurements can be found along this chapter.

- To check the PDB voltage, a power resistor was connected, because without this, to burn the Power Management Honeycomb was possible. To calculate the maximum value of power resistor, a several kind of that were connected, and letting the rest of outputs without load connection. Firstly, with a 6.8 Ω power resistor connected, around 9 V at PDB was achieved. Between 18 V – 20 V at PDB was the maximum voltage level searched. Then 22 Ω power resistor was connected, and around 16.5 V were achieved. Finally, with 33 Ω power resistor, around 19 V were reached. Then, starting the tests from 33 Ω as maximum power resistor, the programmable load was connected in parallel with this, to do the measurements. A deeper study has been done at this chapter.

- To characterize the 3 V reference voltage, knowing that the maximum current output is 20 mA and connecting the programmable output, letting the rest of outputs without load connection, the range of load values is calculated as: $R = \frac{V}{I} = \frac{3V}{20mA} = 150\Omega$. Then several values between 500 Ω and 150 Ω were done. The measurements can be found along this chapter.

- Finally, the ripple of the regulators was calculated, other measurements were done and some photos with the thermal camera were taken.

The laboratory equipment used for the measurements are attached at the Appendix C.

5.1 – Testing regulators

A study of regulators and their behavior was done.

5.1.1 – Testing 5V regulator

At the next table is shown the input and output voltage and current. For testing the 5 V regulator is connected the supply voltage to the Honeycomb. Between the 5 V output and GND is plugged the programmable load to calculate the different voltages and currents changing its value.

The digital ammeter calculates the input current, I_IN at the table. The digital voltmeter calculates the output voltage, V_OUT. The programmable load had an internal multimeter which calculated the voltage, current and power at the load, V_ROUT, I_ROUT and P_ROUT.

Rw represents the resistance of the wires, this becomes important when the load has a small value.

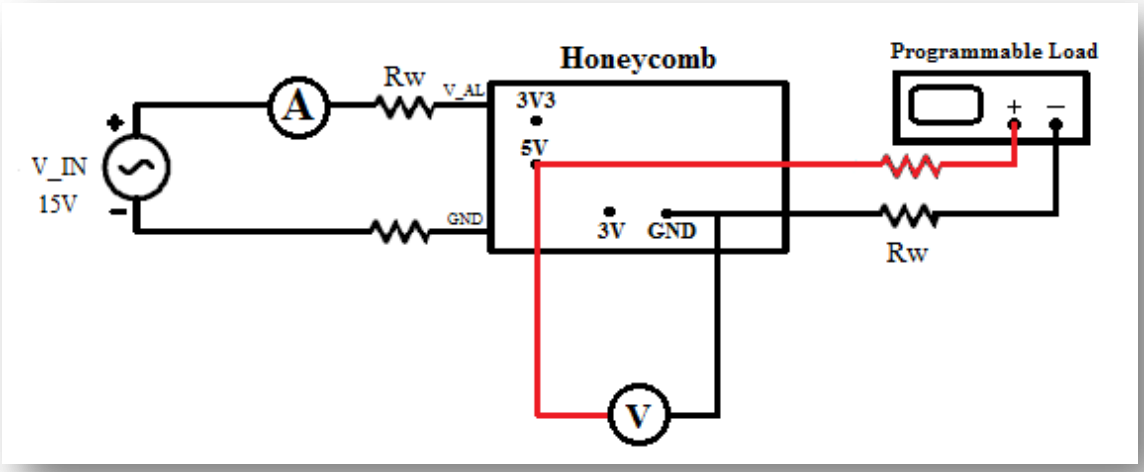


Figure 5.1. 5V regulator connections.

The input current of the power supply was limited to 3.5 A to assure not exceed the 5 A. We can observe how more input current is required when the load value is decremented.

At the load, we can see the same behavior as the current at the input, and when the load takes a small values, it cannot raises the 5 V.

The T(ºC) column corresponds with the temperature of the TPS5450 regulator.

At the measurements of this regulator the smaller load value achieved was 1 Ω, and it was not decremented for two reasons: one, the output current was close to 5 A, and two, the temperature of the regulator was high.

A second table is included with the input and output power calculated and the efficiency.

A third table is shown with the wire resistance measured, when the drop voltage was important, because its value was as the load.

R(Ω)	V_IN(V)	I_IN(mA)	V_OUT(V)	I_ROUT(mA)	V_ROUT(V)	P_ROUT(W)	T(ºC)
500	15	3.94	5.00	10	5.04	0.1	30.0
400	15	4.84	5.00	12	5.04	0.1	30.2
350	15	5.74	5.00	14	5.03	0.1	31.0
300	15	6.37	5.00	16	5.03	0.1	31.1
250	15	7.68	5.00	20	5.03	0.1	31.3
200	15	9.55	5.00	25	5.03	0.1	31.7
150	15	11.74	5.00	33	5.03	0.2	31.8
100	15	18.03	5.00	50	5.03	0.3	32.0
75	15	25.13	5.00	67	5.03	0.3	32.1
50	15	37.35	5.00	100	5.03	0.5	32.3
40	15	45.31	5.00	125	5.03	0.6	32.4
30	15	62.34	5.00	167	5.03	0.8	32.5
20	15	88.04	5.00	250	5.01	1.3	32.7
15	15	122.65	5.00	334	5.01	1.7	32.8
12	15	151.72	5.00	417	5.01	2.1	32.8
10	15	182.06	5.00	498	4.98	2.5	32.9
9	15	202.19	5.00	553	4.98	2.8	33.0
8	15	226.35	5.00	623	4.98	3.1	33.5
7	15	258.88	5.00	712	4.98	3.5	33.9
6	15	300.98	5.00	826	4.95	4.1	35.5
5.5	15	328.85	5.00	901	4.95	4.5	36.2
5	15	362.60	5.00	991	4.95	4.9	36.5
4.5	15	401.16	5.00	1095	4.93	5.4	37.7
4	15	450.39	5.00	1232	4.93	6.1	38.5
3.5	15	517.38	5.00	1401	4.90	6.9	38.8
3	15	604.30	5.00	1625	4.87	7.9	39.6
2.5	15	724.08	5.00	1940	4.85	9.4	40.5
2	15	908.93	5.00	2400	4.79	11.5	47.7
1.8	15	1011.06	5.00	2660	4.78	12.7	48.1
1.6	15	1143.85	5.00	2977	4.76	14.2	52.8
1.5	15	1220.20	5.00	3150	4.72	14.9	53.8
1.4	15	1311.07	5.00	3350	4.69	15.8	60.0
1.3	15	1417.96	5.00	3610	4.69	17.0	66.8
1.2	15	1545.47	5.00	3860	4.67	18.0	68.2
1.1	15	1695.32	5.00	4190	4.61	19.4	72.3
1	15	1882.11	5.00	4423	4.44	19.8	75.1

Table 5.1. 5V regulator measurements.

R(Ω)	V_IN(V)	I_IN(mA)	P_IN(W)	I_ROUT(mA)	V_ROUT(V)	P_OUT(W)	EFFICIENCY
500	15	3.94	0.0591	10	5.04	0.0504	85.28
400	15	4.84	0.0726	12	5.04	0.0605	83.31
350	15	5.74	0.0861	14	5.03	0.0704	81.79
300	15	6.37	0.0955	16	5.03	0.0805	84.23
250	15	7.68	0.1152	20	5.03	0.1006	87.33
200	15	9.55	0.1432	25	5.03	0.1257	87.78
150	15	11.74	0.1761	33	5.03	0.1659	94.26
100	15	18.03	0.2704	50	5.03	0.2515	92.99
75	15	25.13	0.3769	67	5.03	0.3370	89.40
50	15	37.35	0.5602	100	5.03	0.5030	89.78
40	15	45.31	0.6796	125	5.03	0.6287	92.51
30	15	62.34	0.9351	167	5.03	0.8400	89.83
20	15	88.04	1.3206	250	5.01	1.2525	94.84
15	15	122.65	1.8397	334	5.01	1.6733	90.95
12	15	151.72	2.2758	417	5.01	2.0891	91.80
10	15	182.06	2.7309	498	4.98	2.4800	90.81
9	15	202.19	3.0328	553	4.98	2.7539	90.80
8	15	226.35	3.3952	623	4.98	3.1025	91.38
7	15	258.88	3.8832	712	4.98	3.5457	91.31
6	15	300.98	4.5147	826	4.95	4.0887	90.56
5.5	15	328.85	4.9327	901	4.95	4.4599	90.41
5	15	362.60	5.4390	991	4.95	4.9054	90.19
4.5	15	401.16	6.0174	1095	4.93	5.3983	89.71
4	15	450.39	6.7558	1232	4.93	6.0737	89.90
3.5	15	517.38	7.7607	1401	4.90	6.8649	88.46
3	15	604.30	9.0645	1625	4.87	7.9137	87.30
2.5	15	724.08	10.8612	1940	4.85	9.4090	86.63
2	15	908.93	13.6339	2400	4.79	11.4960	84.32
1.8	15	1011.06	15.1659	2660	4.78	12.7148	83.84
1.6	15	1143.85	17.1577	2977	4.76	14.1705	82.59
1.5	15	1220.20	18.3030	3150	4.72	14.8680	81.23
1.4	15	1311.07	19.6660	3350	4.69	15.7115	79.89
1.3	15	1417.96	21.2694	3610	4.69	16.9309	79.60
1.2	15	1545.47	23.1820	3860	4.67	18.0262	77.76
1.1	15	1695.32	25.4298	4190	4.61	19.3159	75.96
1	15	1882.11	28.2316	4423	4.44	19.6381	69.56

Table 5.2. 5V regulator efficiency.

We can observe a good efficiency for this regulator, achieving the best performance between 150 Ω and 4 Ω load.

Resistor (Ω)	Drop voltage at wire (mV)
2	92
1.8	101
1.6	107
1.5	120
1.4	132
1.3	143
1.2	153
1.1	163
1	172

Table 5.3.Drop voltage at wire of the 5V regulator.

This is the thermal camera view of the regulator.

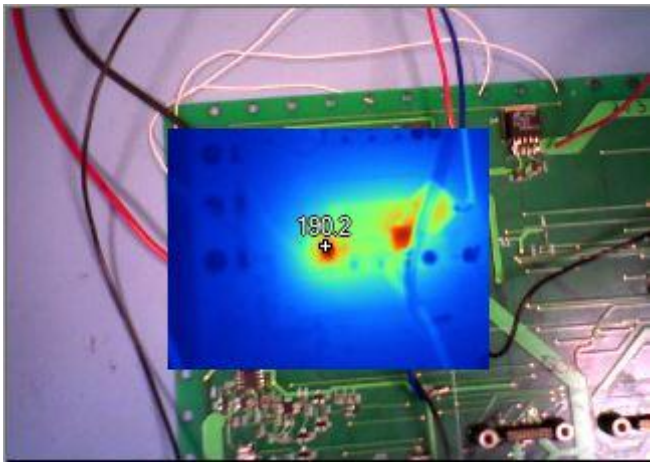


Figure 5.2. 5V regulator thermal camera view.

5.1.2 – Testing 3V3 regulator

At the next table is shown the input and output voltage and current. For testing the 3.3 V regulator is connected the supply voltage to the Honeycomb. Between the 3.3 V output and GND is plugged the programmable load to calculate the different voltages and currents changing its value.

The digital ammeter calculates the input current, I_IN at the table. The digital voltmeter calculates the output voltage, V_OUT. The programmable load had an internal multimeter which calculated the voltage, current and power at the load, V_ROUT, I_ROUT and P_ROUT.

Rw represents the resistance of the wires, this becomes important when the load has a small value.

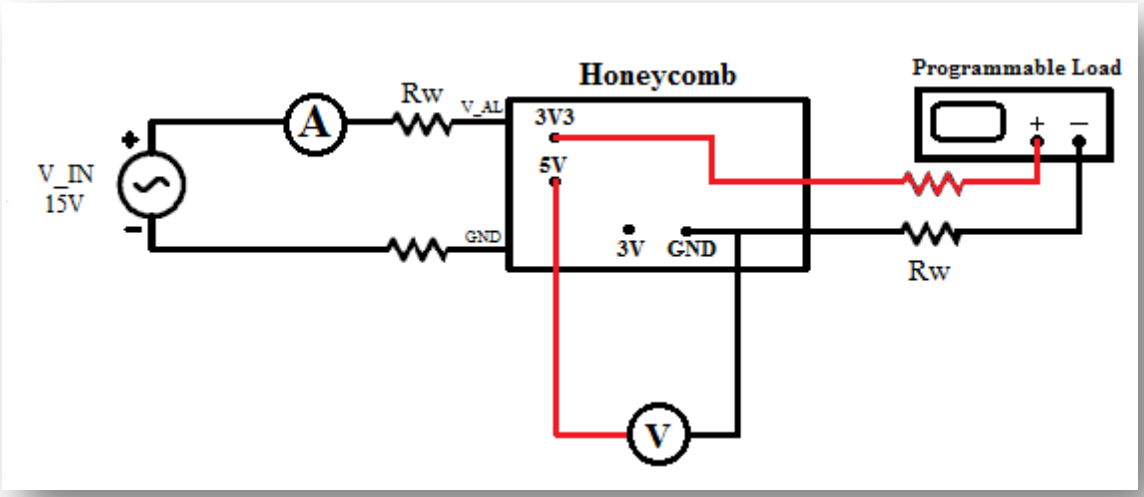


Figure 5.3. 3.3V regulator connections.

The input current of the power supply was limited to 1.4 A to assure not exceed the 1.6 A. We can observe how more input current is required when the load value is decremented.

At the load, we can see the same behavior as the current at the input, and when the load takes a small values, it cannot raises the 3.3 V.

The first T(ºC) column corresponds with the temperature of the TPS5450 regulator and the second T(ºC) column is the LT1963 temperature.

At the measurements of this regulator the smaller load value achieved was 2.5 Ω, and it was not decremented for two reasons: one, the output current was close to 1.6 A, and two, the temperature of the regulator was high.

A second table is included with the input and output power calculated and the efficiency.

A third table is shown with the wire resistance measured, when the drop voltage was important, because its value was as the load.

R (Ω)	V_IN (V)	I_IN (mA)	V_OUT (V)	I_ROUT (mA)	V_ROUT (V)	P_ROUT (W)	T (ºC)	T (ºC)
500	15	1.63	3.296	6	3.329	0.0	30.6	31.2
400	15	2.09	3.295	8	3.329	0.0	30.8	32.3
350	15	2.50	3.295	9	3.329	0.0	30.9	32.7
300	15	3.21	3.295	11	3.327	0.0	30.9	33.3
250	15	3.89	3.295	13	3.327	0.0	31.0	33.8
200	15	4.15	3.295	16	3.327	0.1	31.3	34.0
150	15	6.45	3.295	22	3.327	0.1	31.8	34.1
100	15	9.42	3.295	33	3.325	0.1	32.0	34.4
75	15	12.30	3.295	44	3.325	0.1	32.1	34.6
50	15	18.77	3.295	66	3.323	0.2	32.3	35.1
40	15	23.34	3.295	83	3.321	0.3	32.5	35.2
30	15	32.77	3.295	110	3.317	0.4	32.7	36.0
20	15	49.02	3.295	165	3.313	0.5	32.8	36.8
15	15	65.36	3.295	220	3.307	0.7	33.0	38.1
12	15	81.80	3.293	275	3.301	0.9	33.1	38.6
10	15	97.97	3.293	329	3.294	1.1	33.2	38.8
9	15	109.04	3.293	365	3.290	1.2	33.3	41.1
8	15	122.62	3.293	410	3.286	1.3	33.4	42.0
7	15	140.04	3.291	468	3.280	1.5	33.6	43.3
6	15	163.73	3.291	545	3.273	1.8	34.5	44.6
5.5	15	178.60	3.291	594	3.267	1.9	35.0	45.9
5	15	196.64	3.289	652	3.261	2.1	35.2	47.1
4.5	15	218.65	3.289	722	3.253	2.3	35.5	48.8
4	15	245.98	3.287	811	3.245	2.6	35.7	52.0
3.75	15	262.17	3.287	863	3.238	2.8	36.3	52.8
3.5	15	281.10	3.285	923	3.232	3.0	36.5	53.0
3.25	15	302.75	3.285	991	3.226	3.2	37.2	55.3
3	15	328.07	3.283	1072	3.218	3.4	38.1	57.9
2.75	15	357.88	3.283	1166	3.208	3.7	38.3	58.3
2.5	15	393.38	3.283	1277	3.194	4.1	39.4	61.2

Table 5.4. 3.3V regulator measurements.

R(Ω)	V_IN(V)	I_IN(mA)	P_IN(W)	V_OUT(V)	I_OUT(mA)	P_OUT(W)	EFFICIENCY
500	15	1.63	0.0244	3.329	6	0.0199	81.69
400	15	2.09	0.0313	3.329	8	0.0266	84.95
350	15	2.50	0.0375	3.329	9	0.0299	79.89
300	15	3.21	0.0481	3.327	11	0.0365	76.01
250	15	3.89	0.0583	3.327	13	0.0432	74.12
200	15	4.15	0.0622	3.327	16	0.0532	85.51
150	15	6.45	0.0967	3.327	22	0.0731	75.65
100	15	9.42	0.1413	3.325	33	0.1097	77.65
75	15	12.30	0.1845	3.325	44	0.1463	79.29
50	15	18.77	0.2815	3.323	66	0.2193	77.89
40	15	23.34	0.3501	3.321	83	0.2756	78.73
30	15	32.77	0.4915	3.317	110	0.3648	74.23
20	15	49.02	0.7353	3.313	165	0.5466	74.34
15	15	65.36	0.9804	3.307	220	0.7275	74.21
12	15	81.80	1.2270	3.301	275	0.9077	73.98
10	15	97.97	1.4695	3.294	329	1.0837	73.74
9	15	109.04	1.6356	3.290	365	1.2008	73.42
8	15	122.62	1.8393	3.286	410	1.3472	73.25
7	15	140.04	2.1006	3.280	468	1.5350	73.07
6	15	163.73	2.4559	3.273	545	1.7837	72.63
5.5	15	178.60	2.6790	3.267	594	1.9405	72.44
5	15	196.64	2.9496	3.261	652	2.1261	72.08
4.5	15	218.65	3.2797	3.253	722	2.3486	71.61
4	15	245.98	3.6897	3.245	811	2.6316	71.32
3.75	15	262.17	3.9325	3.238	863	2.7943	71.06
3.5	15	281.10	4.2165	3.232	923	2.9831	70.75
3.25	15	302.75	4.5412	3.226	991	3.1969	70.39
3	15	328.07	4.9210	3.218	1072	3.4496	70.10
2.75	15	357.88	5.3682	3.208	1166	3.7405	69.68
2.5	15	393.38	5.9007	3.194	1277	4.0787	69.12

Table 5.5. 3.3V regulator efficiency.

We can observe a good efficiency for this regulator, achieving the best performance between 500 Ω and 40 Ω load, approximately. This time, the regulator is worst regarding to the efficiency.

Resistor (Ω)	Drop voltage at wire (mV)
5.5	16.0
5	18.2
4.5	19.8
4	22.7
3.75	24.3
3.5	25.7
3.25	27.7
3	30.1
2.75	32.6
2.5	35.9

Table 5.6. Drop voltage at wire of the 3.3V regulator

This is the thermal camera view of the regulator.

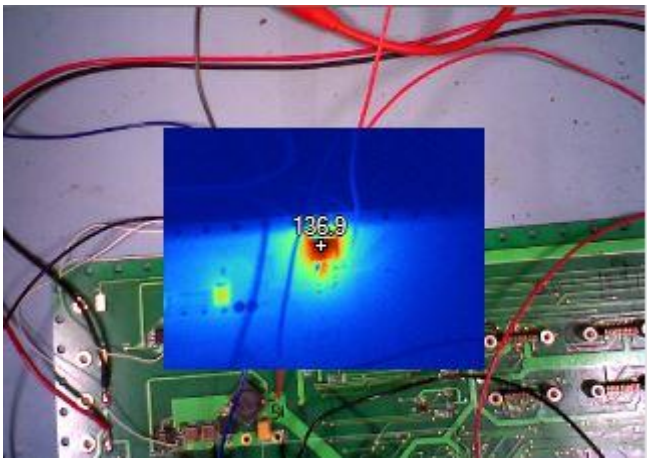


Figure 5.4. 3.3V regulator thermal camera view (I).

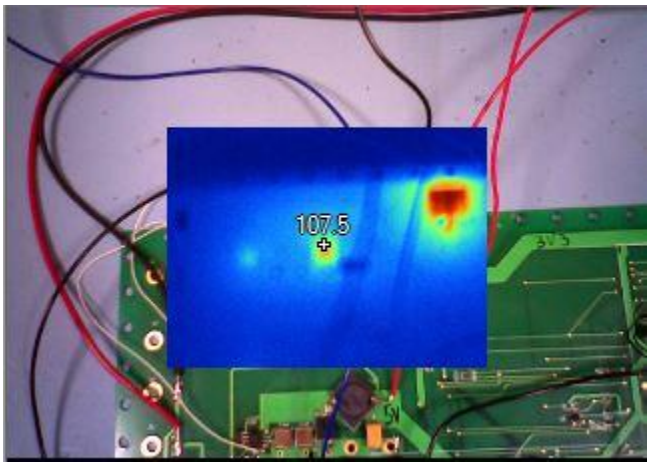


Figure 5.5. 3.3V regulator thermal camera view (II).

5.1.3 – Testing 3V regulator

At the next table is shown the input and output voltage and current. For testing the 3 V regulator is connected the supply voltage to the Honeycomb. Between the 3 V output and GND is plugged the programmable load to calculate the different voltages and currents changing its value.

The digital ammeter calculates the input current, I_IN at the table. The digital voltmeter calculates the output voltage, V_OUT. The programmable load had an internal multimeter which calculated the voltage, current and power at the load, V_ROUT, I_ROUT and P_ROUT.

Rw represents the resistance of the wires, this becomes important when the load has a small value.

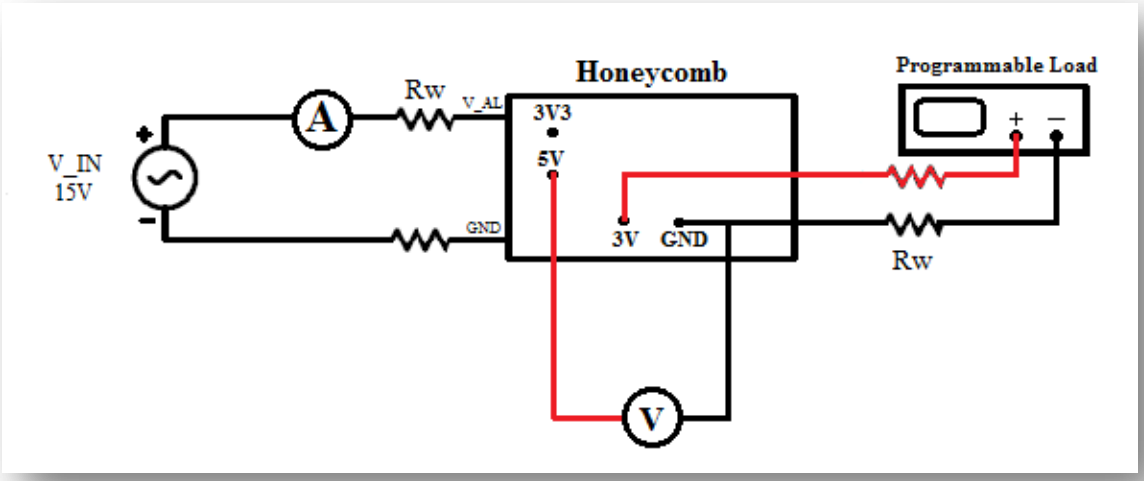


Figure 5.6. 3V regulator connections.

The input current of the power supply was limited to assure not exceed the 20 mA output current, maximum value of the datasheet.

At the load, we can see that, lower is this, more current is required.

The T(ºC) column corresponds with the temperature of the LM4128 regulator temperature.

At the measurements of this regulator the smaller load value achieved was 155 Ω, and it was not decremented because the output current was close to 20 mA.

A second table is included with the input and output power calculated and the efficiency.

The 3 V reference voltage was the lower regulator regarding to the efficiency.

Power supply connected to the regulators:
V_IN = 15V

R(Ω)	I_IN(A)	V_OUT(V)	V_ROUT(V)	I_ROUT(A)	P_ROUT(W)	T(ºC)
500	0.100	2.989	3.012	0.006	0.0	30.0
450	0.100	2.988	3.012	0.006	0.0	30.0
400	0.100	2.988	3.012	0.007	0.0	30.0
350	0.100	2.987	3.010	0.008	0.0	30.0
300	0.102	2.986	3.010	0.010	0.0	30.2
250	0.102	2.984	3.008	0.012	0.0	30.2
225	0.102	2.984	3.006	0.013	0.0	30.2
200	0.103	2.982	3.004	0.015	0.0	31.1
175	0.105	2.980	3.002	0.017	0.1	31.3
155	0.105	2.980	3.002	0.019	0.1	32.0

Table 5.7. 3V regulator measurements

R(Ω)	V_IN(V)	I_IN(A)	P_IN(W)	V_ROUT(V)	I_ROUT(A)	P_OUT(W)	EFFICIENCY
500	15	0.100	1.500	3.012	0.006	0.018	1.20
450	15	0.100	1.500	3.012	0.006	0.018	1.20
400	15	0.100	1.500	3.012	0.007	0.021	1.40
350	15	0.100	1.500	3.010	0.008	0.024	1.60
300	15	0.102	1.530	3.010	0.010	0.030	1.97
250	15	0.102	1.530	3.008	0.012	0.036	2.36
225	15	0.102	1.530	3.006	0.013	0.039	2.55
200	15	0.103	1.545	3.004	0.015	0.045	2.91
175	15	0.105	1.575	3.002	0.017	0.051	3.24
155	15	0.105	1.575	3.002	0.019	0.057	3.62

Table 5.8. 3V regulator efficiency.

5.2 – Testing PDB

Firstly, a power supply directly connected to the solar cell simulator was used, but this system gave us problems at high frequency. The solution was introduce a input resistor between the power supply and the solar cell simulator. The procedure to select the suitable resistor was as follows.

Our solar cell simulator has the maximum point of work for 32 V and working with a current equal to 0.482 A. Taking 50 Ω for the input resistor:

$$Supply\ voltage = 32\ V + drop\ voltage\ at\ R\_IN$$

$$Supply\ voltage = 32\ V + 50\Omega \times 0.482A = 32V + 24V = 56V$$

Then, 56 V for the power supply was applied.

The input power resistor used, was created by soldering two 100 Ω - 10 W resistors connected in parallel to achieve 50 Ω resistor. To view the resistor go to the Appendix C.

The connections are shown at figure below.

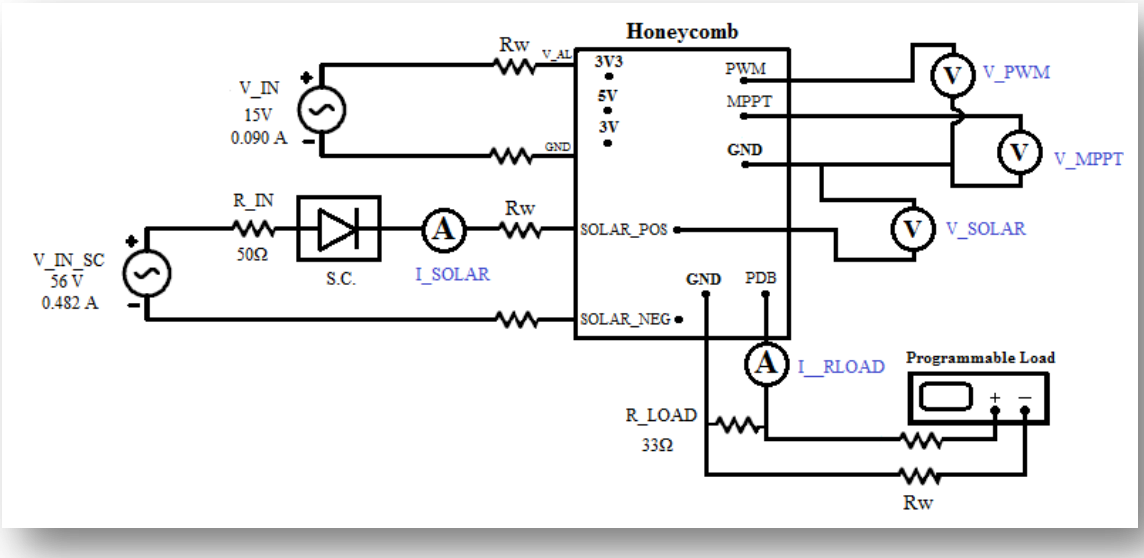


Figure 5.7. Honeycomb connections.

To avoid possible problems, it is explained from where are taken the measurements.

- V_PDB → Between PDB pin and GND.
- V_PWM → Between DC_OUT output of PWM to DC Converter and GND.
- V_MPPT → Between VOUT output of MPPT and GND.
- V_SOLAR → Between SOLAR_POS pin and GND.

- V_RLOAD → Between both terminals of load resistor.
- I_RLOAD → Between PDB and R_LOAD, as shown at *Figure 5.7*.
- I_SOLAR → Between solar cell simulator and SOLAR_POS, as shown at *Figure 5.7*.
- V_IN_SC → Between both terminals of 56 V power supply.

With the aim to not burn the Honeycomb, a power resistor was connected at PDB output. Three different resistors were plugged to characterize the range of resistors that was secure to not burn the system. These are the resistors:

6.8 Ω - 25 W → RS 25W 6.8R (Supplier: RS)

22 Ω - 15 W → HS15 22R J (Supplier: ARCOL)

33 Ω - 50 W → HS50 33R J (Supplier: ARCOL)

Connecting both power supplies, as at the *Figure 5.7*, the values of voltage, current and power measured are the following:

Power supply connected to the regulators:

V_IN = 15V I_IN = 99.6 mA

Power supply connected to the solar inputs:

V_IN_SC = 56V I_IN_SC = 0.482A

Drop voltage on terminals of input resistance: V_RIN = 23.43V

R (Ω)	V_PDB (V)	V_RLOAD (V)	I_RLOAD (A)	P_RLOAD (W)	V_PWM (V)	V_SOLAR (V)	V_MPPT (V)
6.8	8.92	8.91	1.122	9.997	2.586	25.72	8.95
22.0	16.38	16.35	0.683	11.167	2.587	27.15	16.40
33.0	19.22	19.20	0.562	10.790	2.588	27.30	19.32

Table 5.9. PDB initial measurements.

Then, around 19 V at PDB it is enough maximum voltage level, for that, the maximum load connected will be 33.0 Ω, and it will be decreased, connecting in parallel the programmable load. The table with the several voltages is shown below:

Power supply connected to the regulators:

V_IN = 15V I_IN = 0.090A

Power supply connected to the solar inputs:

V_IN_SC = 56V I_IN_SC = 0.482A

Drop voltage on terminals of input resistance: V_RIN = 23.43V

R (Ω)	V_PDB (V)	V_PWM (V)	V_MPPT (V)	V_SOLAR (V)	V_RLOAD (V)	I_RLOAD (A)	I_SOLAR (A)	V_IN_SC (V)
33.00	19.39	2.588	19.41	27.32	19.38	0.566	0.4421	51.5
30.95	19.25	2.588	19.30	27.64	19.26	0.598	0.4434	51.3
28.32	18.35	2.588	18.38	27.48	18.34	0.621	0.4442	51.2
24.81	17.10	2.587	17.13	27.29	17.09	0.658	0.4450	51.0
20.48	15.45	2.587	15.48	27.05	15.44	0.715	0.4461	50.7
18.00	14.48	2.587	14.52	26.90	14.46	0.755	0.4466	50.6
16.50	13.80	2.587	13.84	26.80	13.79	0.786	0.4469	50.5
14.22	12.80	2.586	12.84	26.63	12.78	0.837	0.4475	50.3
12.45	11.94	2.586	11.99	26.46	11.94	0.885	0.4479	50.2
10.31	10.94	2.586	11.00	26.25	10.90	0.954	0.4485	49.9
8.80	10.08	2.586	10.14	26.05	10.07	1.016	0.4490	49.7
7.07	9.04	2.586	9.10	25.80	9.04	1.106	0.4496	49.4
6.43	8.68	2.586	8.73	25.70	8.67	1.142	0.4498	49.3
5.77	8.27	2.586	8.33	25.56	8.25	1.190	0.4501	49.2
5.07	7.73	2.586	7.80	25.43	7.73	1.249	0.4504	49.1
4.34	7.21	2.586	7.26	25.26	7.20	1.319	0.4507	48.9
3.56	6.52	2.586	6.60	25.05	6.53	1.421	0.4511	48.6

Table 5.10. PDB measurements.

The following are the temperature of two diodes of the honeycomb tile.

R (Ω)	R (Ω)	T – M1 (ºC)	T – D10 (ºC)
-	33.00	37.6	37.3
33 // 500	30.95	38.5	38.1
33 // 200	28.32	40.4	39.7
33 // 100	24.81	42.5	42.1
33 // 54	20.48	44.2	44.0
33 // 40	18.00	45.9	45.1
33 // 33	16.50	46.2	45.5
33 // 25	14.22	46.6	46.2
33 // 20	12.45	48.8	46.8
33 // 15	10.31	49.1	47.2
33 // 12	8.80	52.2	48.3
33 // 9	7.07	53.1	50.1
33 // 8	6.43	53.6	53.7
33 // 7	5.77	53.7	56.8
33 // 6	5.07	55.1	58.4
33 // 5	4.34	56.7	60.2
33 // 4	3.56	57.6	64.2

Table 5.11. Diodes temperature.

And this is the study of the efficiency of the PDB system.

R (Ω)	V_SOLAR (V)	I_SOLAR (A)	P_IN (W)	V_RLOAD (V)	I_RLOAD (A)	P_OUT (W)	EFFICIENCY
33.00	27.32	0.4421	12.0781	19.38	0.566	10.9690	90.82
30.95	27.64	0.4434	12.2555	19.26	0.598	11.5174	93.98
28.32	27.48	0.4442	12.2066	18.34	0.621	11.3891	93.30
24.81	27.29	0.4450	12.1440	17.09	0.658	11.2452	92.60
20.48	27.05	0.4461	12.0670	15.44	0.715	11.0396	91.48
18.00	26.90	0.4466	12.0135	14.46	0.755	10.9173	90.87
16.50	26.80	0.4469	11.9769	13.79	0.786	10.8389	90.50
14.22	26.63	0.4475	11.9169	12.78	0.837	10.6968	89.76
12.45	26.46	0.4479	11.8514	11.94	0.885	10.5669	89.16
10.31	26.25	0.4485	11.7731	10.90	0.954	10.3986	88.32
8.80	26.05	0.4490	11.6964	10.07	1.016	10.2311	87.47
7.07	25.80	0.4496	11.5996	9.040	1.106	9.9982	86.19
6.43	25.70	0.4498	11.5598	8.67	1.142	9.9011	85.65
5.77	25.56	0.4501	11.5045	8.25	1.190	9.8175	85.33
5.07	25.43	0.4504	11.4536	7.73	1.249	9.6547	84.29
4.34	25.26	0.4507	11.3846	7.20	1.319	9.4968	83.42
3.56	25.05	0.4511	11.3000	6.53	1.421	9.2791	82.11

Table 5.12. PDB efficiency.

5.3 – Ripple of the regulators

5.3.1 – Ripple of 5 V regulator

With the digital oscilloscope of the hardware laboratory, the ripple of the 5 V regulator was measured and plotted with Matlab tool. The measurement was done for several loads.

For 1 Ω load around 60 mV peak to peak ripple.

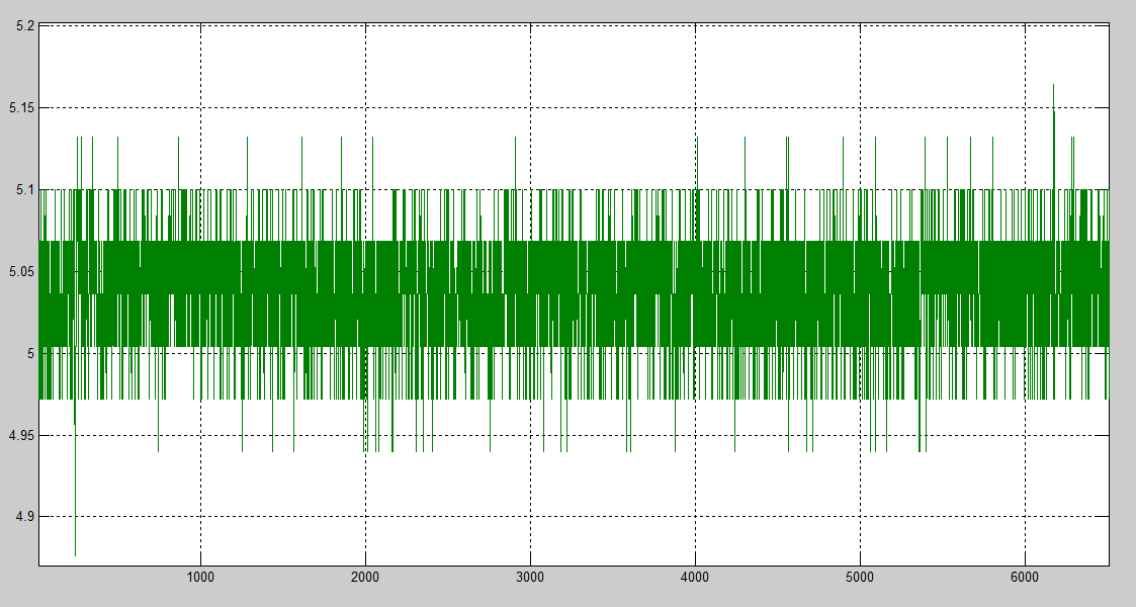


Figure 5.8. Ripple of 5V regulator with 1Ω load.

For 2.5 Ω load around 65 mV peak to peak ripple.

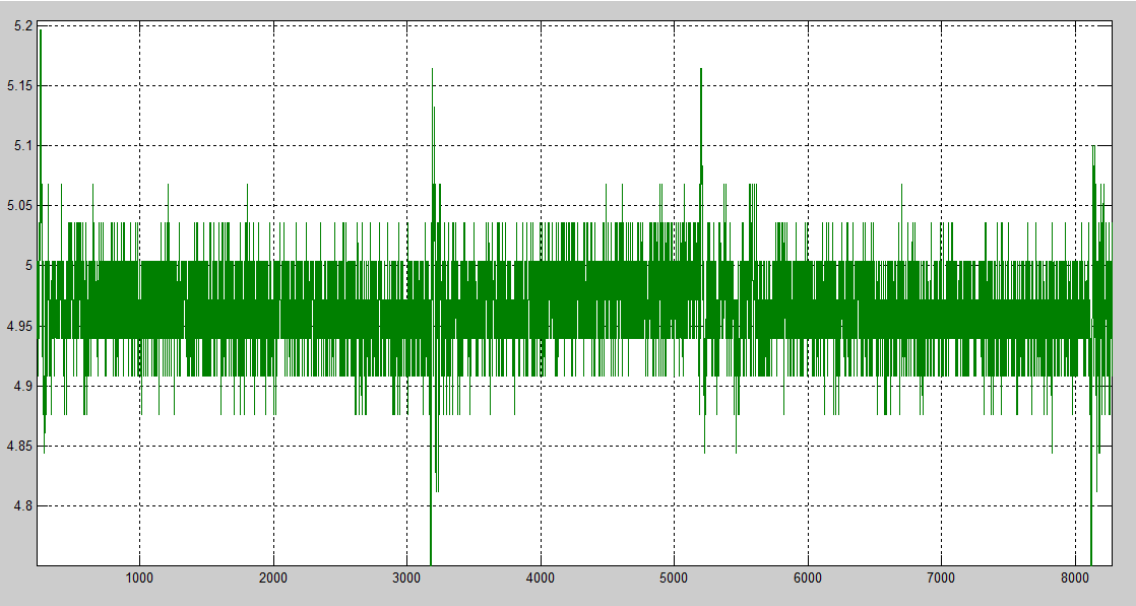


Figure 5.9. Ripple of 5V regulator with 2.5Ω load.

For 5 Ω load around 65 mV peak to peak ripple.

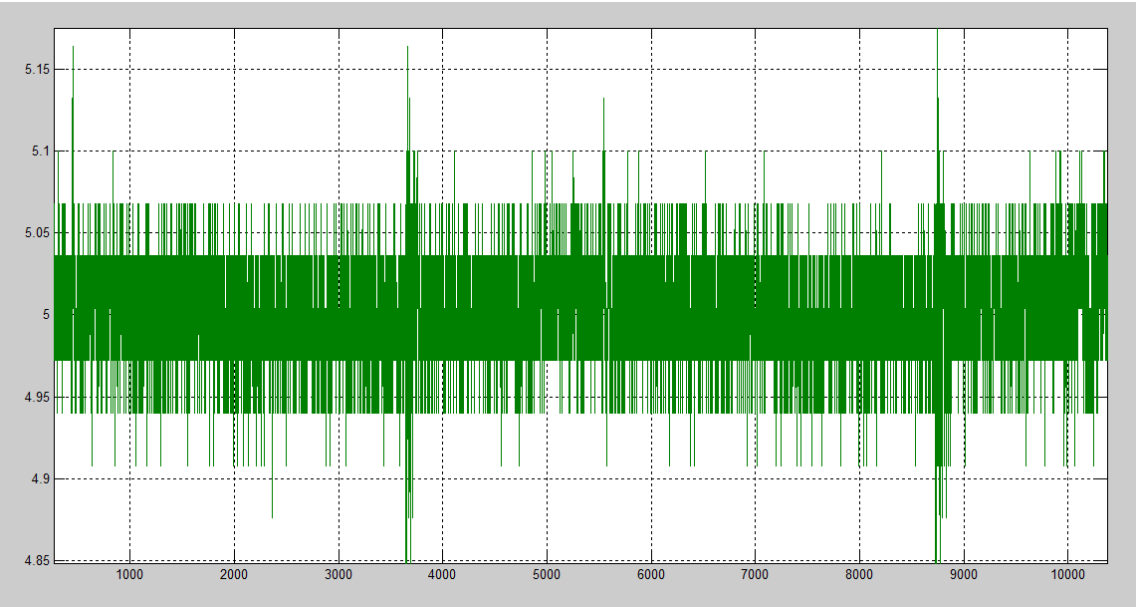


Figure 5.10. Ripple of 5V regulator with 5Ω load.

For 10 Ω load around 95 mV peak to peak ripple.

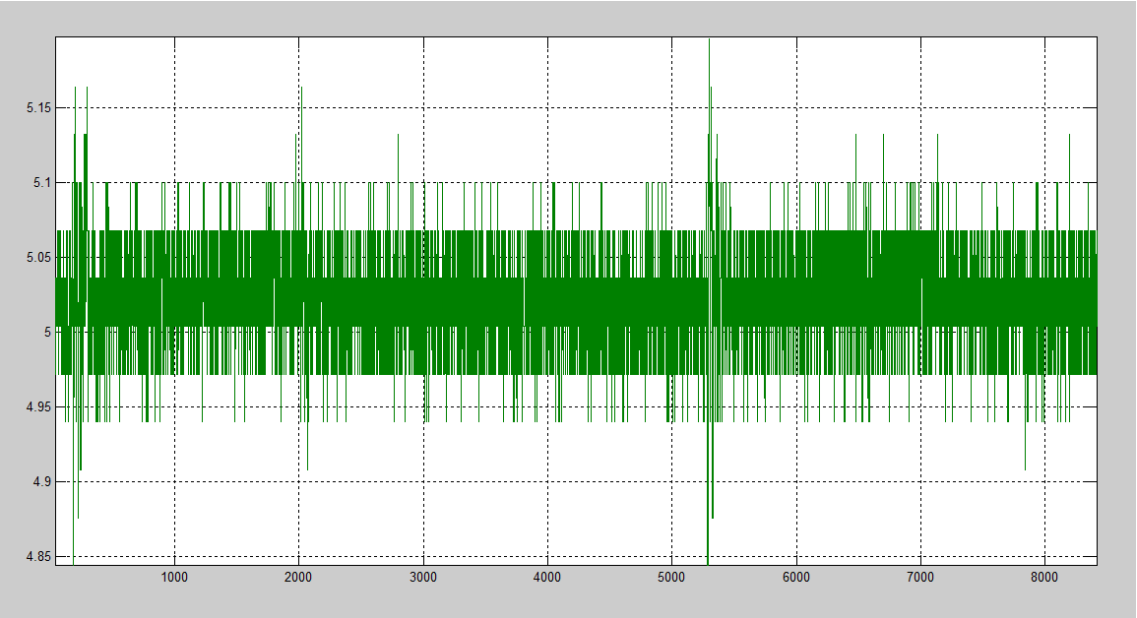


Figure 5.11. Ripple of 5V regulator with 10Ω load.

For 500 Ω load around 95 mV peak to peak ripple.

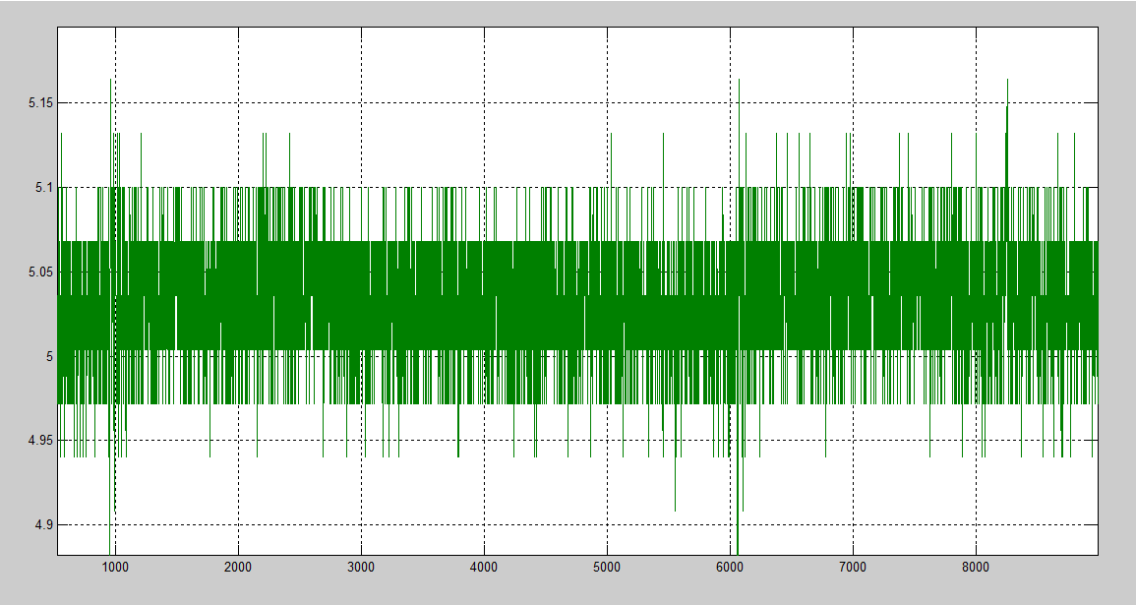


Figure 5.12. Ripple of 5V regulator with 1Ω load.

Also the ripple was calculated from the simulation of Mentor Graphics.

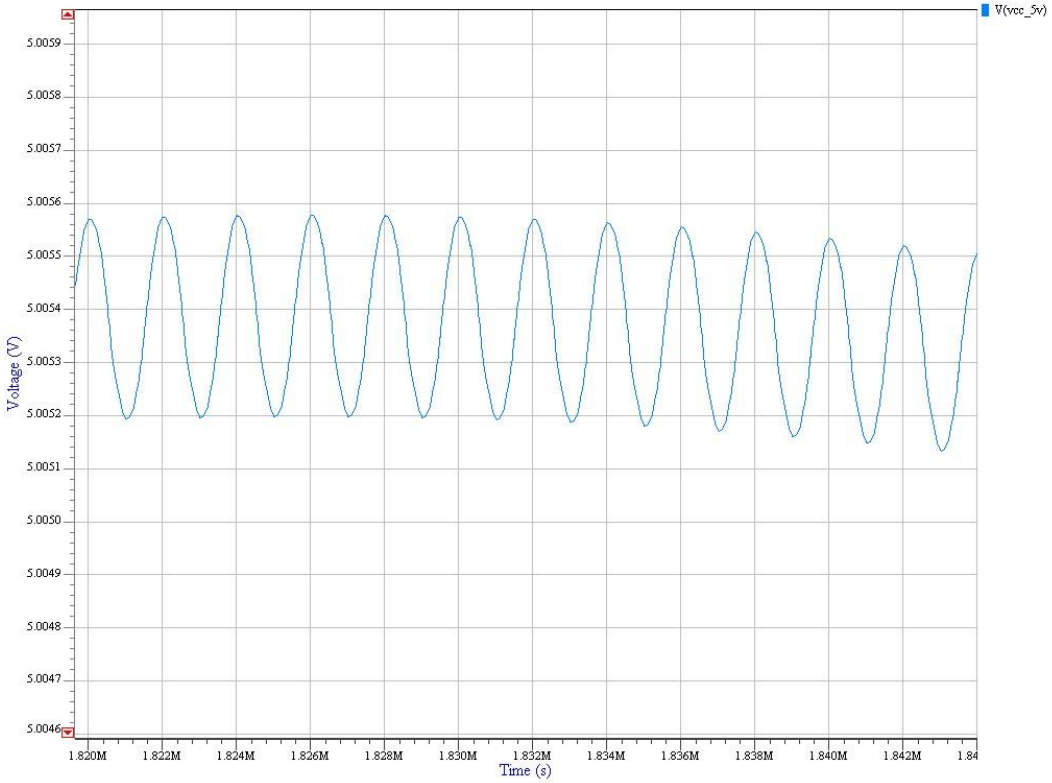


Figure 5.13. Ripple of 5V regulator on Mentor Graphics.

We can observe a ripple of around 0.4 mV, but the simulation does not match with the real regulator.

5.3.2 – Ripple of 3.3 V regulator

With the digital oscilloscope of the hardware laboratory, the ripple of the 3.3 V regulator was measured and plotted with Matlab tool. The measurement was done for several loads.

For 2.5 Ω load around 100 mV peak to peak ripple.

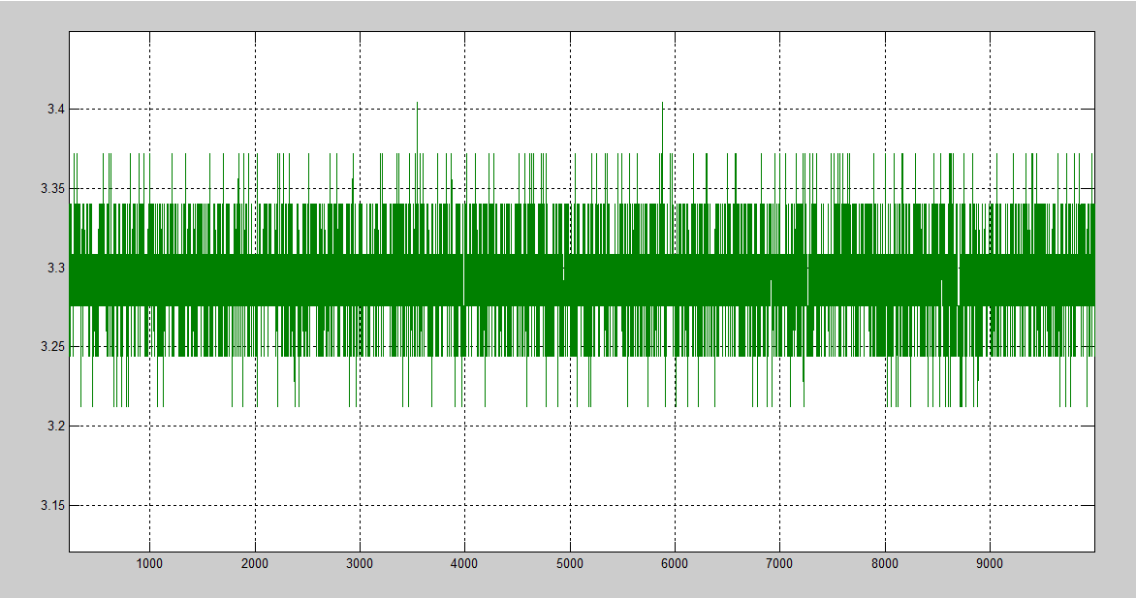


Figure 5.14. Ripple of 3.3V regulator with 2.5Ω load.

For 4 Ω load around 65 mV peak to peak ripple.

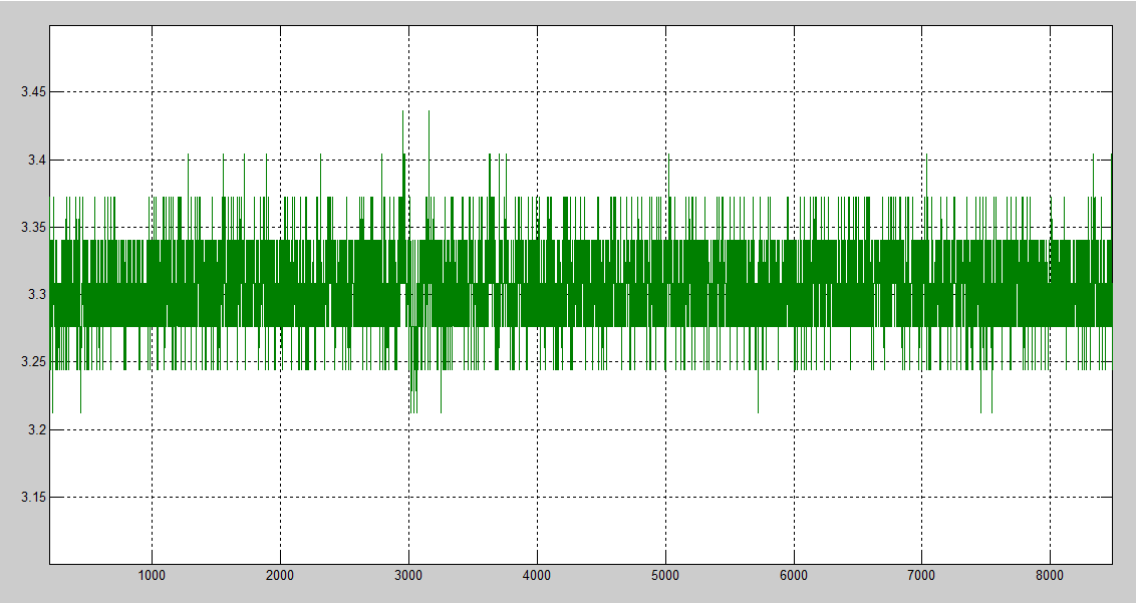


Figure 5.15. Ripple of 3.3V regulator with 4Ω load.

For 6 Ω load around 92 mV peak to peak ripple.

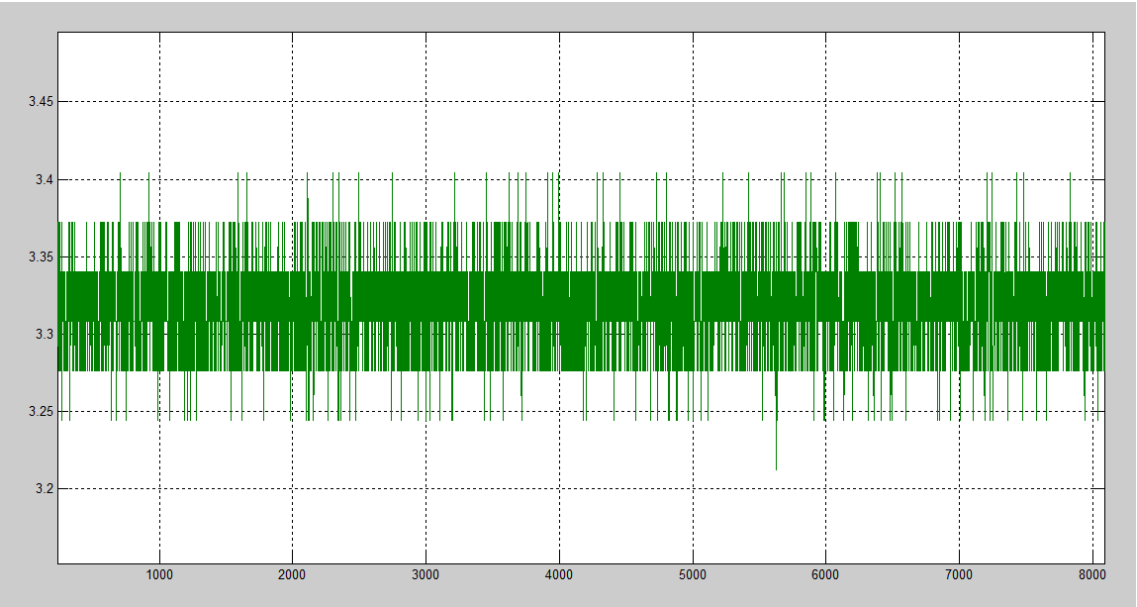


Figure 5.16. Ripple of 3.3V regulator with 6Ω load.

For 500 Ω load around 90 mV peak to peak ripple.

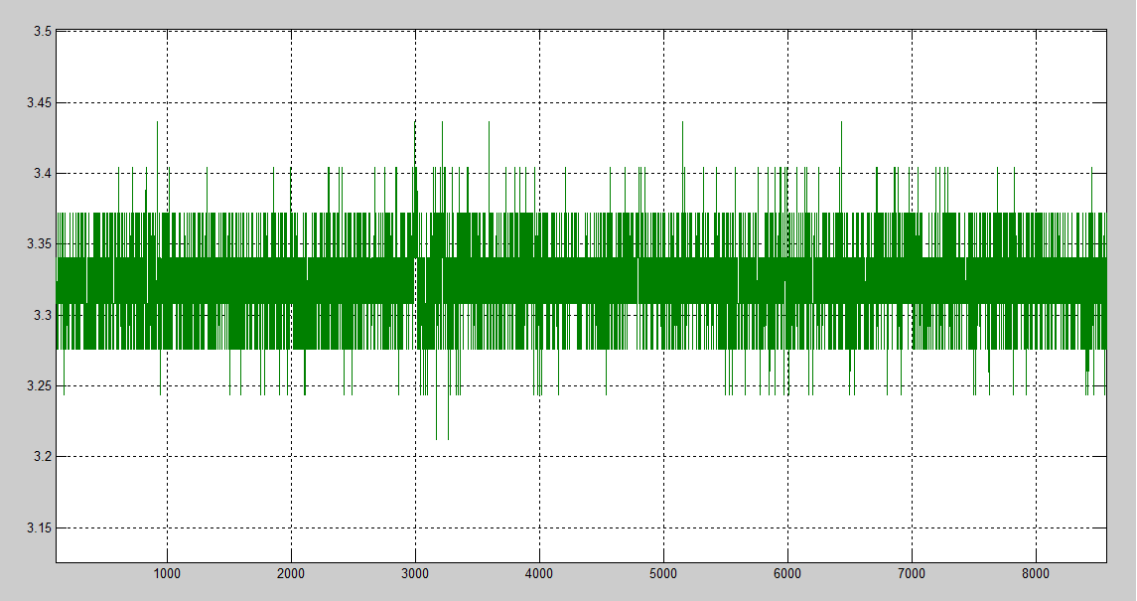


Figure 5.17. Ripple of 3.3V regulator with 500Ω load.

Also the ripple was calculated from the simulation of Mentor Graphics.

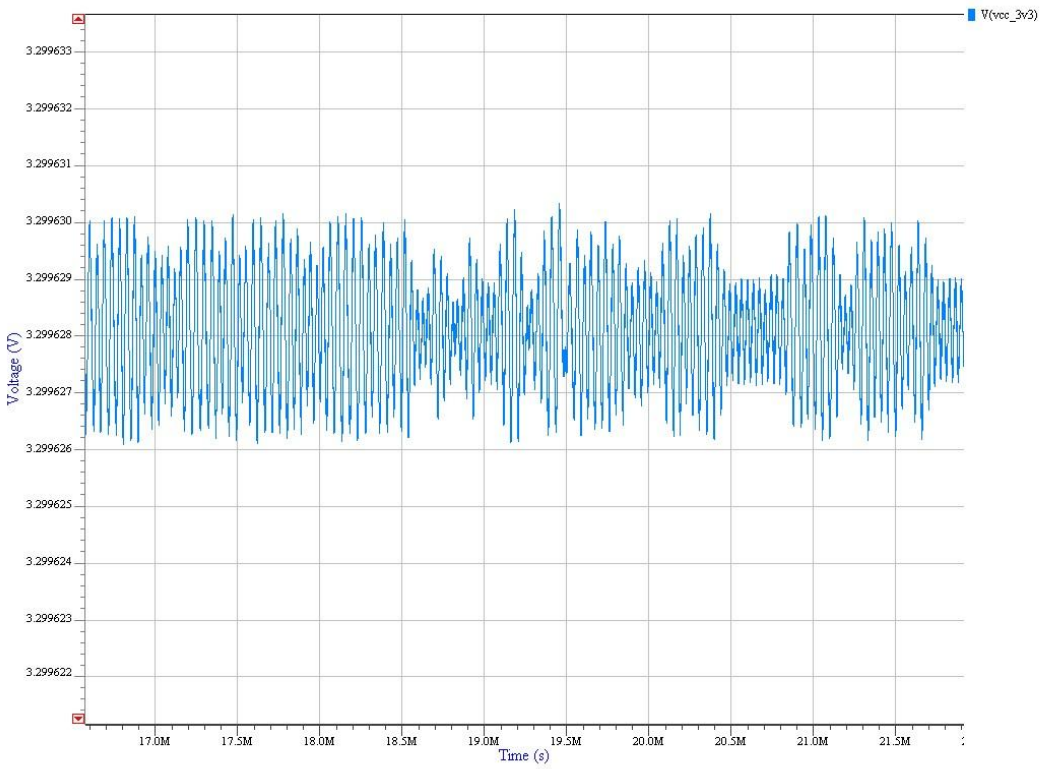


Figure 5.18. Ripple of 5V regulator on Mentor Graphics.

As with the 5 V regulator, we can observe a ripple of around 0.004 mV, but the simulation does not match with the real regulator.

To end this point, the graphs of the TPS5450 real signals of both regulators were plotted with Matlab.

The 3.3 V regulator with a 6 Ω load is shown below:

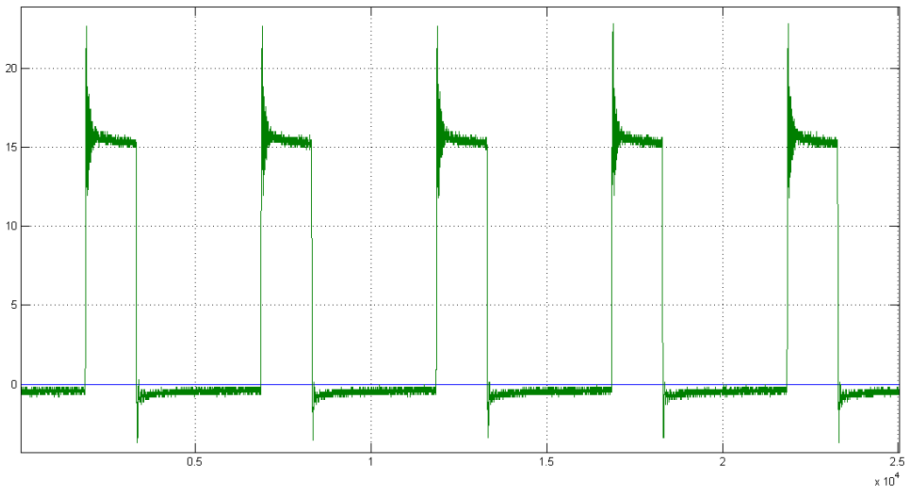


Figure 5.19. 3.3V regulator signal with 6Ω load.

The 5 V regulator with a 25 Ω load is shown below:

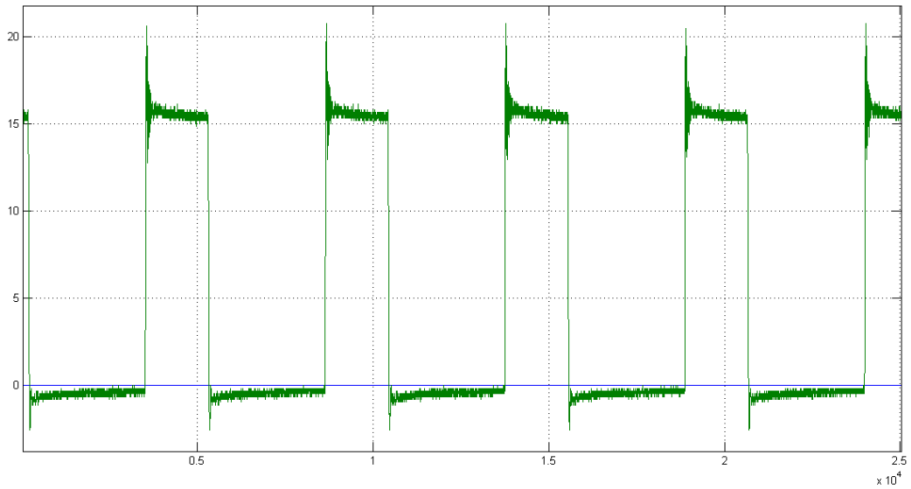


Figure 5.20. 5V regulator signal with 25Ω load.

The switching frequency is close to 500 kHz.

5.3.3 – Ripple of MPPT

The input and output signals of the MAX975 of the MPPT block were plotted with Matlab.

The positive input is shown below.

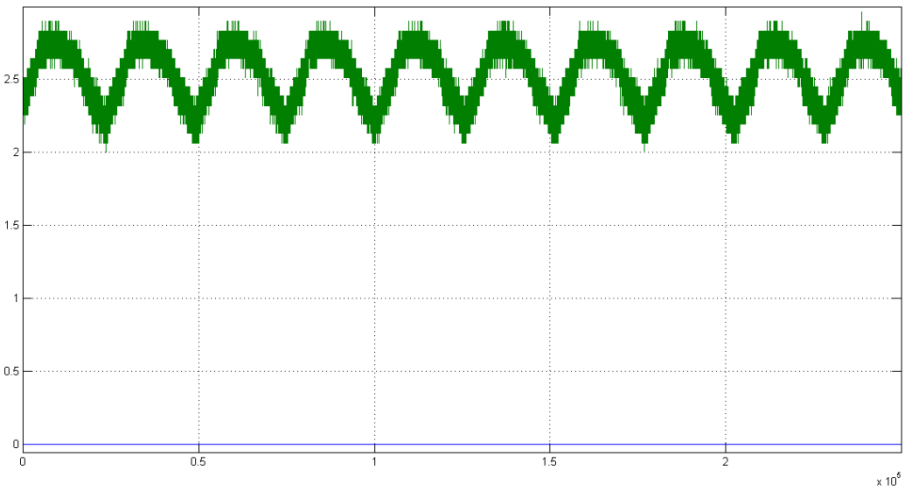


Figure 5.21. MPPT positive input signal.

The negative input is the following.

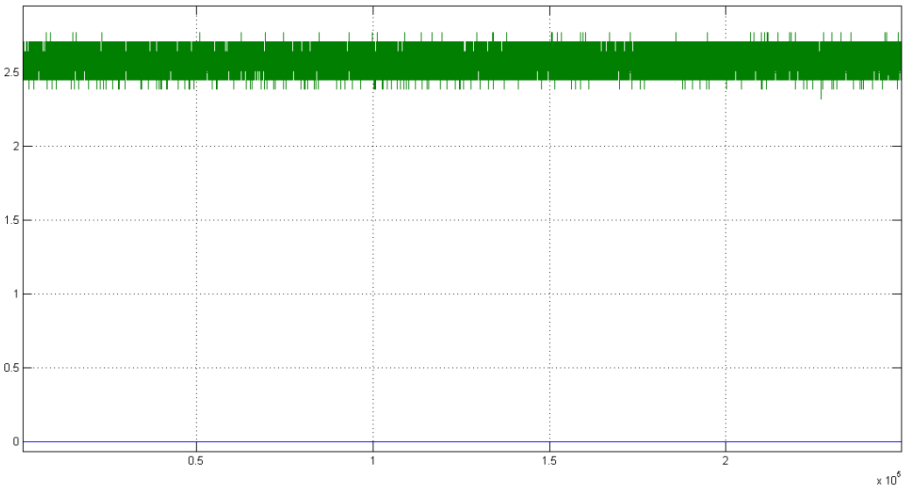


Figure 5.22. MPPT negative input signal.

For the output, two cases were plotted, one for 33 Ω load and another with 33//33 Ω load.

The exit for 33 Ω load is shown below.

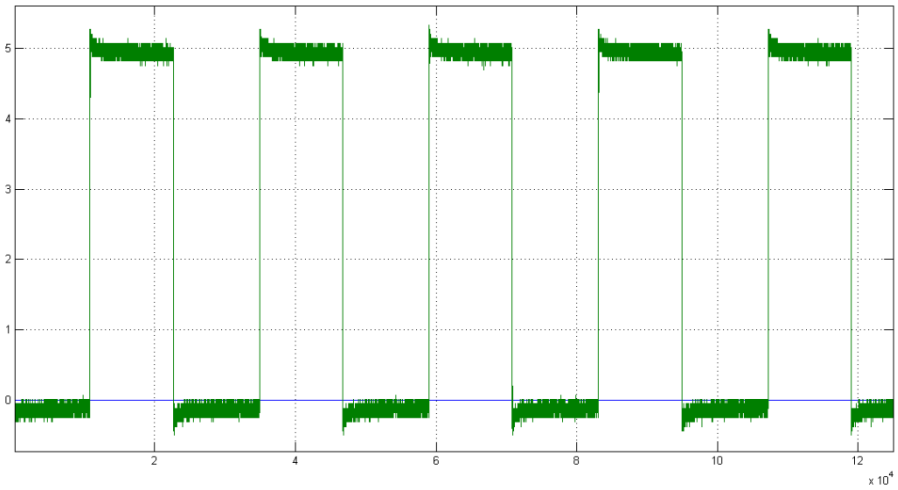


Figure 5.23. MPPT output signal with 33Ω load.

And for 33//33 Ω load.

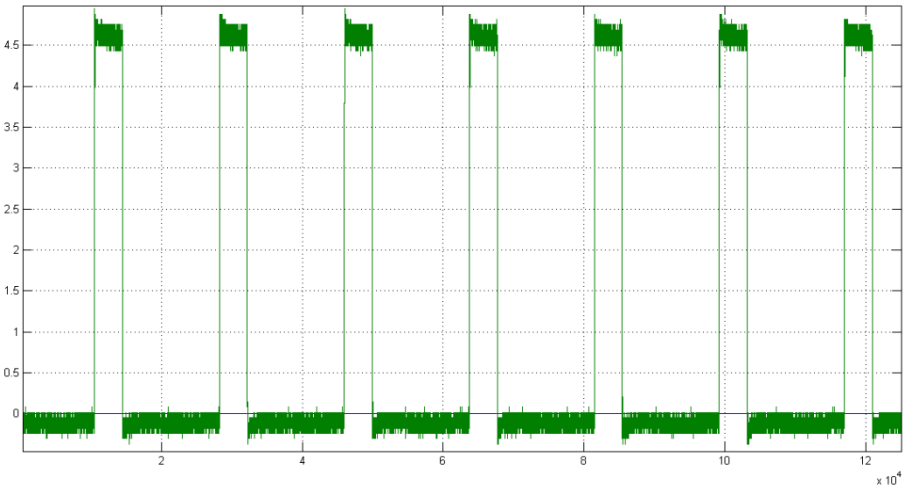


Figure 5.24. MPPT output signal with 33//33Ω load.

A difference of the duty cycle can be note.

Chapter 6

Comparison simulations and testing results

The aim of this chapter is to compare the testing results with the simulations. The current through the load at testing of the regulators is compared for both cases.

For the 5 V regulator, taking the data of the testing of the table of the Chapter 6:

R(Ω)	V_IN(V)	I_IN(mA)	V_OUT(V)	I_ROUT(mA)	V_ROUT(V)	P_ROUT(W)	T(ºC)
250	15	7.68	5.00	**20**	5.03	0.1	31.3
7	15	258.88	5.00	**712**	4.98	3.5	33.9
2	15	908.93	5.00	**2400**	4.79	11.5	47.7
1.1	15	1695.32	5.00	**4190**	4.61	19.4	72.3

Table 6.1. 5V regulator measurements.

And the simulation result, we can see that these values match.

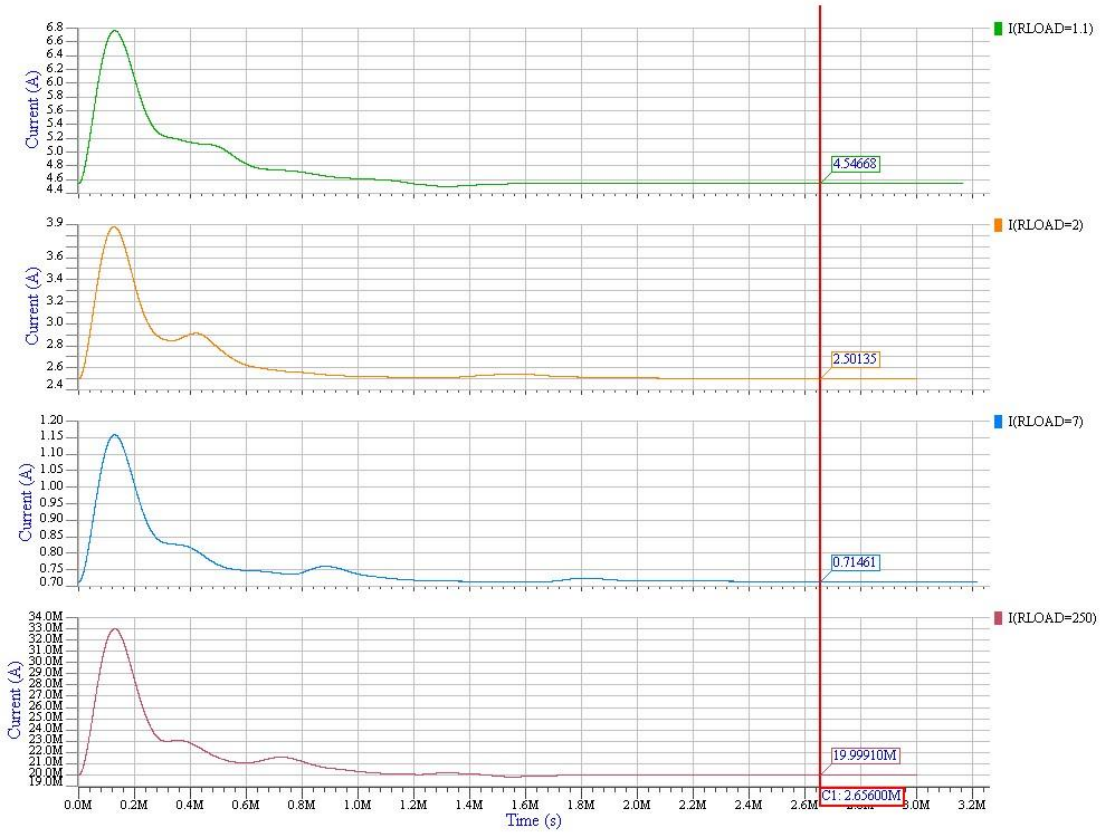


Figure 6.1. Current through the load graphs.

For the 3.3 V regulator, taking the data of the testing of the table of the Chapter 6:

R (Ω)	V_IN (V)	I_IN (mA)	V_OUT (V)	I_ROUT (mA)	V_ROUT (V)	P_ROUT (W)	T (ºC)	T (ºC)
200	15	4.15	3.295	**16**	3.327	0.1	31.3	34.0
6	15	163.73	3.291	**545**	3.273	1.8	34.5	44.6
3.5	15	281.10	3.285	**923**	3.232	3.0	36.5	53.0
2.5	15	393.38	3.283	**1277**	3.194	4.1	39.4	61.2

Table 6.2. 3.3V regulator measurements.

And the simulation result, we can see that these values match.

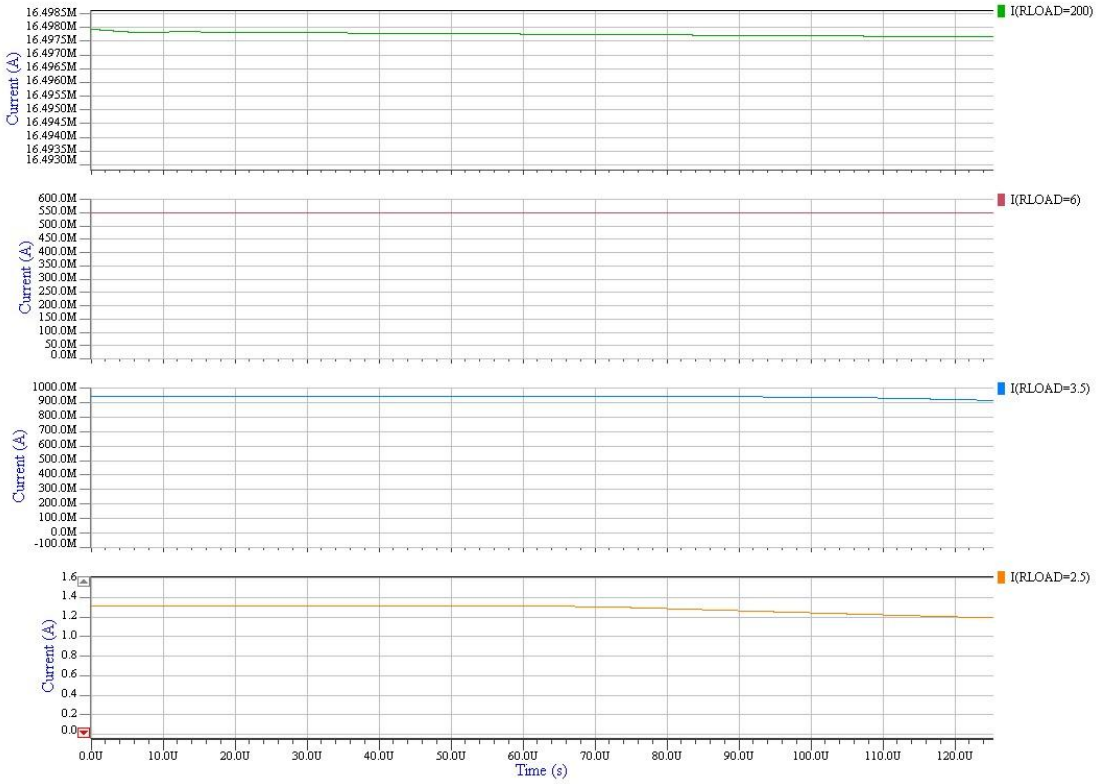


Figure 6.2. Current through the load graphs.

For the 3 V regulator, taking the data of the testing of the table of the Chapter 6:

R(Ω)	I_IN(A)	V_OUT(V)	V_ROUT(V)	I_ROUT(A)	P_ROUT(W)	T(ºC)
500	0.100	2.989	3.012	**0.006**	0.0	30.0
250	0.102	2.984	3.008	0.012	0.0	30.2
155	0.105	2.980	3.002	0.019	0.1	32.0

Table 6.3. 3V regulator measurements.

And the simulation result, we can see that these values match.

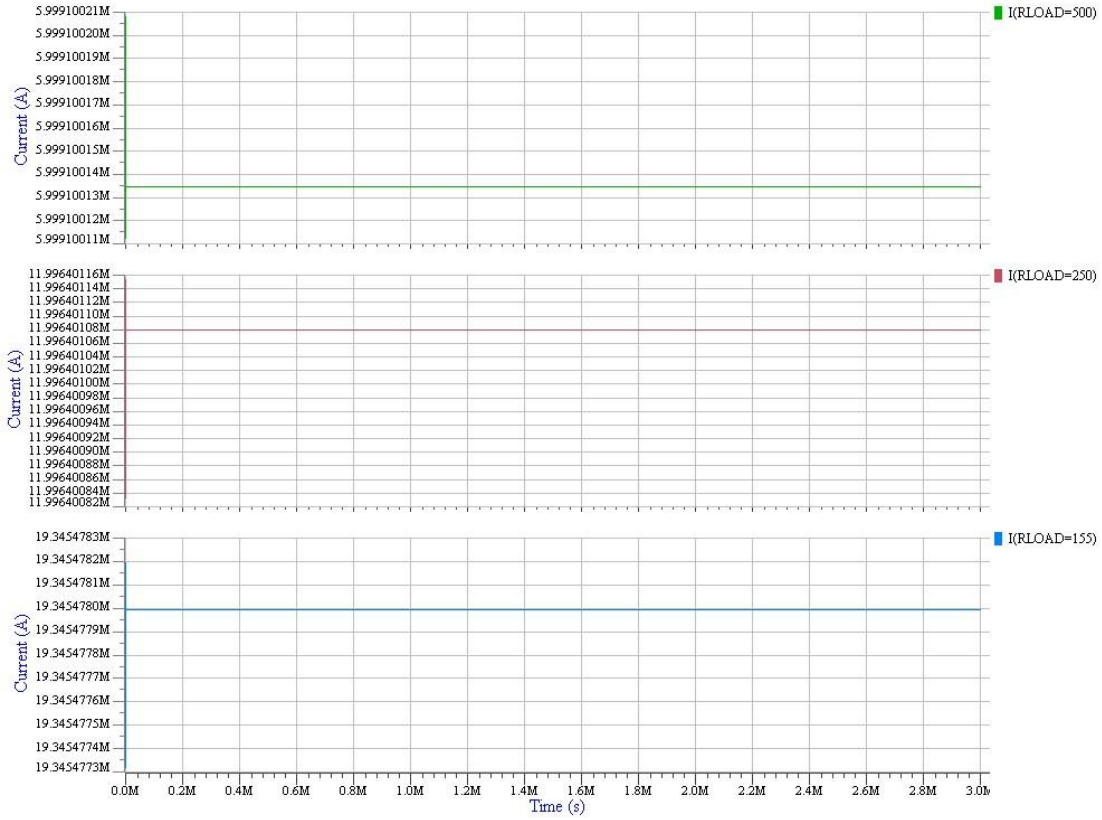


Figure 6.3. Current through the load graphs.

Chapter 7

Conclusion

The goal of this thesis is to test a power management system for spacecraft modules. The work consists of a study of hardware schematics, doing some modification of hardware board and compare the simulation tests with the real behavior of the board.

This work started from studying and analyzing the design concept of AraMiS satellites, papers related to module architecture, and thesis about the project 1B81_Power_Management _Honeycomb. Then a number of updates and designs are applied as a new version for the new requirements. The hardware design is also a one more step to exploit small size, low power and COTS components. It aims to follow all the concept of cubesat with modularity architecture to perform in a more efficient way. What's more, the precious experience of the process of fabricating a PCB board helped us learn through practice.

The main work of the thesis consist in simulate the blocks of the power management honeycomb individually, after check that the output signals were appropriates, the entire block was tested. To achieve the solar signal input, a model of solar cell was created. After achieve the simulation, the board was tested. Some power supplies were necessary to supply the board, and also, a solar cell physical model was required to simulate the solar energy. Once done and doing measurements, some problems appears until achieve the well behavior. Some components were necessary to be replaced and to understand the layout was mandatory to read the wires of the board.

To conclude, can be said that the regulators of the board work well, taking care with the current to not burn the own components. The MPPT also works well, and a future scenario to be developed could be test the board with a real solar panels and with the real solar energy, to ensure a good behavior of the system.

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APPENDIX A – PROJECT SCHEMATICS

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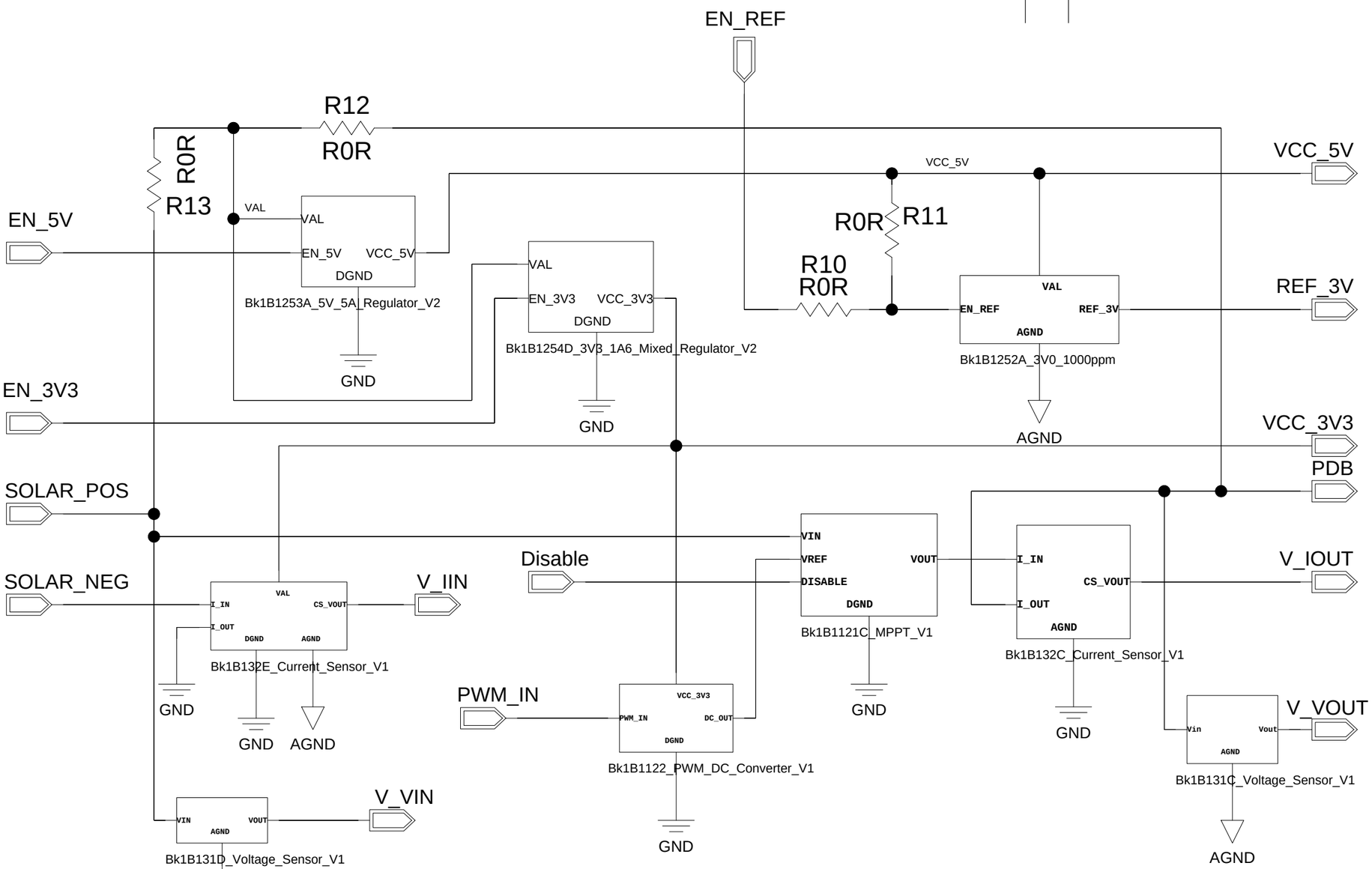

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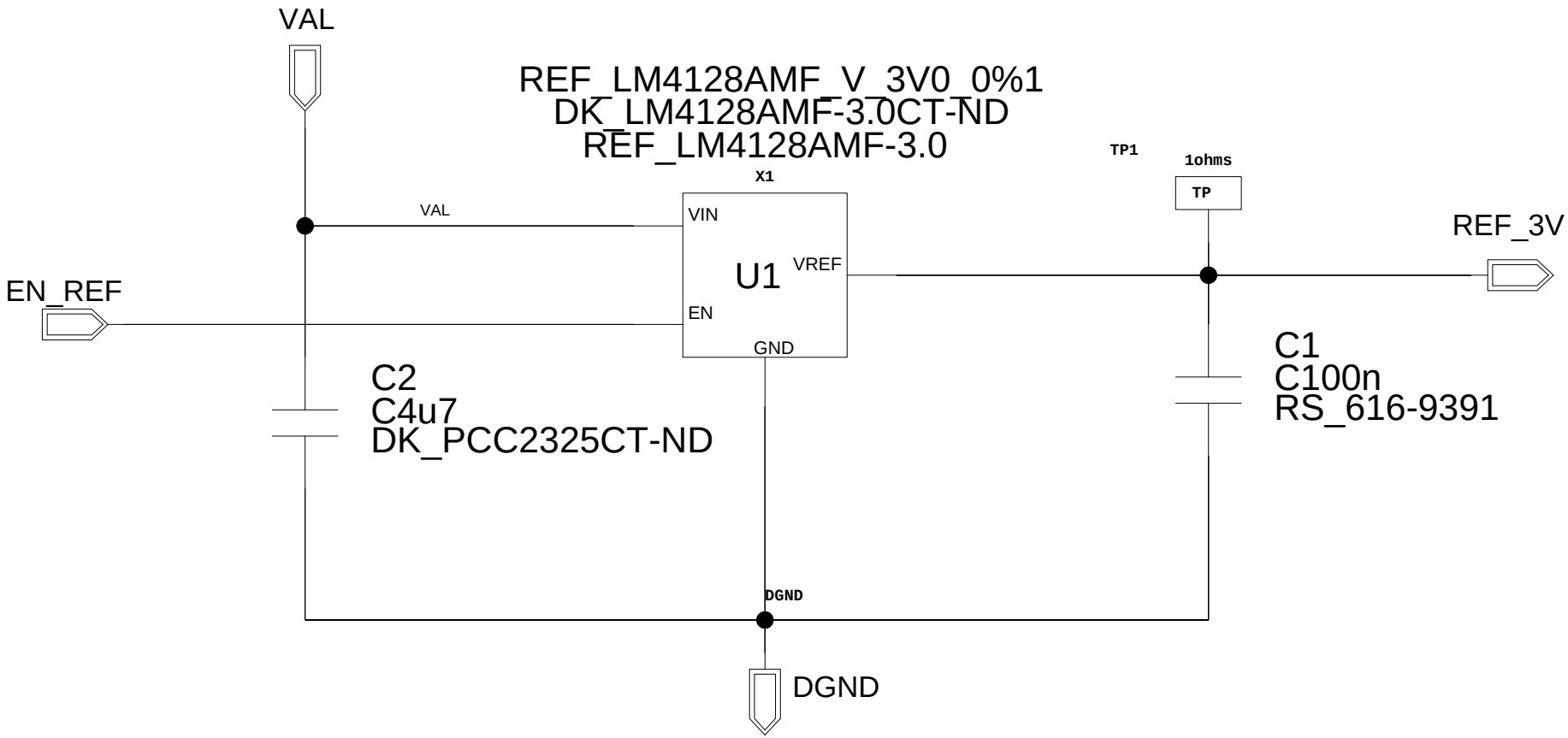

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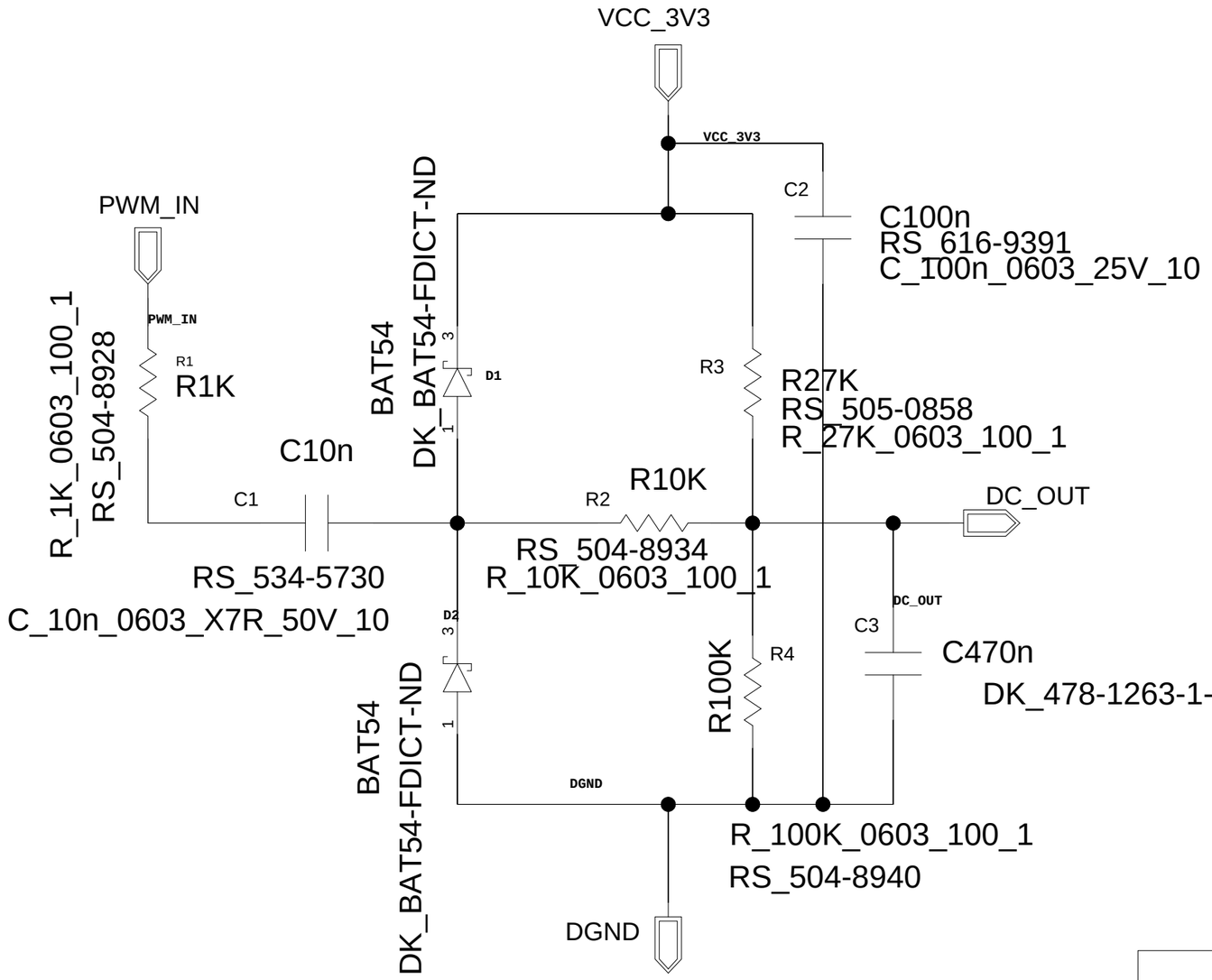

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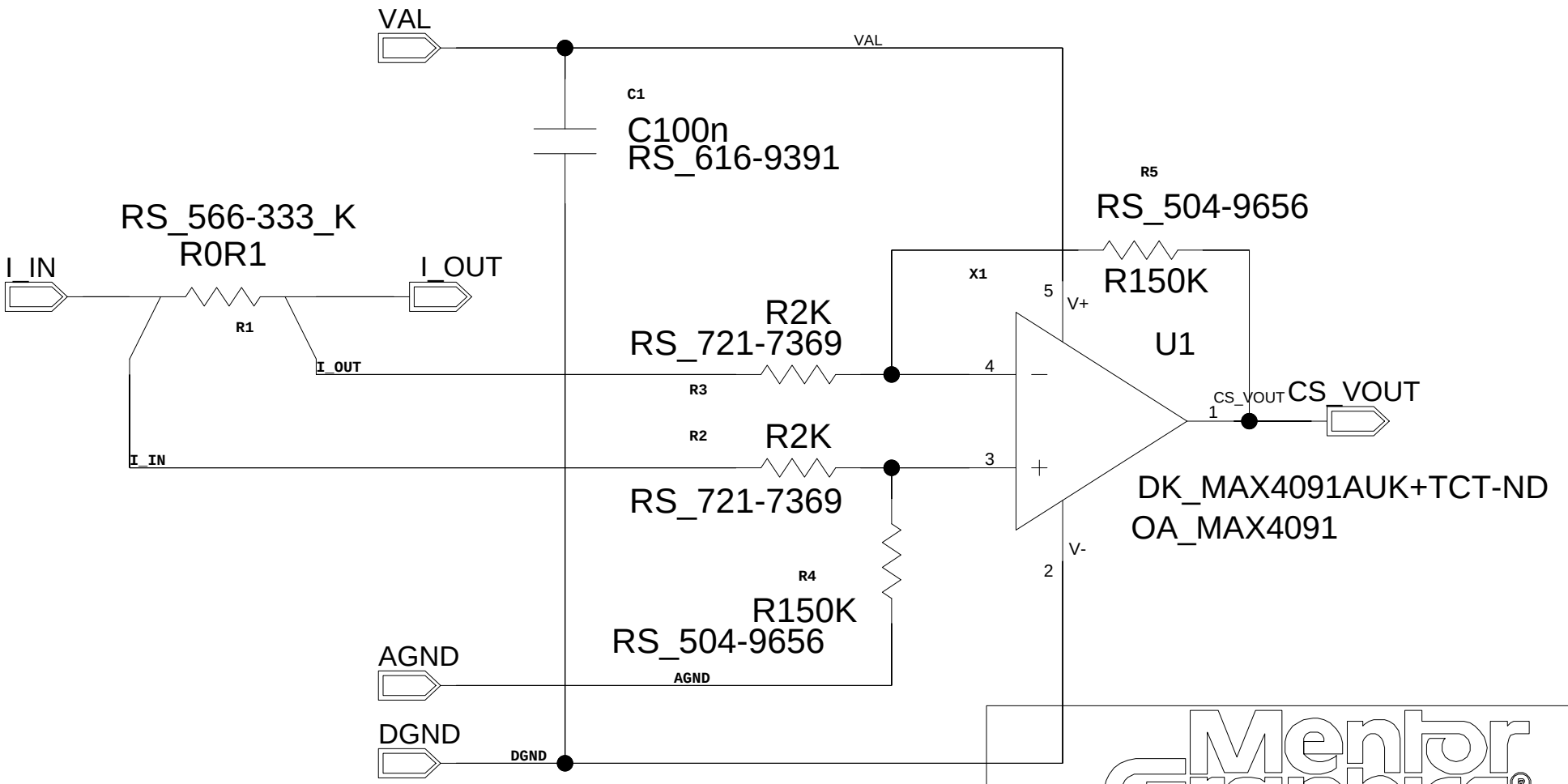

Mentor Graphics®

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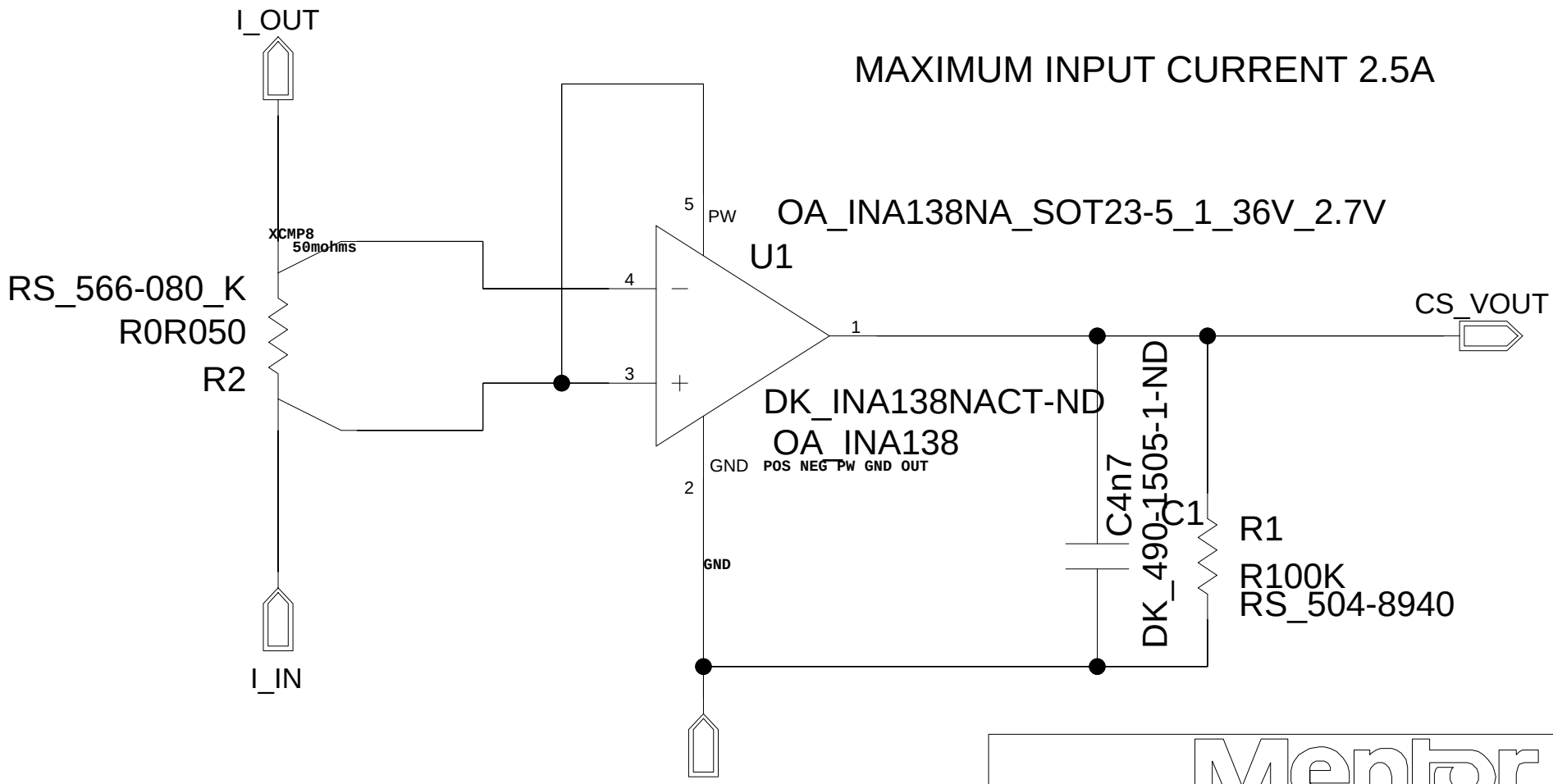

Mentor Graphics®

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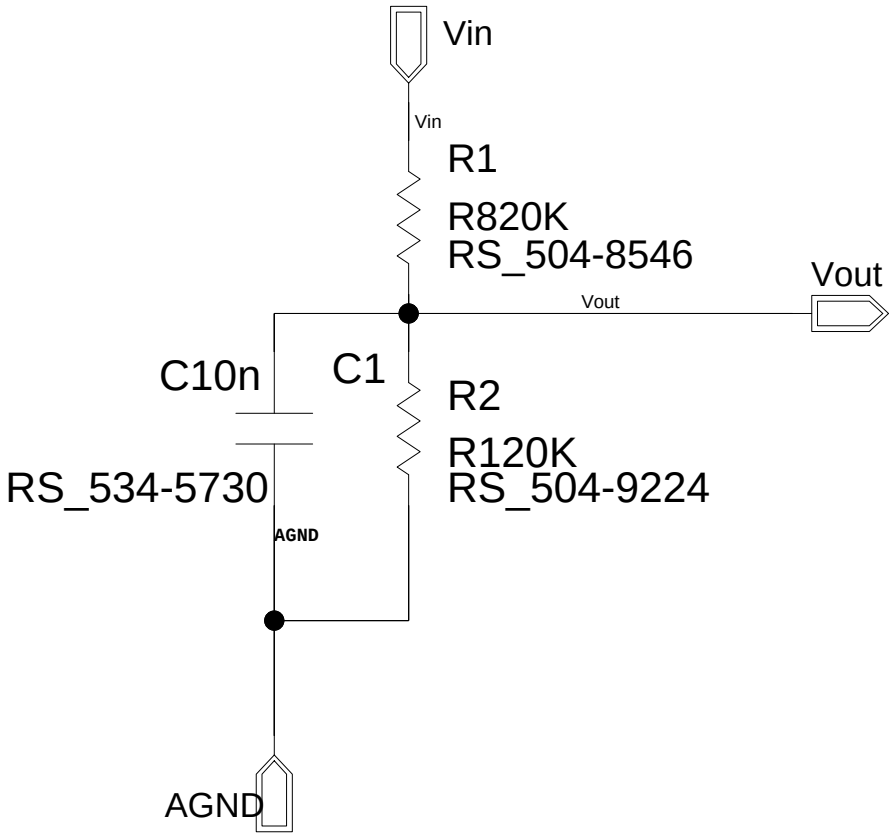

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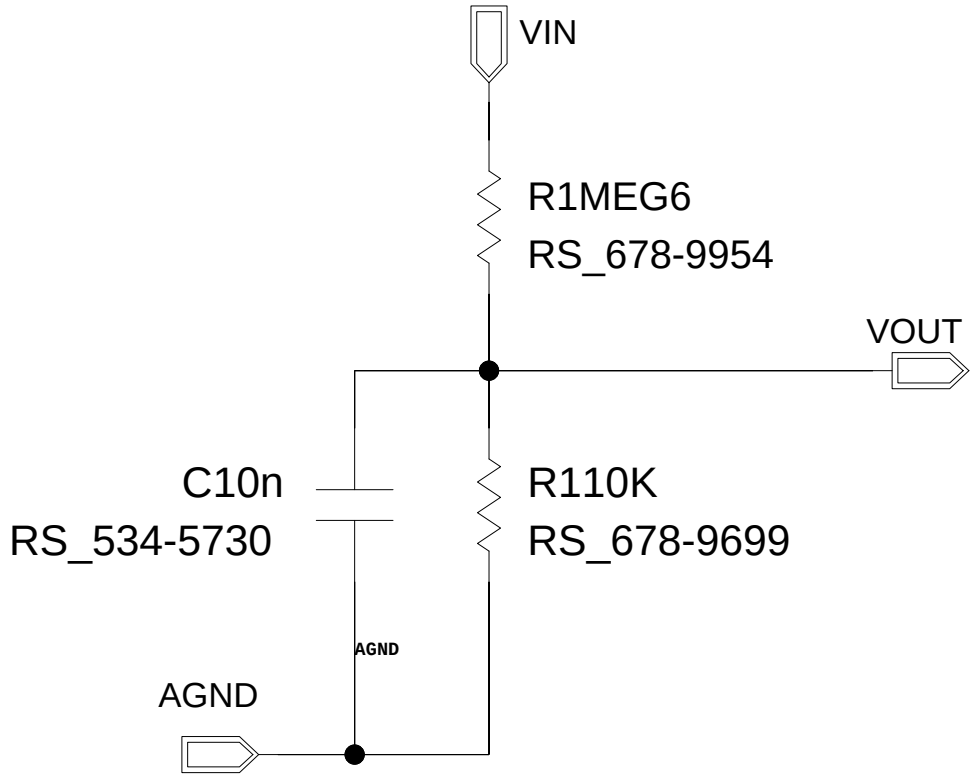

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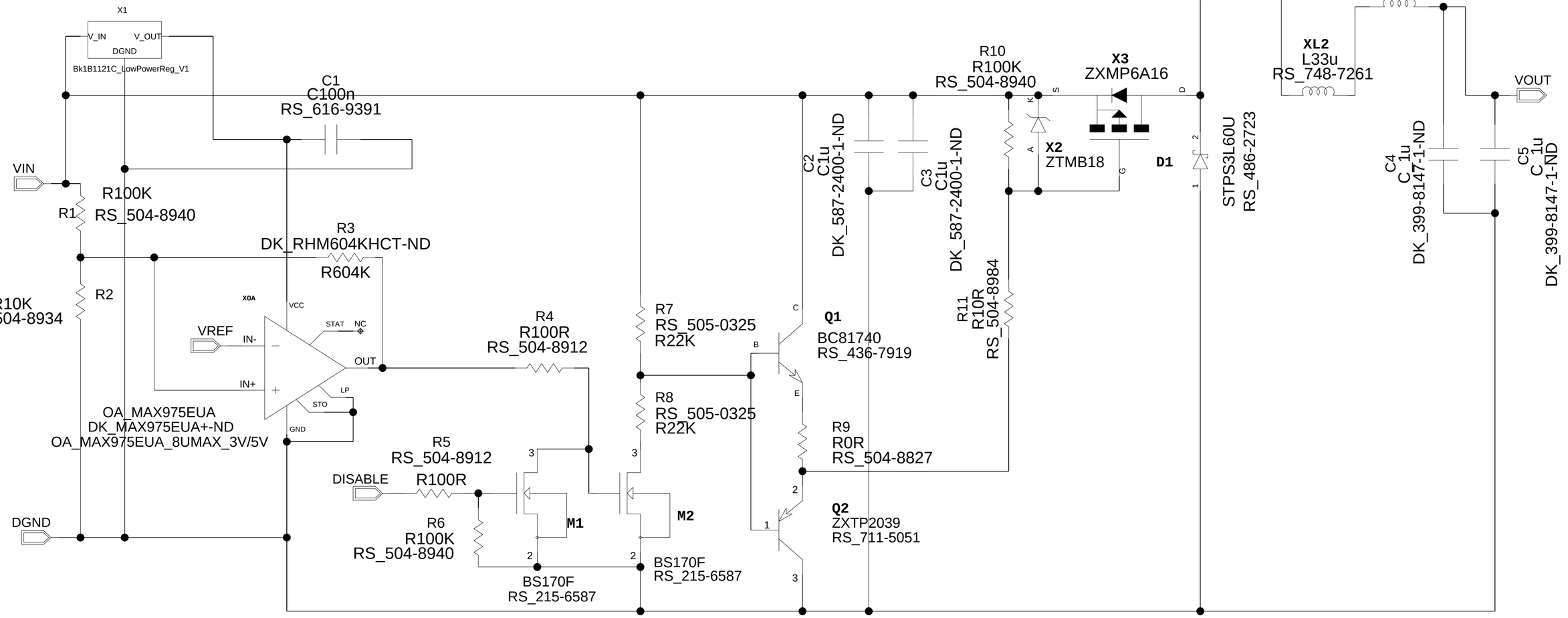

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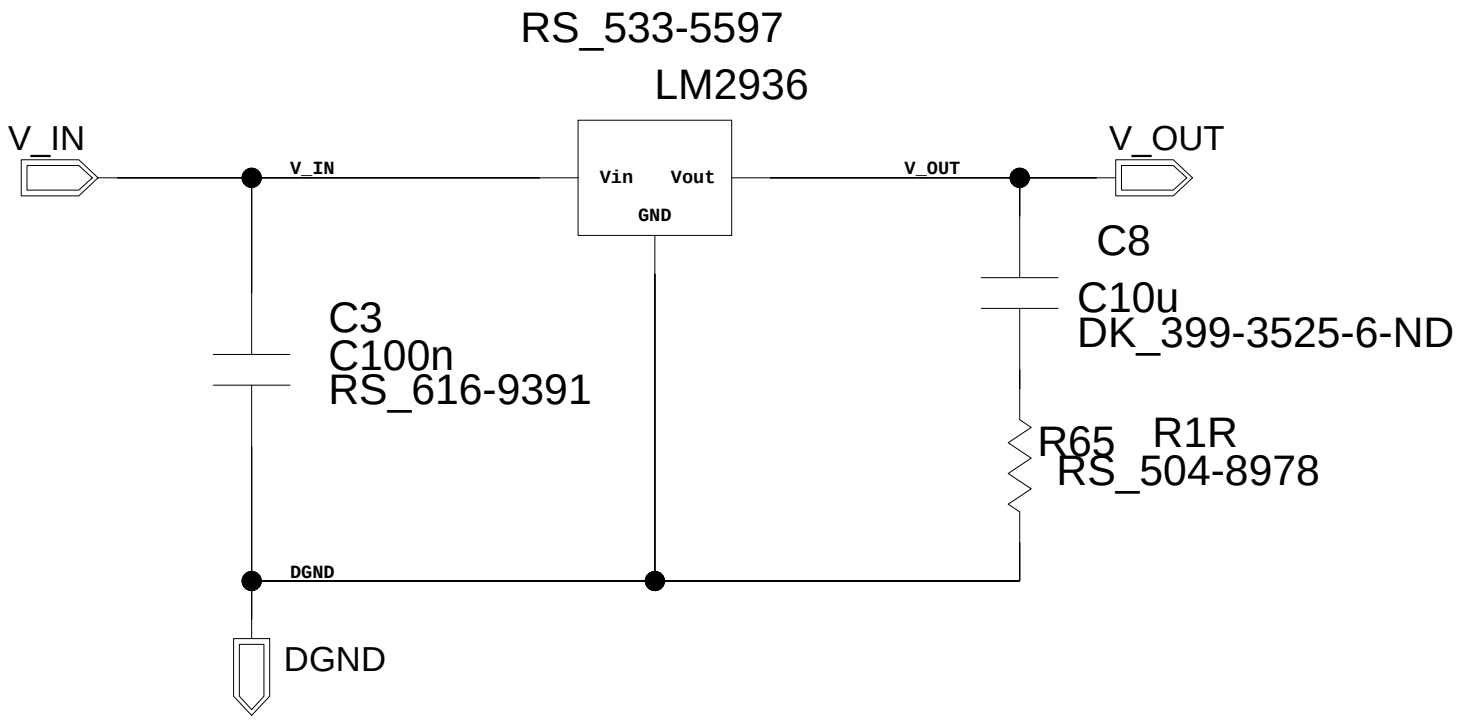

Mentor Graphics®

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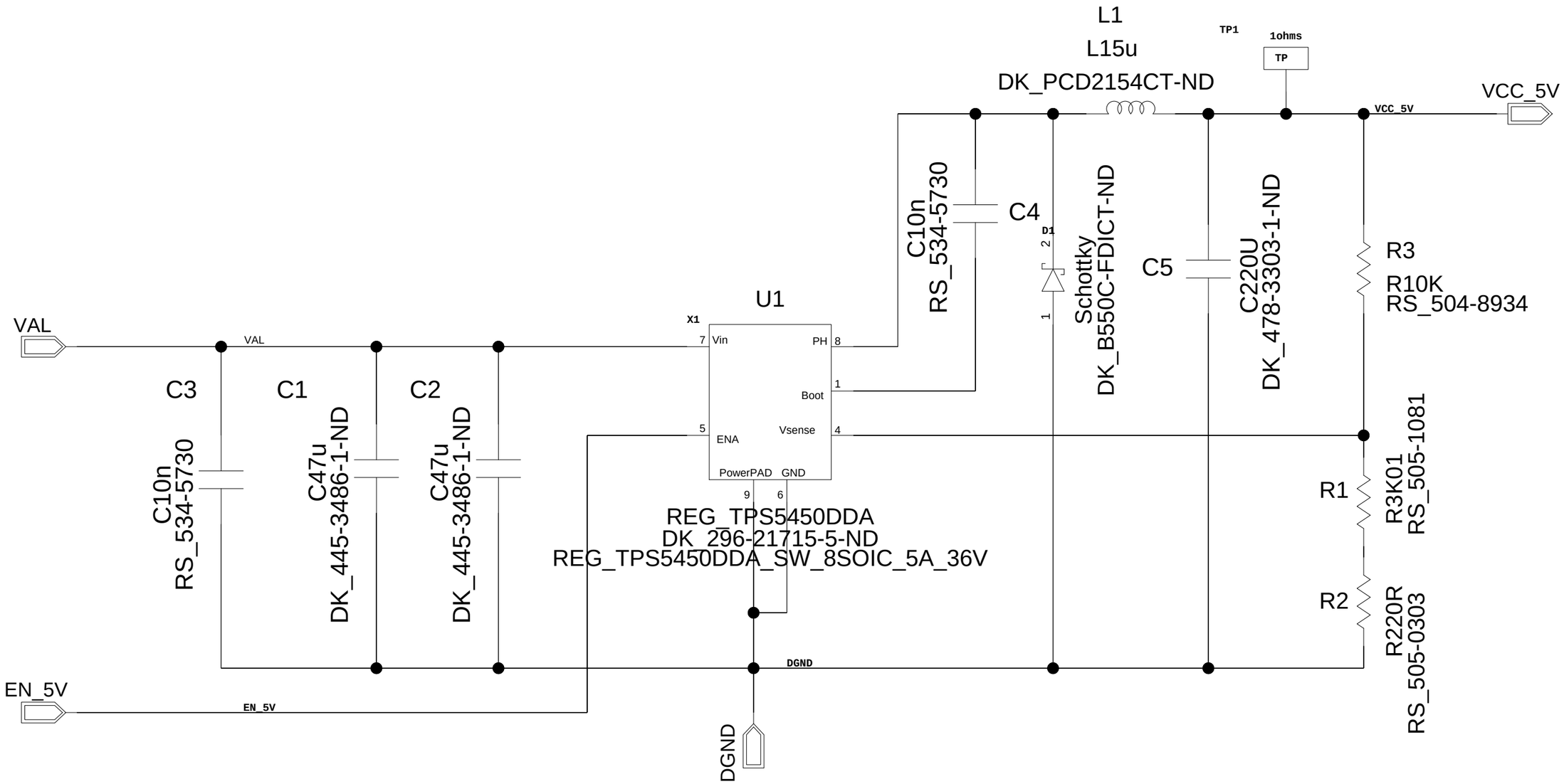

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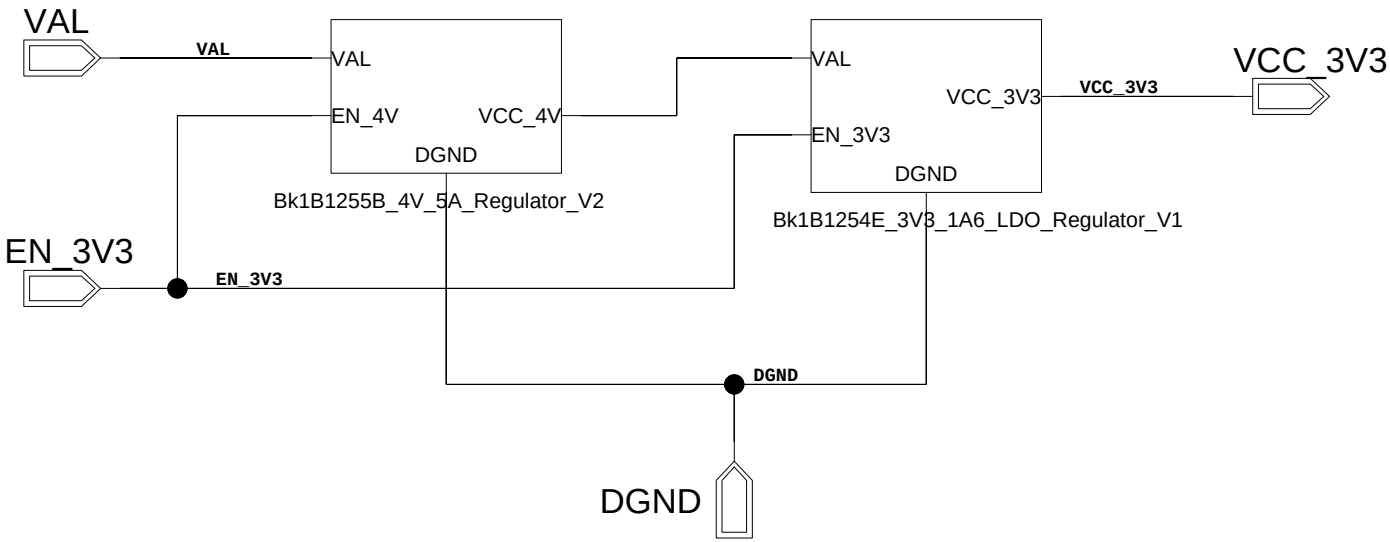

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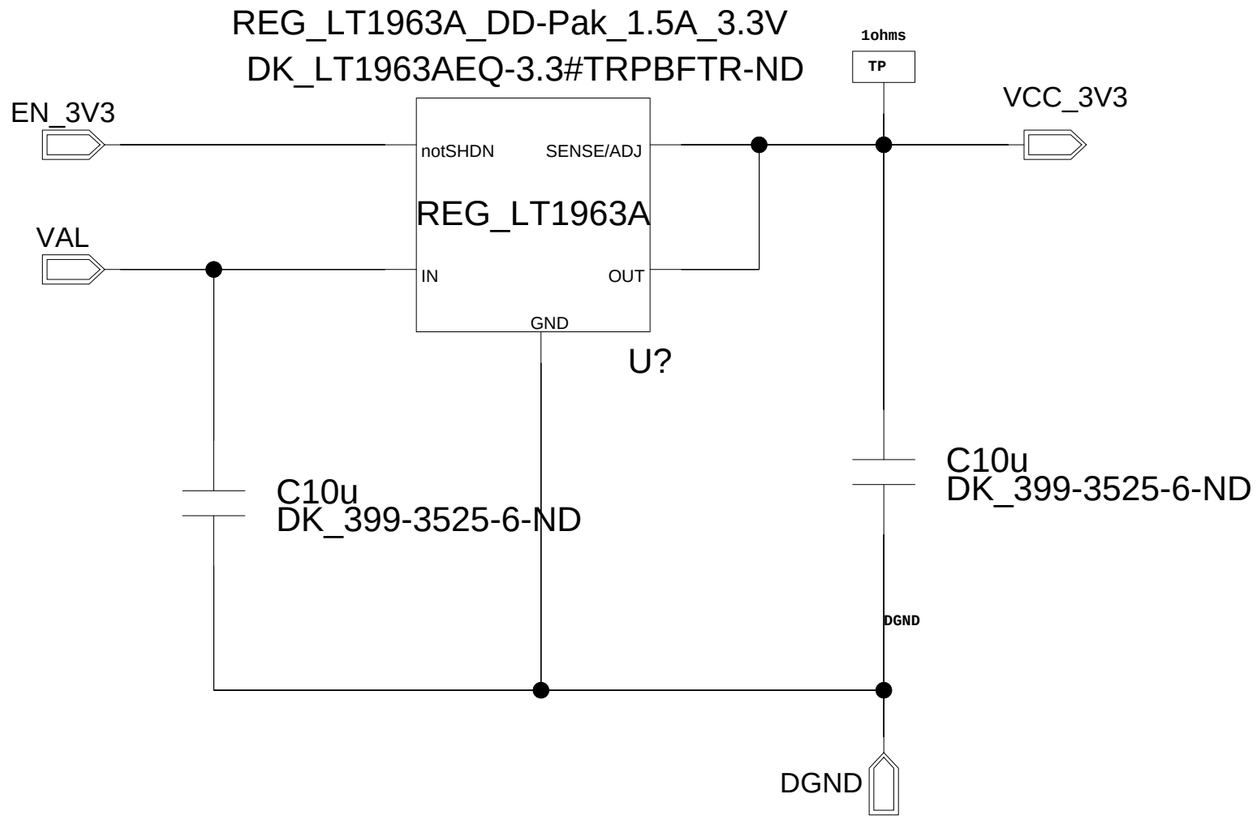

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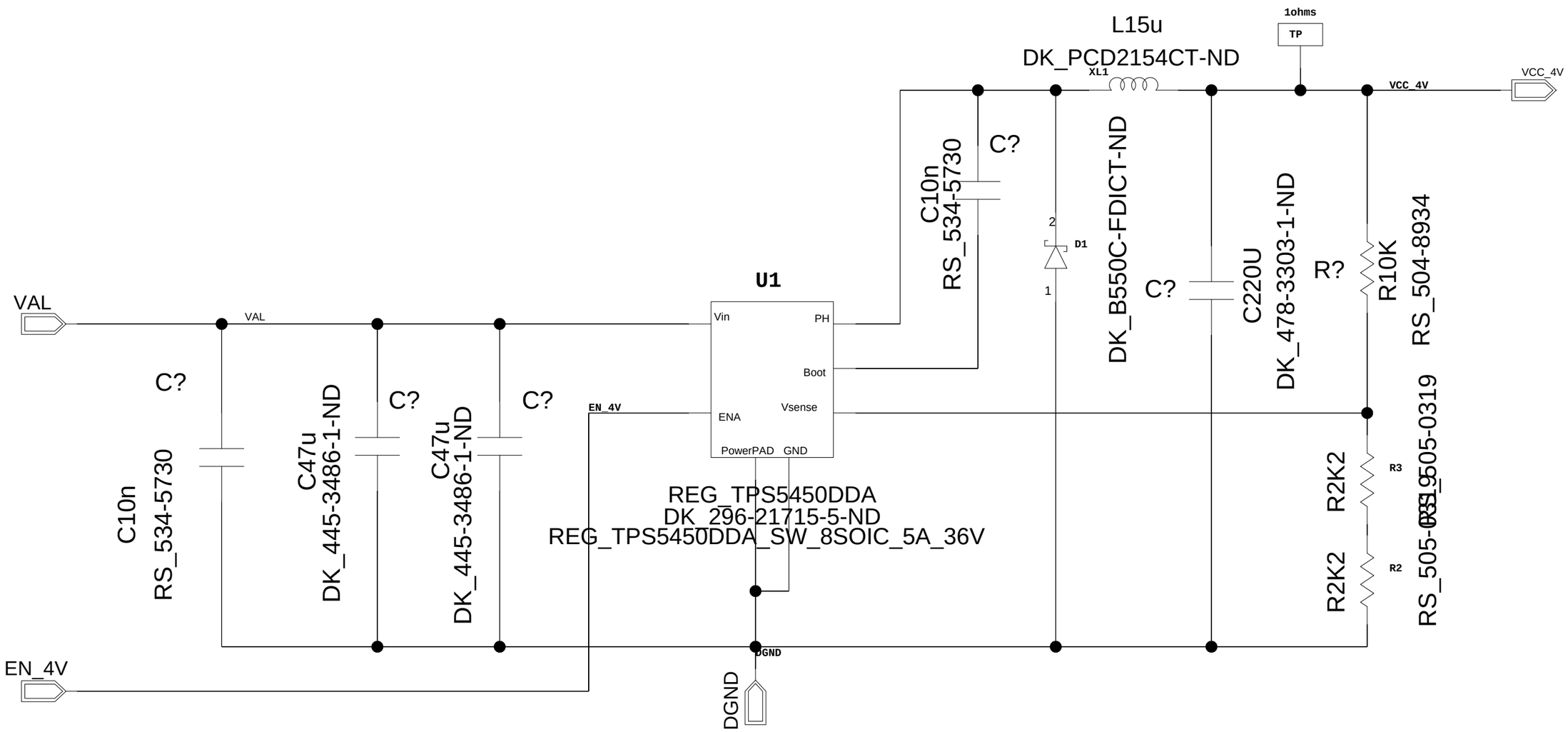

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APPENDIX B – SOLAR CELLS DATA

Collected data of the solar cell test

R_prog.load (Ω)	V (V)	I (A)
500	36.90	0.073
475	36.90	0.077
450	36.70	0.081
425	36.70	0.086
400	36.40	0.091
375	36.40	0.097
350	36.10	0.103
325	35.99	0.110
300	35.99	0.119
290	35.91	0.123
280	35.73	0.127
270	35.73	0.132
260	35.65	0.137
250	35.57	0.142
240	35.49	0.147
230	35.41	0.153
220	35.30	0.160
210	35.19	0.167
200	35.10	0.175
190	34.99	0.184
180	34.90	0.193
170	34.75	0.204
160	34.60	0.216
150	34.47	0.229
140	34.31	0.244
130	34.11	0.262
120	33.87	0.282
110	33.61	0.305
100	33.27	0.332
95	33.11	0.348
90	32.85	0.361
85	32.55	0.383
80	32.23	0.403
75	31.80	0.424
70	31.35	0.447
65	30.64	0.471
64	30.51	0.476
63	30.35	0.481
62	30.18	0.486
61	29.27	0.491
60	29.79	0.496
59	29.55	0.501
58	29.33	0.505
57	29.06	0.510
56	28.75	0.513
55	28.48	0.518
54	27.77	0.523

Points of the solar cell simulation model

V (V)	I (A)
27.37	0.455
27.51	0.455
27.59	0.455
27.79	0.454
27.92	0.454
28.02	0.453
28.13	0.453
28.24	0.453
28.33	0.452
28.42	0.452
28.54	0.451
28.64	0.451
28.78	0.450
28.88	0.449
28.97	0.449
29.10	0.448
29.18	0.447
29.27	0.446
29.38	0.445
29.47	0.444
29.57	0.443
29.65	0.442
29.75	0.441
29.82	0.440
29.91	0.439
29.98	0.438
30.04	0.437
30.12	0.436
30.18	0.435
30.26	0.434
30.29	0.433
30.34	0.432
30.39	0.431
30.43	0.430
30.50	0.429
30.57	0.427
30.68	0.425
30.74	0.424
30.82	0.422
30.88	0.420
30.97	0.418
31.06	0.415
31.14	0.412
31.24	0.409
31.31	0.407
31.43	0.403
31.55	0.398
31.65	0.394
31.77	0.389

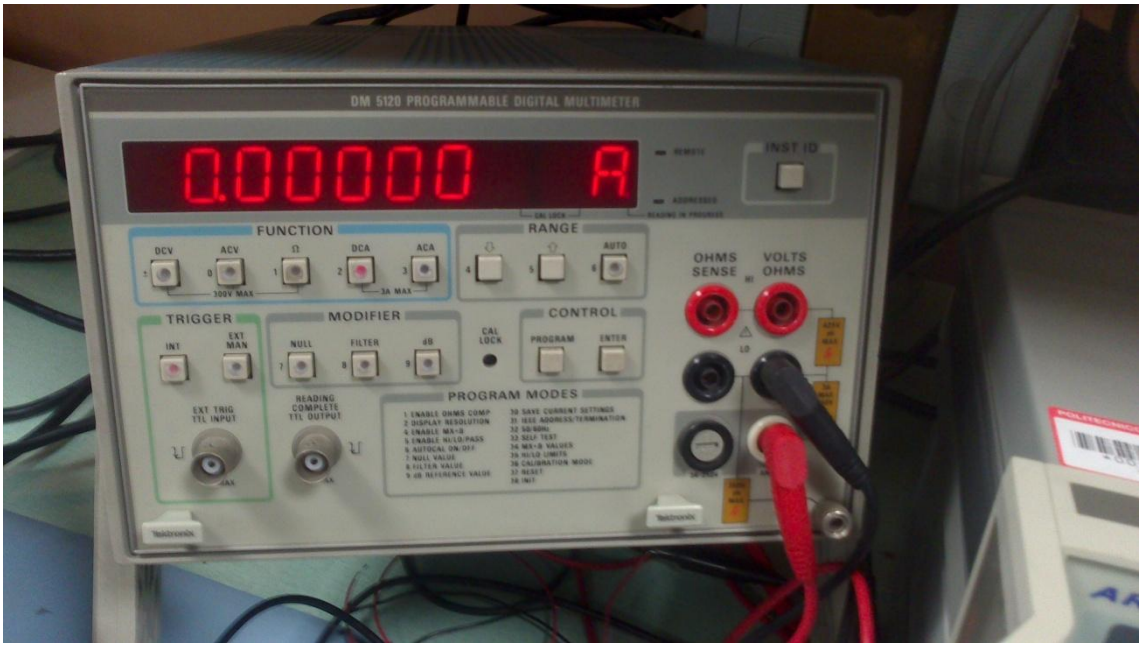
31.86	0.385
31.97	0.380
32.07	0.375
32.19	0.369
32.31	0.363
32.41	0.357
32.55	0.349
32.64	0.343
32.74	0.337
32.88	0.328
32.98	0.321
33.10	0.312
33.20	0.305
33.29	0.298
33.45	0.286
33.54	0.279
33.67	0.269
33.79	0.258
33.90	0.249
33.99	0.241
34.13	0.229
34.27	0.216
34.42	0.202
34.60	0.185
34.76	0.170
34.89	0.157
34.99	0.147
35.13	0.133
35.34	0.111
35.46	0.099
35.55	0.089
35.64	0.080
35.71	0.072
35.79	0.064
35.85	0.057
35.93	0.049
36.05	0.036
36.17	0.023
36.27	0.012
36.32	0.007
36.35	0.003
36.38	0.001

APPENDIX C – IMAGES AND FEATURES OF EQUIPMENT

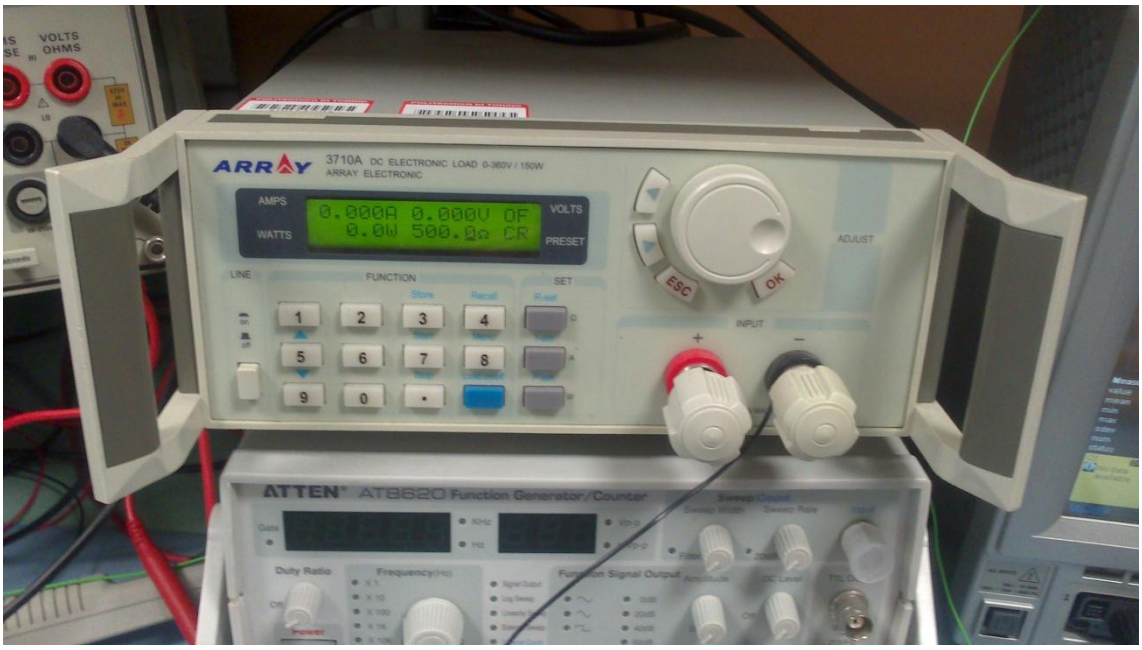
Power supply: ATTEN TPR3003-3C (Triple-Output Regulated DC Power Supplies)

Power supply: GW INSTEK GPC-3030D

Programmable digital multimeter: Tektronix DM 5120

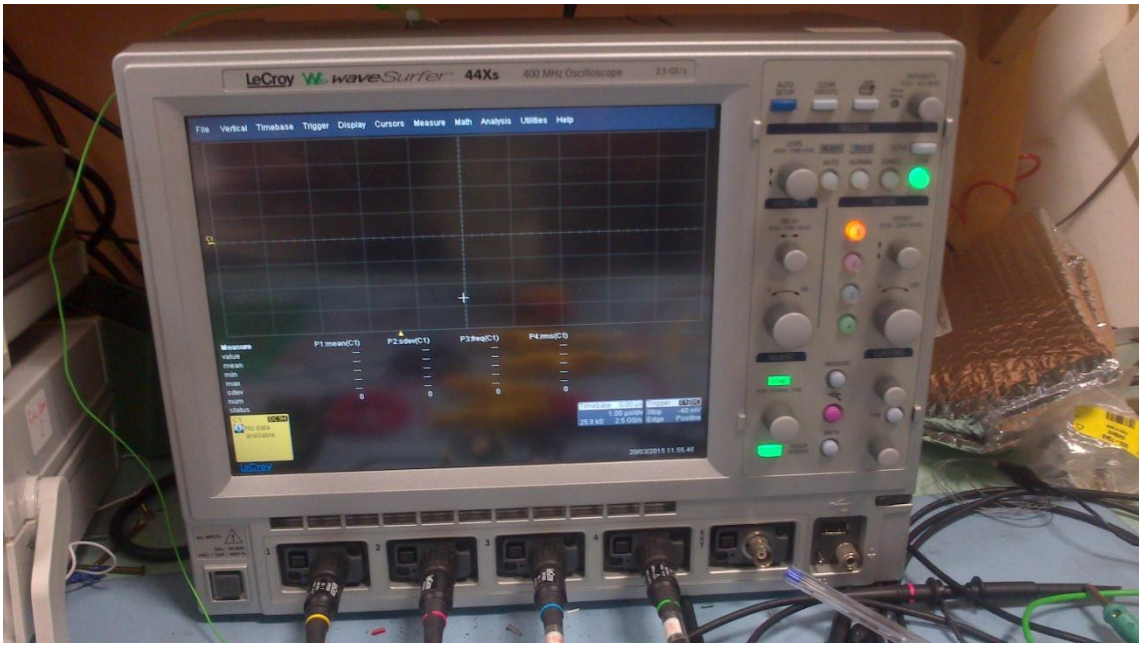


Programmable load: ARRAY 3710A

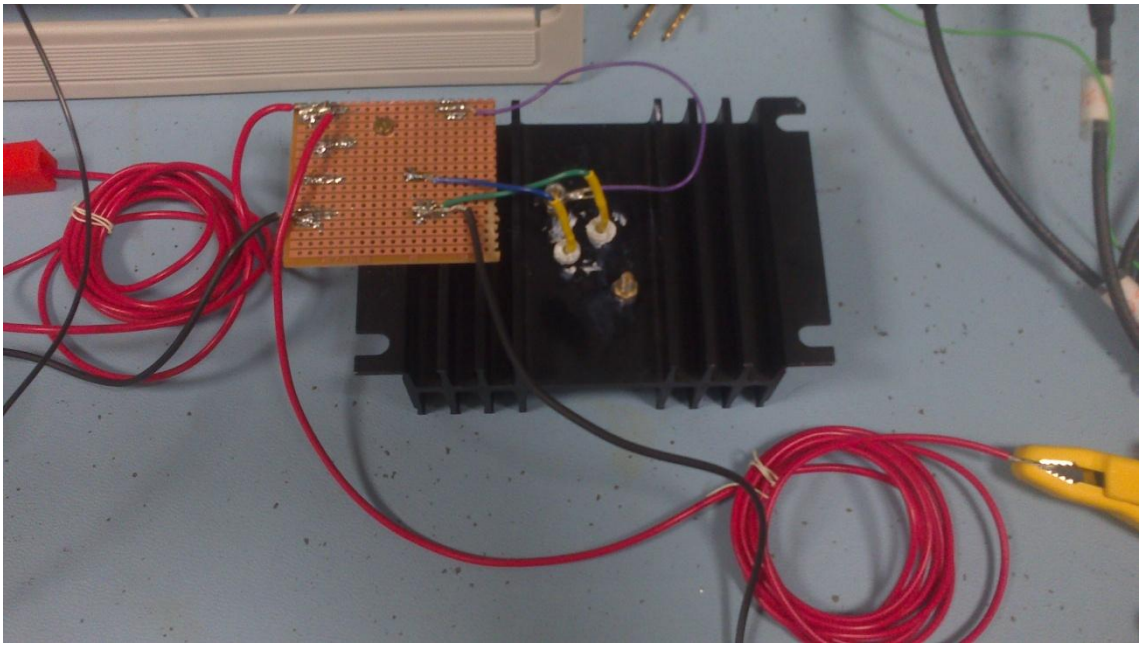


Thermal camera: Fluke Ti10

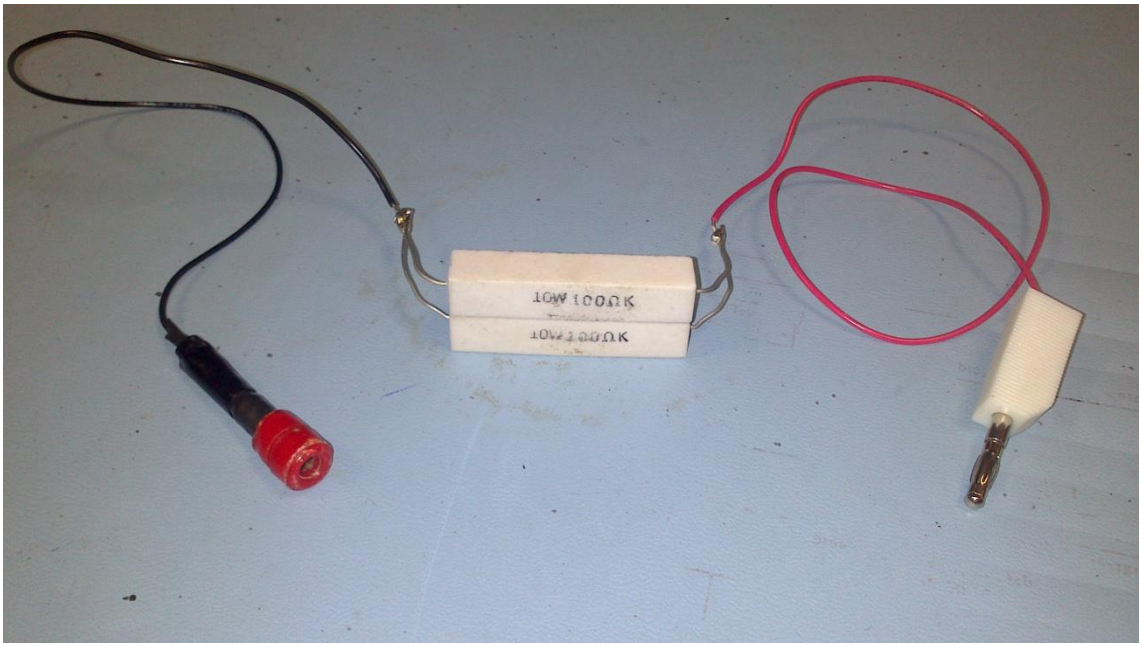
Digital oscilloscope: LeCroy waveSurfer 44Xs



Solar cell



50 Ω resistor



Top and bottom views of solar cell