POLITECNICO DI TORINO

Dipartimento di Elettronica e Telecomunicazioni

Master degree in Electronic Engineering

Master Degree Thesis

Development and testing of a deploying mechanism for the solar panel structure in ARAMIS satellite platform

Supervisor
prof. Leonardo Reyneri

Candidate
Alessandro Di Paola

OCTOBER 2017

Acknowledgements

I would like to thank my friends and my family for being with me on this journey. A special thanks to my father, my mother, Luca and Chiara who have been and will always be my strength.

Contents

List of Tables

Introduction

The small size satellites like ARAMIS platforms are low cost solutions for the creation of several kinds of satellite applications. ARAMIS is a new approach used in CubeSat. Its faces are PCBs that realize all basic features of the satellite and that represent also the physical tiles of the CubeSat. ARAMIS structure can be implemented for different format of CubeSat (1U, 2U, 3U), it is able to bring on board small telescopes, antennas and other; nevertheless these are characterized to have a high power consumption, therefore the faces of CubeSat are not large enough to mount a number of solar panels able to provide enough power to satellite subsystems. For this reason, a solution with deployable solar panels might be used. In the launch phase these deployable structures are closed to avoid vibration. After the expulsion from the P-POD module, the solar panels' structure is deployed once in orbit and in this way the total surface of satellite exposed to the sun is increased, therefore also the power. The deployable solar panels are a solution that can be adapted to all CubeSat configurations.

The designing of the deploying mechanism, (that allows to open the solar panels' structure), and the test board where it is placed, is the target of my work. The thesis deals with the mechanical as well the electrical part of test board focusing on the compatibility with ARAMIS structure. Trough *Altium Design* the PCB has been developed. First of all the circuit has been described through the creation of a blocks diagram in order to describe the behaviour of the entire system. This operation has been followed by the physical realization of the board taking into account the right positioning of components. All elements that form the PCB are chosen considering the worst case in order to guarantee correct operation. Attention has been paid at the deploying mechanism used to detach the fixing wires. They keep closed the solar panels' structure, during the launch, before passing the atmosphere and entering in orbit. The UML language has been used to describe main operations and for the design phase. All the main blocks have the corresponding UML class. All these classes are referred to Bk1B6711 and 1B111E sections of the ARAMIS project of the Polytechnic of Turin.

Chapter 1

Abstract

The Bk1B6711 is the test board that allows the detachment of the deployable solar panels' structure, called 1B111E. This remains closed during the launch phase, after the expulsion of the satellite from P-POD module, the *thermal fusers* on the Bk1B6711, have been used to detach the fixing wires that maintain the tiles of the deployable structure folded. In this way the solar panels' structure is deployed through an elastic mechanism.

First of all the 1B111E has been studied, paying particular attention at the connection that must be made to attach the structure to Bk1B6711 Test Board. Two spacers should be mounted in the opposite side to guarantee that the deployable structure does not touch the Test Board. It should handle the two power channels coming from two side of the deployable structure. Second of all, the concept of thermal fusers can be introduced. A mechanism of eight CuBe wires with 0.3 mm of diameter has been developed in order to folded the 1B111E. The choice of material has been made considering the tensile strength and the force due to the acceleration in the launch phase. A thermal analysis has been made considering the electrical model in order to achieve the melting temperature of the tin where the wire is soldered. The idea of the thermal fusers is that a current passes through a resistance to produce heat due to Joule effect. Using the 14 V PDB and 1.5 W required, it is possible to find the current needed to produce enough heat to melt the tin where the CuBe wire is soldered. The value of current found is 107 mA, therefore the resistance equivalent is 131 Ω. Two configurations are possible: Parallel and Series. Besides the fact their resistance values are different they also have different reliability to failure. In series configuration, if one or both of the resistors are detached from the weld because of the temperature or vibrations in the launch phase, it does not pass any current and therefore no more heat is produced by Joule effect. In the parallel configuration, however, if a resistance is damaged or disconnected and the other one is connected, it is always a source of heat that could be able to detach the wire and allow the deployment of the solar panels' structure. The command that allows the

current to pass through the resistances must be sent when the satellite is pushed out from the P-POD module, so it is necessary to use a microcontroller. However, this can not control directly the thermal fusers with a 107 mA current, so a drive circuit has to be designed. If the temperature increases too much, it can produce catastrophic failure of the mission. This situation can cause the detachment of the resistors and produce debris and a series of short circuits. In order to avoid this, a NTC temperature sensor has been inserted. In this way a feedback control checks the temperature of the resistances. The NTC sensor varies its electrical resistance parameter according to the temperature variations. A linearization circuit composed by two resistance is needed to avoid the non linear behaviour of the sensor.
The subsystems of Bk1B6711 Test Board need several power supply voltage to work properly. The 14 V PDB must be adjusted to have different values of power supply and therefore the Test Board needs three voltage regulators. The microcontroller requires a power supply of 3.3 V while the linearization circuit for NTC needs a power supply of 3 V. The regulators provide 3.3 V, 5 V and 3 V, and these voltage levels can be used also for other satellite subsystems.

The physical test board has been created to be fixed to the skeleton of CubeSat. For these purpose the board has dimension 98x82.6 mm and eight holes, four for each shorter sides. The wires that pass through other eight holes keep the solar panels' structure closed. This number is necessary because the vibrations in launch phase can destroy the structure and therefore the mission may fail. For this reason the thermal fusers must be positioned in specific points on the Bk1B6711 Test Board. The position of others components has the only restriction of not being too high. If they are, they can touch the deployable solar panels' structure and thus damage it; for this reason the components higher than the spacers must be soldered in the bottom side of the test board. Thus, connectors, microcontroller, the power management system and their components have been positioned in the bottom side. The Bk1B6711 Test Board is composed of 4 layers, where the internal planes are used for PDB and GND. These do not reach the area where the eight thermal fusers are positioned in order to avoid interferences to the melting of the tin where the wire is soldered and the temperature measured by the NTC. Afterwards, the Gerber file and the bill of material have been generated.

In conclusion the Bk1B6711 Test Board can be integrated in the faces of CubeSat to deploy the solar panels' structures. The thermal fusers solution can be used for all the CubeSat configurations.

1.1 Problem statement

The principal goals of the thesis are the designing of the deploying mechanism and the realization of a test board able to release the deployable solar panels' structure. The space reduction is another target, in this way it is possible to integrate into the board other functions easily. The Bk1B6711 Test Board represents the reference for tiles that should be compatible with deployable solar panels. Thus, to guarantee the correct behaviour of the structure 1B111E, it should be mounted on Bk1B6711 Test Board.
Electrical part has been made following particular rules such as avoiding detachment of small parts in orbit and too high temperature due to the *thermal fusers*. They are the deploying mechanism and therefore the main part of entire system. The deployable phase is based on a microcontroller, because the thermal fusers can create problems on other components of the circuit.

1.2 Proposed solution

The Bk1B6711 has been made to be compatible with ARAMIS tiles (98x82.6 mm), so scalability and modularity approach has been followed. The deployable structure should be mounted above the test board. The proposed solution is to develop a deploying mechanism and the test board able to deploy the solar panels' structure. The figure 1.1 shows a conceptual design of the Bk1B6711 Test Board. Eight thermal fusers have been used to detach the wire that keeps the deployable structure closed.

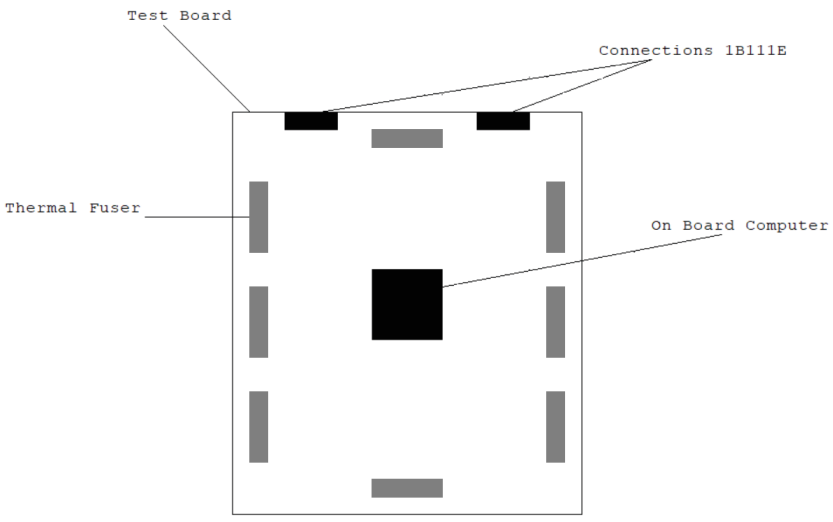


Figure 1.1. Design of the Test Board

1B111E is composed by three tiles 1B111E20, where two solar panels are mounted for each side. Since four deployable structures should be attached on the CubeSat, the Bk1B6711 will form four faces of the satellite. The test board has been made using components easily findable on market. They are selected considering the small dimensions, weigh and prize. Obviously, these components have been chosen to guarantee the proper operation of the board in space.
The 1B111E starts folded, mechanical springs are employed to maintain the structure in charge. After passing the atmosphere, thermal fusers have been used to detach the fixing wires that keep the deployable solar panels structure closed. Thus the thermal fusers allow the realise of the 1B111E.
The test board Bk1B6711 used to test the deploying mechanism has been made following functional, electric and mechanical specifications required to be compatible with standard panels of the CubeSat. First of all physical structure of the board as been made using *Solid Works* and then it has been imported in *Altium Design*. The components have been chosen considering electrical and functional specifications. At the end, they are distributed on the board to guarantee the correct behaviour of the entire structure.

1.3 Specifications

The main specifications are analyzed in this paragraph, they are related to the implementation of the system on 1U CubeSat satellite. This section is divided in functional and electrical requirements to better understand all the main specifications needed to the system.

1.3.1 Functional and Mechanical specifications

The functional and mechanical specifications are the requirements that the system needs to work properly.

- Bk1B6711 Test Board should be able to deploy a 1B111E structure composed by three tiles 1B111E20. This is the main requirement for the entire system.
- Bk1B6711 Test Board should be compatible with ARAMIS CubeSat skeleton tile. Four holes are needed to secure the Test Board on the CubeSat structure. Each face of the satellite and therefore Bk1B6711 test board must have dimension 98x82.6 mm. Two holes has been made for each shorter side and no holes in the long ones, according to the figure 1.5.
- Components, on top side of Bk1B6711 Test Board, should not be too high ($<$ 2mm) in order to do not touch the 1B111E deployable structure. This requirement is for P-POD module compatibility.

- The *thermal fusers* system control should be integrated on the Test Board. In this way the system works independently.
- Bk1B6711 test board must have two holes on the side where 1B111E structure is mounted in order to permit the installation of hinges that allow the deployment of solar panels structure.
- Bk1B111E21 are spacers that should be mount in the other side where the deployable solar panels' structure is not fixed in order to avoid the touching between the test board and the 1B111E structure. In this way the 1B111E is parallel at the Bk1B6711 test board and thus at CubeSat's face. For this reason two holes should be added.

1.3.2 Electrical specifications

The electrical specifications involves all the requirements related to electrical parts of the Bk1B6711 Test Board.

- Flexible cables should be compatible with those of 1B111E deployable solar panels' structure.
- Bk1B6711 Test board has to handle two different power channels coming from the sides of the structure 1B111E. Each power channel is composed by six solar cells.
- Bk1B7611 must have eight thermal fusers according to the holes of the solar panels' structure. They must be eight to keep the 1B111E firmly closed in the launch phase, in order to avoid damage to the deployable solar panels' structure due to the vibrations.
- Each thermal fuser should generate 1.5W to disconnect the wire with a power supply voltage of 14V.
- A temperature control should be included in the Bk1B6711 system to avoid overheating and therefore detachment of components.
- The opening system, composed by eight thermal fusers activated, has a maximum power consumption of 15W.
- The melting temperature of the tin where the fixing wire is soldered, is 160°C. This temperature should be reached by eight thermal fusers in 10 seconds.
- The entire opening system composed by eight thermal fusers activated should have a maximum energy consumption in 10 seconds of 150J.

1.4 P-POD Compatibility

The launch is a very critical phase. If it is not properly managed the whole mission fails. The P-POD module (*Poly Picosatellite Orbital Deployer*) is a rectangular box with a spring mechanism capable to release the inner CubeSats. In general the P-POD can contain three CubeSat satellites at time. These ones are insert inside the box until the launch vehicle reaches the orbital altitude and the release point. Then the CubeSat satellites are pushed out by mechanical springs. Figure 1.2 and 1.3.

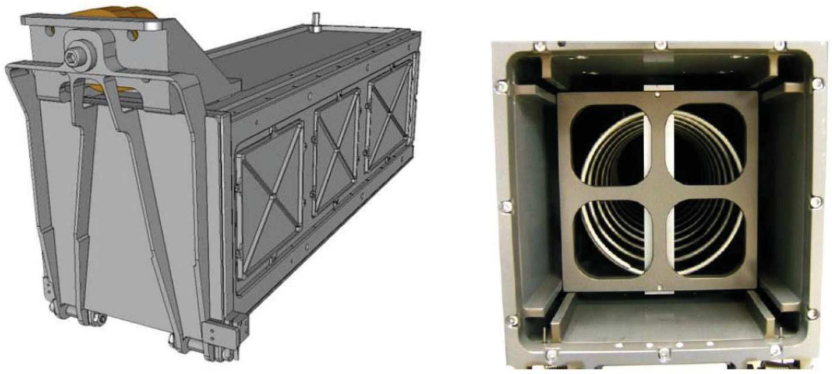


Figure 1.2. P-POD module and cross section

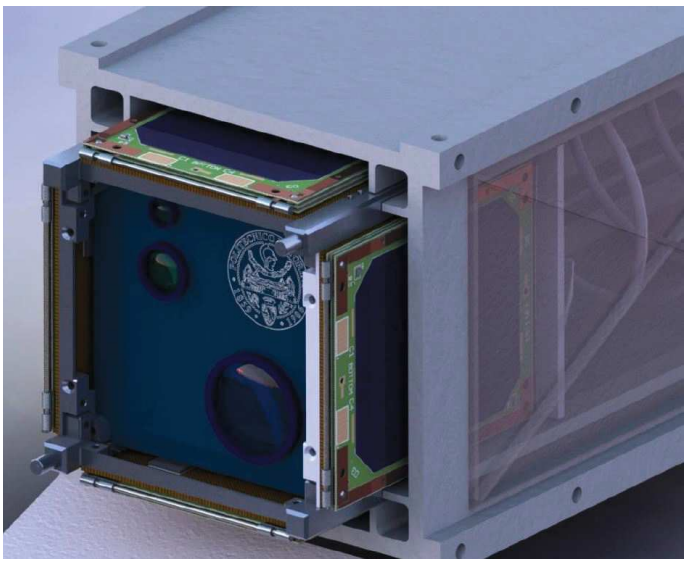


Figure 1.3. ARAMIS CubeSat inside P-POD module

The CubeSat should be compatible with the P-POD module to ensure safety

and success of the mission. The test board of deployable solar panels' structure has been developed to keep the structure closed in order to insert the satellite smoothly in P-POD module. A small space, between the solar panels and the structure of the P-POD module, has been left to avoid damage due to vibrations in the launch phase. For this reason, the entire deployable solar panels' structure has been composed by only three 1B111E20. The Bk1B6711 Test Board should respect two restrictions in order to be guaranteed that the CubeSat can be insert in the P-POD module. The deployable solar panels' structure does not be higher than 5mm and the component in the test board do not be higher than 2mm. These specification should be respect in order to insert the CubeSate in the P-POD module and to avoid damage of the 1B111E . The figure 1.4 shows these two requirements.

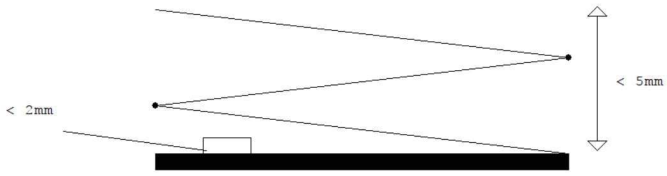


Figure 1.4. P-POD compatibility

The ARAMIS CubeSat skeleton is the structure where PCBs are mounted to create the satellite. The CubeSat is pushed out from the P-POD module by two mechanical springs when the appropriate height is reached. Four holes on each side have been used to fix the test boards forming the faces of satellite. Figure 1.5. The size of the skeleton is totally compatible with the P-POD module.

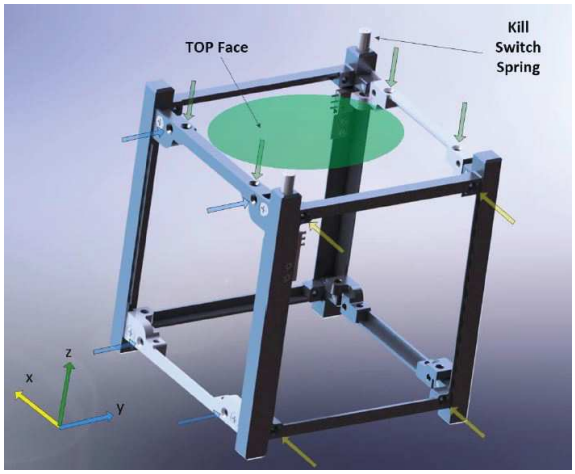


Figure 1.5. ARAMIS CubeSat skeleton

Chapter 2

Deployable Solar Panels Structure

The 1B111E is a structure of solar panels used in the CubeSat to achieve greater power than the solution without deployable structure. The generic satellite is composed of six faces where each one has two solar panels, the deployable structure increases the number of PCBs where the solar panels can be fixed. Since the deployable structure consists of three PCBs, the total number of photovoltaic panels becomes six for each side of the 1B111E. However, it is not mounted on each side of CubeSat but only on four.The faces of satellite where the deployable solar panels' structure is mounted, will be the Bk1B6711 test boards used to deploy the 1B111E.

2.1 Deployable structure configurations

Since standard tiles are modular, it is possible to compose the deployable structure with an indefinitely number of tiles, but due to the limit space of P-POD module, in order to stay under the tolerance margins, the deployable structure of solar panels is composed by a maximum of three tiles.
Three are the main configurations in strict relation with a single Bk1B111E20 and they are designed one for each type of face, as shown in figure 2.1. The three configurations are:

- Bk1B111E17_DepStruct_AAAf_Config
- Bk1B111E18_DepStruct_AwAAf_Config
- Bk1B111E19_DepStruct_BBBf_Config

The configurations are characterize by type of tile used, starting from left to right, in order of mounting. It means to go from the tile attached to the side of CubeSat to the terminal tile of the deployable solar panels' structure.

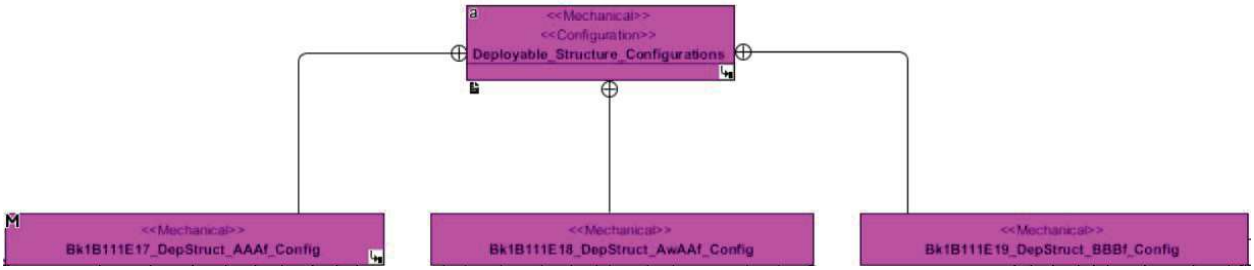


Figure 2.1. Configurations of deployable solar panels' structure

The configuration used in this thesis is the Bk1B111E17_DepStruct_AAAf_Config. This means a structure composed by three tiles: starting from side attached on the CubeSat, the first standard tile is A, the second is A and the final is Af. The figure 2.2 shows an example of AAAf configuration. Its orientation reflects the previous description.

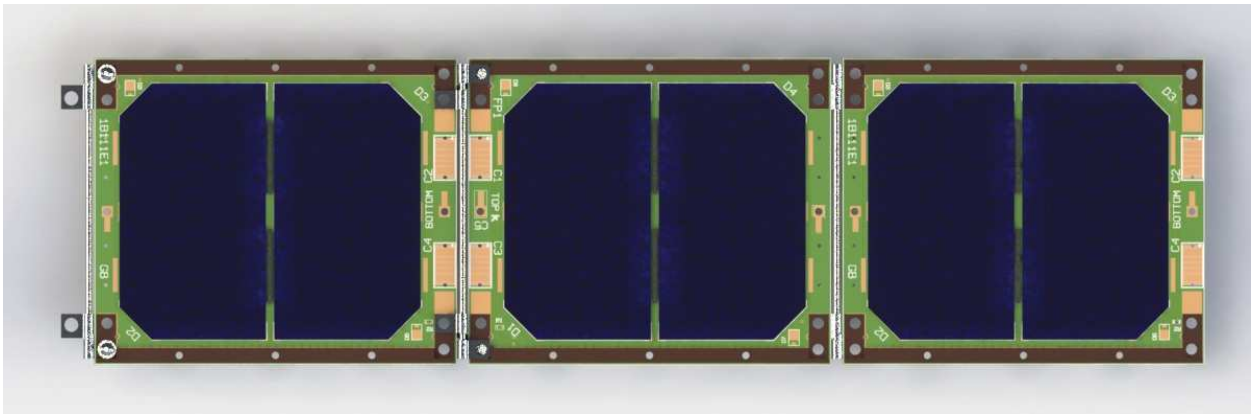


Figure 2.2. Deployable structure configuration AAAf

The first and second tile are the same, but the middle one is mounted in opposed way. By doing this, the tiles are fully compatible and the hinges do not change.

2.1.1 Bk1B111E17_DepStruct_AAAf_Config

The UML class of Bk1B111E17_DepStruct_AAAf_Config contains the main components of the structure. A simplify class diagram has been chosen to describe the AAAf configuration, as it is shown in the figure 2.3. The main components are two A and one Af tile, each one have Bk1B111E3_HingeFem_B, Bk1B111E3_HingeFem_A,

four solar cells and a Bk1B111E20_DepTilePanel_1U. The last one is the base standard tile used as mechanical structure to assemble each type of configurations.

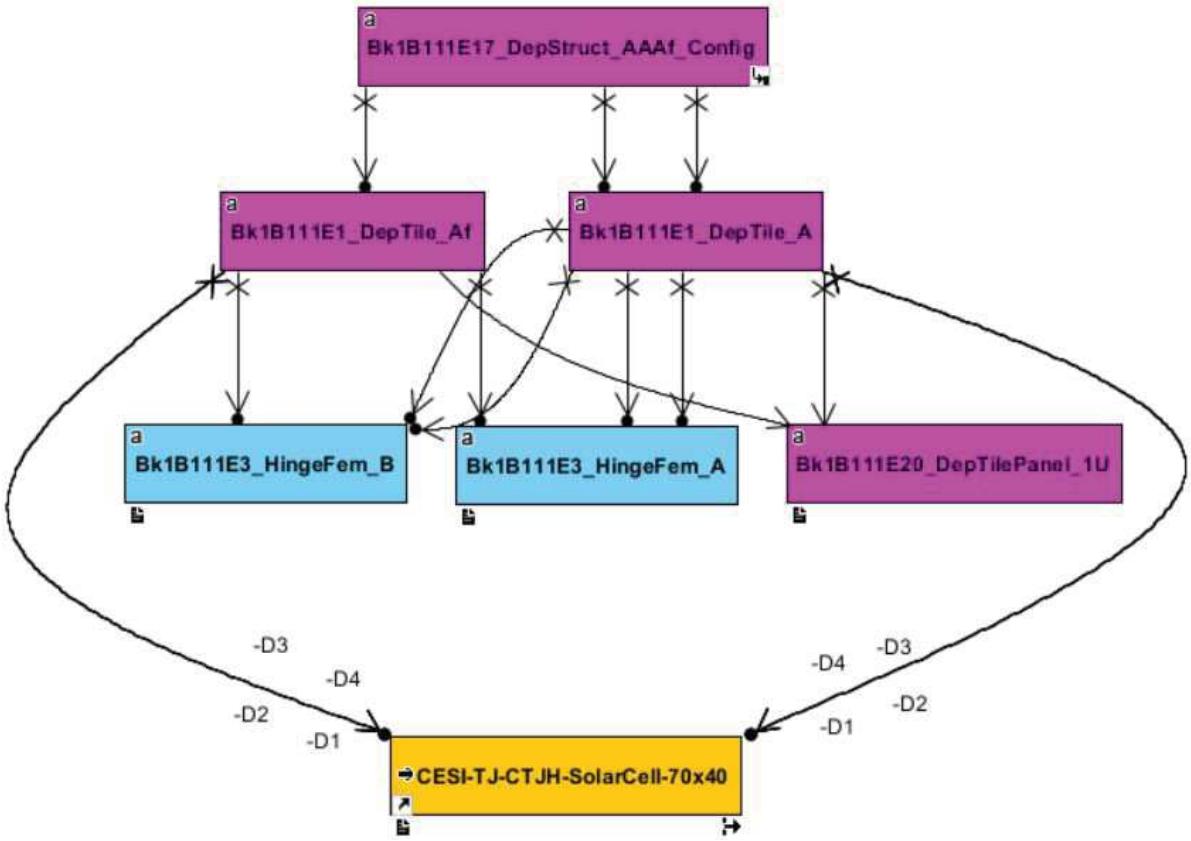


Figure 2.3. Simplify diagram of Bk1B111E17_DepStruct_AAAf_Config

Two different hinges, called Bk1B111E7_HingeFemDock_INTA and Bk1B111E8_HingeFemDock_INTB, connect mechanically the ARAMIS CubeSat Tile to a Bk1B111E20_DepTilePanel_1U. These two hinges are shown in the figure 2.4 and 2.5.

Figure 2.4. Bk1B111E7_HingeFemDock_INTA

Figure 2.5. Bk1B111E8_HingeFemDock_INTB

When the solar panels' structure is deployed, thanks to mechanical springs, the hinges rotate 180 degrees and stop in the correct position due to their particular shape. All the hinges considered are fixed to the tiles by screws.

The configuration used for this thesis is Bk1B111E17_DepStruct_AAAf_Config, thus all the considerations are related to it.

The UML class in figure 2.1 shows the the different configurations.
The Bk1B111E17_DepStruct_AAAf_Config will be analyzed in detail, considering the tiles used in this configuration separately. In figure 2.6 the Bk1B111E1_DepTile_A and Bk1B111E1_DepTile_Af are shown.

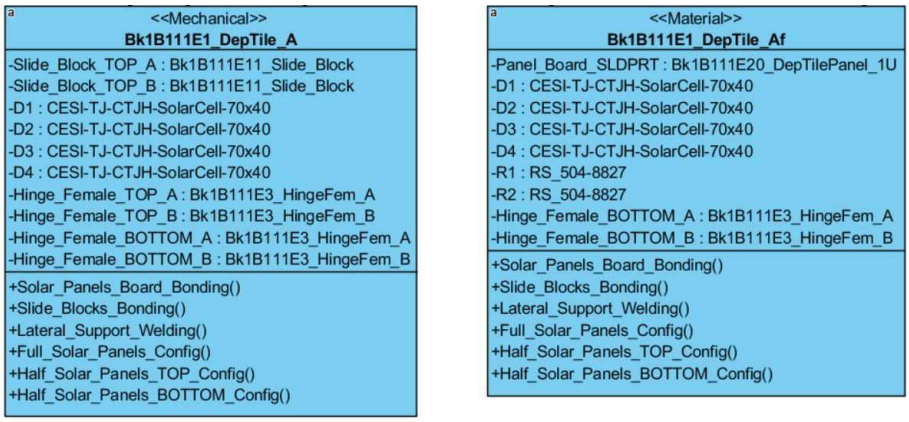


Figure 2.6. Tiles A and Af

First of all the Bk1B111E1_DepTile_A is considered. This type of tiles is used twice in the deployable solar panels' structure. The second one in opposite direction. Hinges and slides block do not change. Four CESI-TJ-CTJH-SolarCell-70x40 solar cell are used, they do not change in the other configurations (these are better analyzed in paragraph 2.2). Two slides block are used, for each A tile, to avoid touching between tiles. In this way the probability of damaging of components and solar cells, is reduced. The slides block are shown in figure 2.7.

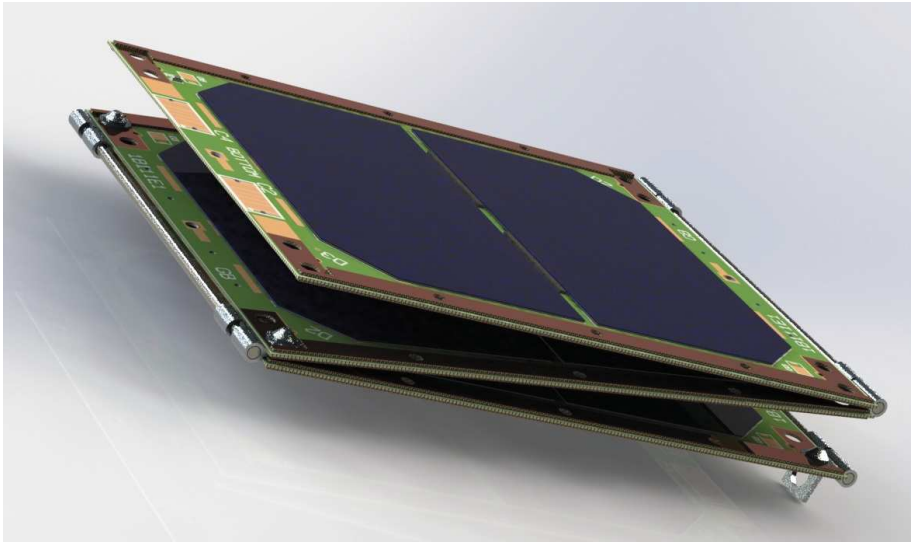


Figure 2.7. Slides Block

There are two slides block for each tile A, the Af tile does not need it. The height of these is 2.30 mm which is enough to keep the tiles apart and avoid damage. The Bk1B111E11_Slide_Block are positioned in the outer holes on the top part of tiles. Slide_Block_TOP_A and Slide_Block_TOP_B are the names used to distinguish them, one mounted on the right and one on the left.
Figure 2.8 shows a slide block and its dimensions.

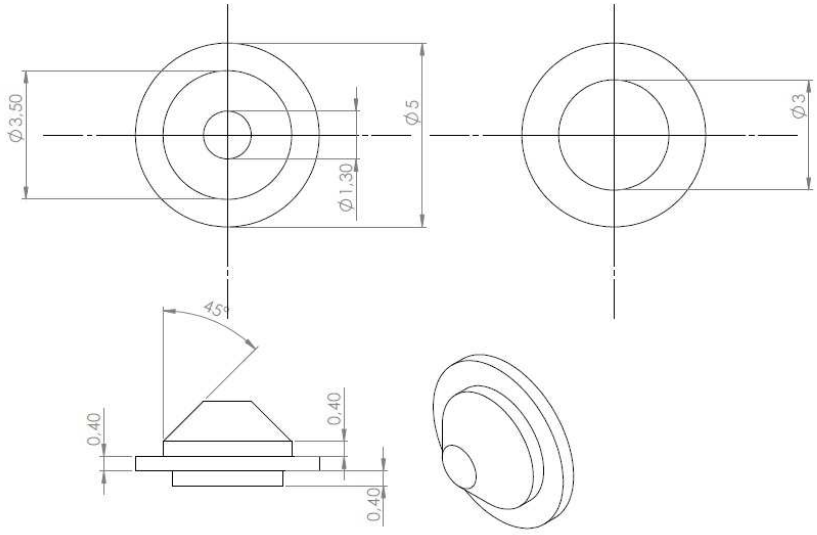


Figure 2.8. Technical features of a Slide Block

Four hinges in Bk1B111E1_DepTile_A have been used to allow the deployment of structure. These hinges are of two types: Bk1B111E3_HingeFem_A and Bk1B111E3_HingeFem_B. A pair is mounted in top part and the other in bottom one as a function of the name. When the wire is detached, the movement due to the springs forces the hinges to make a 180 degree movement, like in the case of Bk1B111E7_HingeFemDock_INTA and Bk1B111E8_HingeFemDock_INTB, and therefore the structure is deployed. The figures 2.9 and 2.10 show the two type of hinges used in AAAf configuration of deployable solar panels' structure.

Second of all the Bk1B111E1_DepTile_Af is considered. It is not very different from Bk1B111E1_DepTile_A, like the number and the type of solar cells, but there are some changes. In this case, only two hinges are needed, mounted in the top part, to hold the Af tile to the A. Internal holes in the bottom part are not used.
Bk1B111E20_DepTilePanel_1U is the mechanical structure of standard tiles used to assemble each type of Deployable_Tile_Configurations. It is composed by: a Bk1B111E1_PCB_Board_98x82, that represents both the PCB and mechanical

structure of the tiles and mechanical reinforcement of the structure composed by four Bk1B111E10_BoardLatSuppBar.

Figure 2.9. Bk1B111E3_HingeFem_A

Figure 2.10. Bk1B111E3_HingeFem_B

The latest components used in Bk1B111E1_DepTile_Af, are two 0 Ω resistances to close the circuit formed by the solar cells of the entire deployable solar panels' structure. In this way the system is ready to be connected to a side tile of a 1U ARAMIS CubeSat.

2.2 Solar cells

The solar cells chosen for the tiles in all configuration of deployable solar panels' structure, are CESI-TJ-CTJH-SolarCell-70x40, four for each tile and therefore two for each side. Their efficiency is 26% and they can generate approximately 2.2V, so their series provides an output voltage of about 4.4V. A bypass diode is connected in parallel to each cell to be sure that the single cell works correctly although one of two CESI-TJ-CTJH-SolarCell-70x40 is damaged or obscured by the shadow cast

due to the relative movement of the CubeSat. The diode chosen is UPR10E3. Performance, in terms of output voltage and power, of each single cell is degraded with the increase of the temperature. The figure 2.11 describes Power-Voltage characteristic of a single solar cell, two different temperatures, 25°C and 45°C, have been considered.

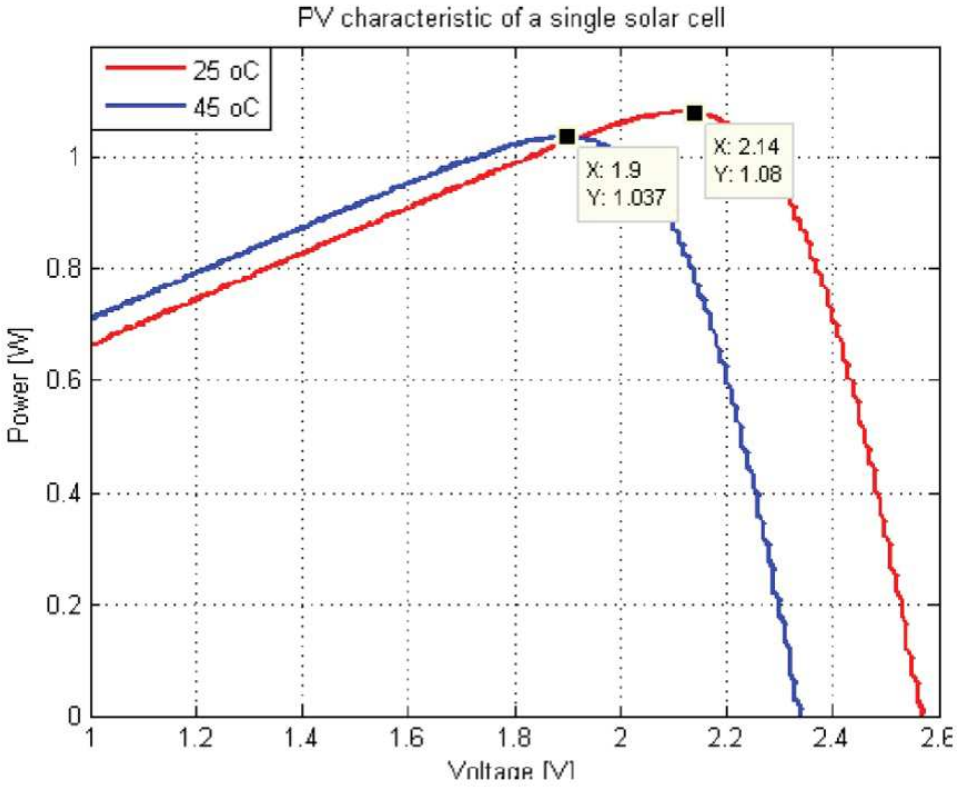


Figure 2.11. P-V characteristic of a single solar cell

It is clear that the maximum power is reached by the line that describes the behaviour of a single solar cell at 25°C. Therefore the temperature influences system efficiency.

A series configuration is used to connect two cells in the same tile. Every tile is connected to another one, except for the final tile, in this case a 0 Ω resistor is used to close the circuit. Each side of the deployable solar panels' structure 1B111E is composed by a power channel in order to transfer power into the CubeSat. Thus, the deployable solar panels' structure has two power channel. As is shown in figure 2.12.

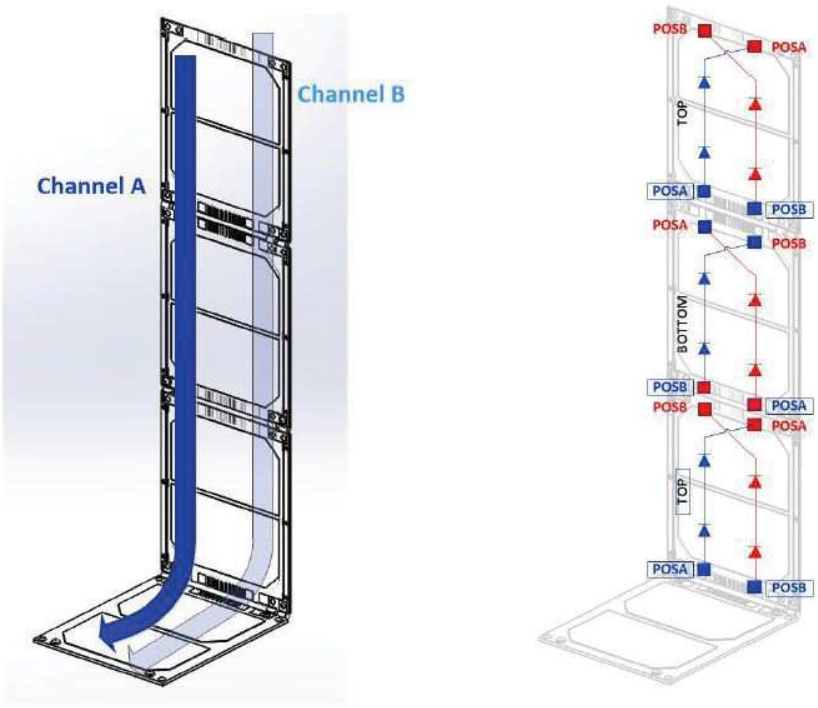


Figure 2.12. 1B111E Power channels

The standard tiles are designed to be extremely symmetric. This symmetry has an impact not only on mechanical shape but in particular on the PBC layouts. How it is clear from the figure 2.13, connectors should be used to connect the bottom of a tile to the top of following one. Since these tiles are completely identical, from the point of view of the PCB layout, means that the electrical layouts have to be coincident in order to establish electrical continuity of the serial circuits of the two channels.

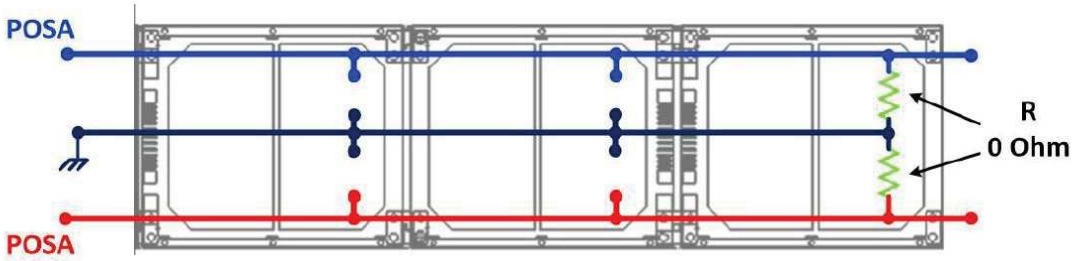


Figure 2.13. 1B111E Power channels with final 0Ωresistor

The figure 2.14 shows the circuit of a generic tile composed by four CESI-TJ-CTJH-SolarCell-70x40.

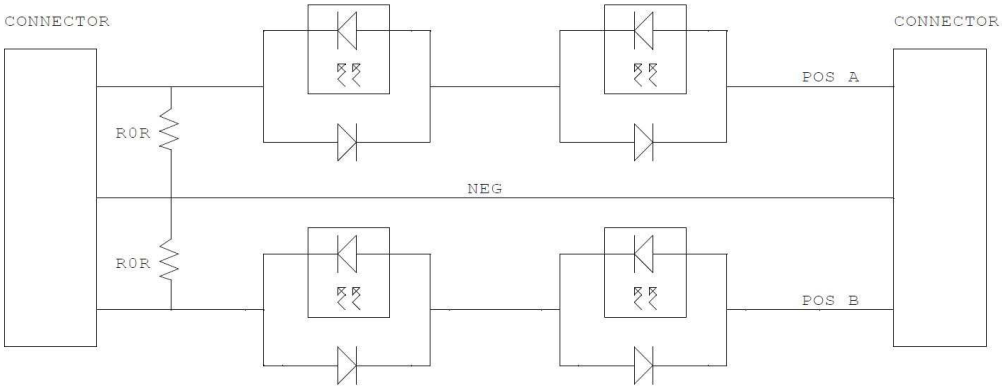


Figure 2.14. 1B111E1_Solar_Panel_Module

It is important to remember that the thickness of the connectors should respect the compatibility with P-POD module, therefore they have to occupy small space. When the 1B111E deployable solar panels' structure is folded, the space between tiles is narrow, so components of the upper tile can make contact with those of the bottom one. In order to avoid this situation, the components are placed to be interlocked with a small space tolerance once the tiles are folded.

The 1B111E deployable solar panels' structure is a power source of solar arrays in double channel. The structure is completely modular from the electronic point of view. Once deployed the structure two different situations of solar lighting are possible, as shown in the figure 2.15.

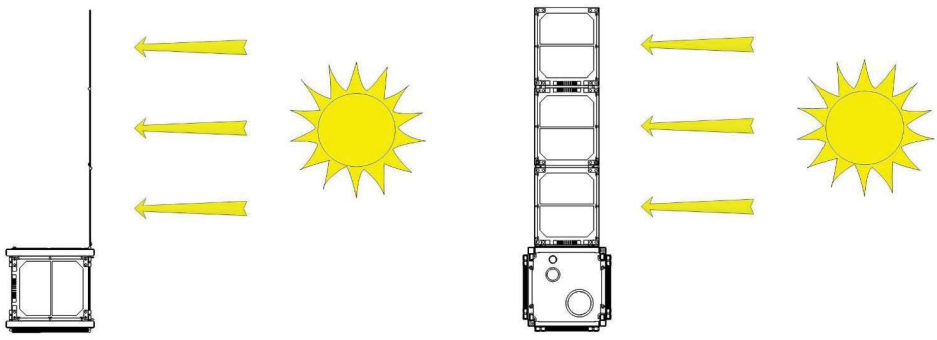


Figure 2.15. 1B111E structure sun exposures: Full side and Partial side exposure

The first condition analyzed is the full side exposure, in this case only one side of the deployable solar panels' structure is exposed to the sun, while the other side is in shadow. The double channel is used to handle this situation, although the side in shadow makes the system inefficient, because solar panels are open circuits and the drop voltages of bypass diodes are source of lost, there is the possibility to switch and activate only the illuminated side channel. The second condition, described in the figure 2.15, is relative to the situation where each side is partially exposed to sun. In this case it is possible to choose both power channel in order to increase the performance of the 1B111E solar panels' structure.

Chapter 3

Thermal Fuser

The goal of this thesis is to develop and test a deploying mechanism for 1B111E solar panels' structure. It is important to consider that all the consideration are related to this specific deployable structure, although the concept used in this work can be adapted also in other cases, like different configuration of the CubeSat satellite such as 2U and 3U. No different consideration should be made if the configuration of deployable structure is Bk1B111E18_DepStruct_AwAAf_Config or Bk1B111E19_DepStruct_BBBf_Config, but is still take into consideration the Bk1B111E17_DepStruct_AAAf_Config.

The first consideration to be made is how the deployable solar panels' structure is folded, then it is possible to find a solution to deploy the 1B111E structure. The technique is to used a wire that goes through the PCBs in order to keep them together. Thus, the proposed solution is to dissolve the tin where the wire has been soldered in order to permit the deployment of entire structure thanks to the mechanical springs.

In figure 2.2 it is possible to note that there are eight unused holes, for each single tile. Six of these are in the two lateral supports and the other two are positioned on the top and on bottom side. The eight holes have been used to pass the wire through the three PCBs. Although eight may seem like a big number, to have eight fixing wires are necessary to stabilize the entire 1B111E structure. When the CubeSat is allocated into the P-POD module, in the launch phase, the vibrations can damage the deployable structure, therefore it is important to use eight wires to keep the deployable structure stable and not subject to vibrations.

This chapter describes in detail the technique to detach the 1B111E deployable structure and which components are used to do that. The thermal fuser concept can be introduced. The idea is really simple: a current passes through a resistance in order to produce the heat needed to weld the tin where the wire is soldered.

Obviously eight thermal fusers are necessary because the tiles of deployable solar panels' structure have eight holes and therefore eight wires to detach.

The detachment system has to satisfy strict requirements like: the tensile strength of the wires should be enough to withstand the high acceleration on the launch phase. The detachment system must to guarantee to do not detach any components from the satellite transforming themselves into dangerous space debris. It is a very important issue because if some component is damaged, for some reason, it can create some short circuit and fail the space mission. Other requirements should satisfy the electrical and thermal specifications: the thermal fusers should not have high power consumption during its activity, and they should not reach too high temperatures. The space occupation and weight follow also strict requirements.

3.1 Sealing wire

The sealing wire is the main element that keeps the 1B111E structure folded. Eight wires are soldered in the test board, where the thermal fusers are placed and in the last tiles of the deployable solar panels' structure (Af tile in the case considered). As is possible see it in the figure 3.1. The choosing of the wire material and its diameter is not trivial. It is important to consider that the wire diameter influences the thermal properties of the thermal fusers and the tensile strength of the wire material affect the total seal force. The best compromise between the material and diameter of the wire should be found in order to avoid problems.

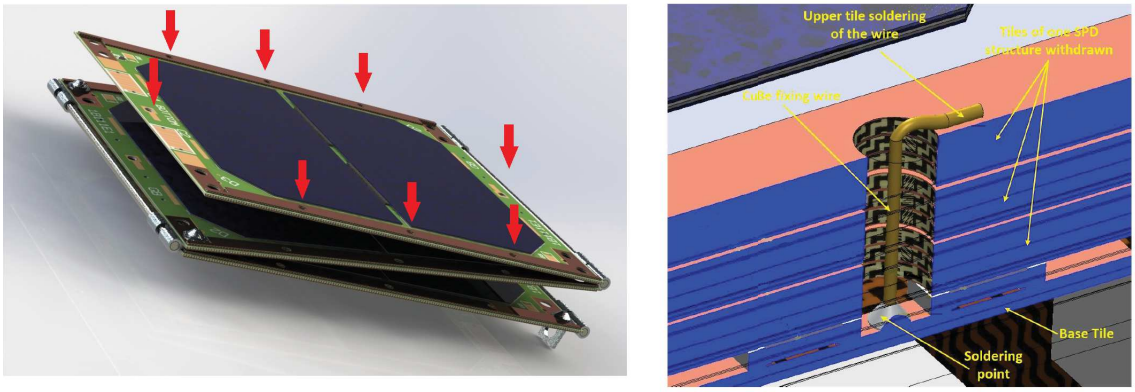


Figure 3.1. Sealing wire in 1B111E structure folded

The wires keep the tiles firm, during the launch, when the structure is subjected to vibrations. The material of the wires and their dimensions should be carefully analyzed to withstand the launch acceleration which can be very large. All the steps

that led to the choice of wire type are reported below.
The resistance of a wire depends on the tensile strength of the material used and the surface where force is applied.

$$F_{st} = T_{st} \cdot S \tag{3.1}$$

Where T_{st} is the tensile strength of the material and S is the area of circular cross section of the wire. In the worst case the maximum acceleration is 20g, so this condition has been used. The total weight of the deployable solar panels' structure has been estimated around 100g. Then, if the satellite is considered as a fix body (with a mass much larger respect to the 1B111E structure) under 20g of acceleration, the structure of tiles can be subjected to an estimated force of about:

$$F = m \cdot a = m \cdot 20g = m \cdot 20 \cdot 9.81\frac{m}{s^2} = 0.1kg \cdot 20 \cdot 9.81\frac{m}{s^2} = 20N \tag{3.2}$$

Although this is a big approximation, it is convenient to choose sealing wires that can withstand much greater force. Considering that, the table 3.1 shows the analysis of different types of materials with different tensile strength.

	Cu	**CuBe**	**Nylon 6**	**Nylon 6/6**
Diameter (d) [m]	3.00E-04	3.00E-04	3.00E-04	3.00E-04
Section/Surface (s) [m^2]	7.07E-08	7.07E-08	7.07E-08	7.07E-08
Tensile Strength [Pa]	7.00E+07	1.30E+09	7.80E+07	8.50E+07
Strength (F) [N]	4.95E+00	9.19E+01	5.51E+00	6,01E+00

Table 3.1. Wire material comparison

The diameter has been chosen of 0.3 mm. The table 3.1 shows how a single CuBe wire is already sufficient to withstand more than 20 N required. The CuBe is therefore a good choice, but the 1B111E deployable solar panels' structure has been designed to be secured with eight wires for a total traction resistance of around 735 N. The use of eight anchorage points is not only to increase the resistance to the acceleration force, but also to increase safety margins, if one or more wires are broken during launch phase. They also distribute the stress over multiple points, avoiding to fall on a single welding point.

3.2 Thermal analysis

The thermal fuser has been considered like an electronic element capable of producing energy and concentrating it in a small area. The point that needs heat is the

pad where the wire, used to keep the 1B111E structure closed, is soldered in the base tile. At first approximation, a structure that concentrates heat in a small area can be characterized by two near resistors, where the soldered point of the wire is between them. In this analysis the series of two resistances has been used to produce heat. The model to consider is shown in the figure 3.2.

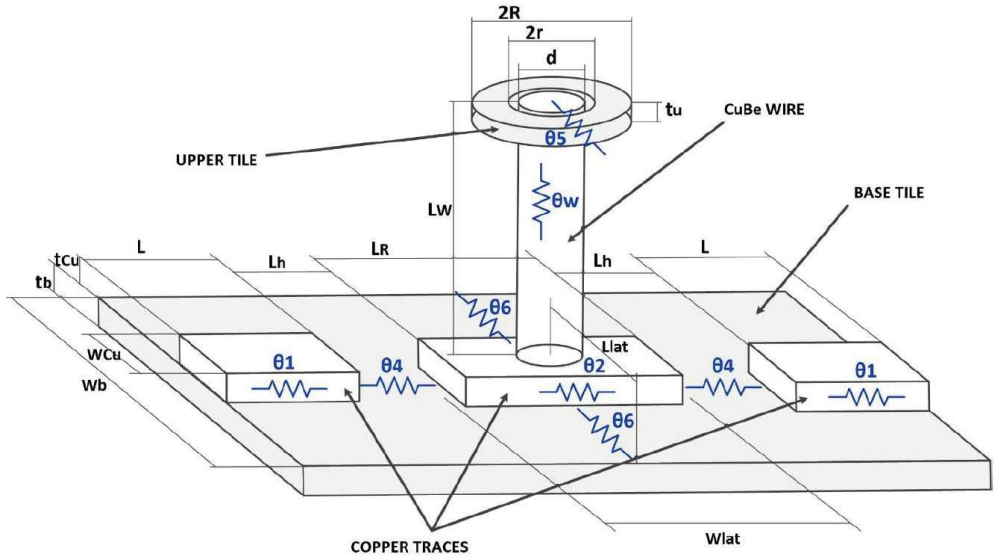


Figure 3.2. Thermal model structure of a series fusers

The main goal is to find the best compromise between shape, size and energy consumption of the thermal fuser. The thermal model for simplicity is reduced to a section of the base where fuser has been mounted. The fuser pattern can be physically confined, making it easier to analyze. Since the CuBe wire is a good heat conductor, it should be considered in the model and also the top tile panel, where the other end of the wire is soldered.

The equivalent circuit of the model in figure 3.2 is shown in figure 3.3.

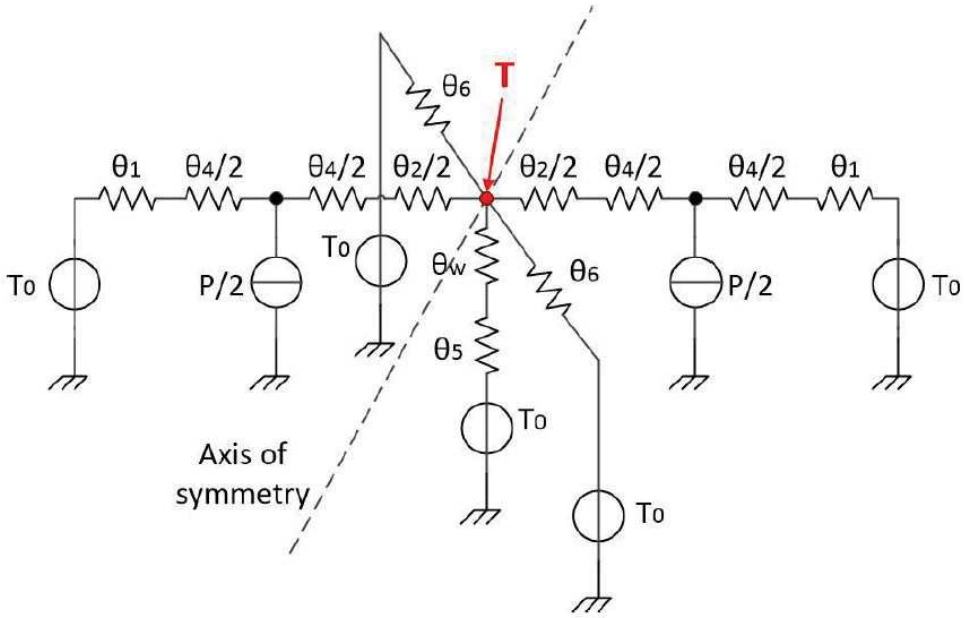


Figure 3.3. Equivalent circuit of thermal fuser model

Where the parameters are:

- T_0 is the environment temperature, considered in a worst case of -25řC.
- P represents the total power of two resistors.
- θ_1 and θ_2 are the thermal resistance of the external copper traces and the central trace respectively.
- θ_4 is the thermal resistance between two traces.
- θ_6 is the thermal resistance of the two lateral gap of FR4.
- θ_w is the thermal resistance of the CuBe wire.
- θ_5 is the thermal resistance of the upper tile.
- T is the temperature of welding point, it is also considered the temperature of entire volume of the soldering tin. This T is the parameter to be found.

Considering the symmetry of circuit in figure 3.3 and making the equivalent of Norton and Thevenin, it is possible to describe the circuit by the equation 3.3

$$T = \frac{\frac{\left(\frac{T_0}{\frac{\theta_1}{2}+\frac{\theta_4}{4}}+P\right)\cdot\left(\frac{\theta_1}{2}+\frac{\theta_4}{4}\right)}{\frac{\theta_1}{2}+\frac{\theta_4}{4}+\frac{\theta_2}{4}+\frac{\theta_4}{4}} + \frac{T_0}{\theta_3} + \frac{T_0}{\frac{\theta_6}{2}}}{\frac{1}{\frac{\theta_1}{2}+\frac{\theta_4}{4}+\frac{\theta_2}{4}+\frac{\theta_4}{4}} + \frac{1}{\theta_3} + \frac{1}{\frac{\theta_6}{2}}} \tag{3.3}$$

$$T = T_0 + P \cdot \left(\frac{\frac{\theta_1}{2} + \frac{\theta_4}{4}}{\frac{\theta_1}{2} + \frac{\theta_4}{2} + \frac{\theta_2}{4}} \cdot \frac{\left(\frac{\theta_1}{2} + \frac{\theta_4}{2} + \frac{\theta_2}{4}\right) \cdot \theta_3 \cdot \frac{\theta_6}{2}}{\theta_3 \cdot \frac{\theta_6}{2} + \left(\frac{\theta_4}{4} + \frac{\theta_1}{2} + \frac{\theta_4}{2} + \frac{\theta_2}{4}\right) \cdot \frac{\theta_6}{2} + \left(\frac{\theta_1}{2} + \frac{\theta_4}{2} + \frac{\theta_2}{4}\right) \cdot \theta_3} \right) \tag{3.4}$$

$$T = T_0 + P \cdot \theta_{tot} \tag{3.5}$$

The goal of the design of a thermal fuser is to reach the desired temperature with the lowest possible energy consumption. So, looking the equation 3.5, assuming that the final temperature is defined as T, if P decreases and T0 is a constant, θ_{tot} must increases. This is obvious because a higher thermal resistance means more heat insulation: the heat is much more limited to the welding point, allowing to reach the detachment of the wire with lees energy consumption.

The concept is simple, but the design of a low thermal resistance structure is much more difficult. A good compromise is reached with the parameters describe in table 3.2. σ is the conductivity of materials.

L_w	5.00E-03 [m]
L	3.00E-03 [m]
L_R	3.00E-03 [m]
L_{lat}	2.00E-03 [m]
W_{cu}	1.00E-03 [m]
W_b	4.00E-03 [m]
W_{lat}	3.30E-03 [m]
R	1.50E-03 [m]
r	5.00E-04 [m]
R/r	3
d	3.00E-04 [m]
σ_{Cu}	4.00E+02 $[W \cdot m^{-1} \cdot K^{-1}]$
σ_{FR4}	5.00E-01 $[W \cdot m^{-1} \cdot K^{-1}]$
σ_{CuBe}	1.01E+00 $[W \cdot m^{-1} \cdot K^{-1}]$
t_{Cu}	3.50E-05 [m]
t_u	1.60E-03 [m]
t_b	4.00E-04 [m]

Table 3.2. Parameters used for thermal fuser

To complete the calculation of θ_{tot}, it is possible to define all the thermal resistances individually. Their values have been obtained, referring to the model of figure 3.2.

$$\theta_1 = \frac{L}{\sigma_{FR4} \cdot (W_b \cdot t_b) + \sigma_{Cu} \cdot (W_{Cu} \cdot t_{Cu})} = 174 \ \left[\frac{K}{W}\right] \tag{3.6}$$

$$\theta_2 = \frac{L_R}{\sigma_{FR4} \cdot (W_b \cdot t_b) + \sigma_{Cu} \cdot (W_{Cu} \cdot t_{Cu})} = 174 \ \left[\frac{K}{W}\right] \tag{3.7}$$

$$\theta_4 = \frac{L_h}{\sigma_{FR4} \cdot (W_b \cdot t_b)} = 969 \ \left[\frac{K}{W}\right] \tag{3.8}$$

$$\theta_w = \frac{L_w}{\sigma_{CuBe} \cdot (\pi \cdot \frac{d^2}{4})} = 70000 \ \left[\frac{K}{W}\right] \tag{3.9}$$

$$\theta_5 = \frac{ln\left(\frac{R}{r}\right)}{\sigma_{FR4} \cdot t_u} = 5490 \ \left[\frac{K}{W}\right] \tag{3.10}$$

$$\theta_3 = \theta_w + \theta_5 = 75490 \ \left[\frac{K}{W}\right] \tag{3.11}$$

$$\theta_6 = \frac{L_{lat}}{\sigma_{FR4} \cdot (W_{lat} \cdot t_b)} = 758 \ \left[\frac{K}{W}\right] \tag{3.12}$$

Replacing all the values it is possible to find the total thermal resistance:

$$\theta_{tot} = 125 \ \left[\frac{K}{W}\right] \tag{3.13}$$

Once the thermal model has been defined, it is possible to choose the type of tin for the soldering wire. The correct operation of the thermal fuser is based on the use of a low temperature melting tin. If this type of tin is not used and a standard tin is selected, the melting temperature of about 220 °C is likely to melt the resistance welding, causing disastrous detachment of the components that fail the mission. Thus, the material chosen for the wires has a melting temperature of about T = 120 °C. Once the temperature has been reached, given $T_0 = -25$°C in the worst case, it is possible to obtain a minimum power of P = 1,16W to be dissipated in order to reach the melting temperature of $T = 120$°C. Taking into account a minimum tolerance to achieve melting temperature, it is possible to use a total power of $P = 1.5$ W, this consideration has been done because T_0 is considered the worst case of low temperature in LEO (Low Earth Orbit) but on reality this value can be inferior. Using this power, the temperature expected is T = 163 °C.

3.2.1 Thermal simulation

The model in Figure 3.2 has been completely translated into a SolidWorks simulation model. Flow Tool Analysis has been used to perform the analysis. The real properties of the materials have been used and all dimensions and shapes of the objects used have been defined (Table 3.2). The welding tin has been inserted into the simulation. This choice is functional as the tin used to ensure physical contact between the board and the wire. Since the tin has a low thermal resistance, the model does not deviate from the analytical one. All shapes and boundary conditions have been defined and heat sources have been positioned.

- The materials are considered with real proprieties.
- The type of analysis is "external", by selecting only the solid heat conduction. This means that the outer space is considered empty (vacuum condition), so only conduction is considered in the solid.
- Entire body is considered a blackbody wall.
- A real wall is applied on lateral surfaces of the upper and bottom board of the model. Temperature applied to real wall is -25C°.
- The external source is only radiation from deep space of 3K.
- The two heat sources are applied to the two volumes of the resistors. The value of generation is 0,75 W for each resistor. In this way the total amount of power generated is 1,5 W.
- The initial temperature of the bodies is 293K.

The figure 3.4 shows the complete thermal model of a fuser.

The figure 3.5 shows the temperature in function of time that the soldering tin reaches. The temperature is about 159 °C (432,15 K) at equilibrium. This value is quite near to the analytic value of 161 °C (434,15 K) and so the simulation model can be validated. The slight difference between the analytical and simulated temperature is probably due to the low precision of the first model. In fact, the analytical model does not consider vertical conduction in the test board. And so the temperature is slightly higher. The figure 3.6 shows the heating steps. The figure 3.7 shows the same steps but with a cross section along the horizontal axis. This figure illustrates how the vertical spread of heat on the board is not negligible as is the case of the analytical model.

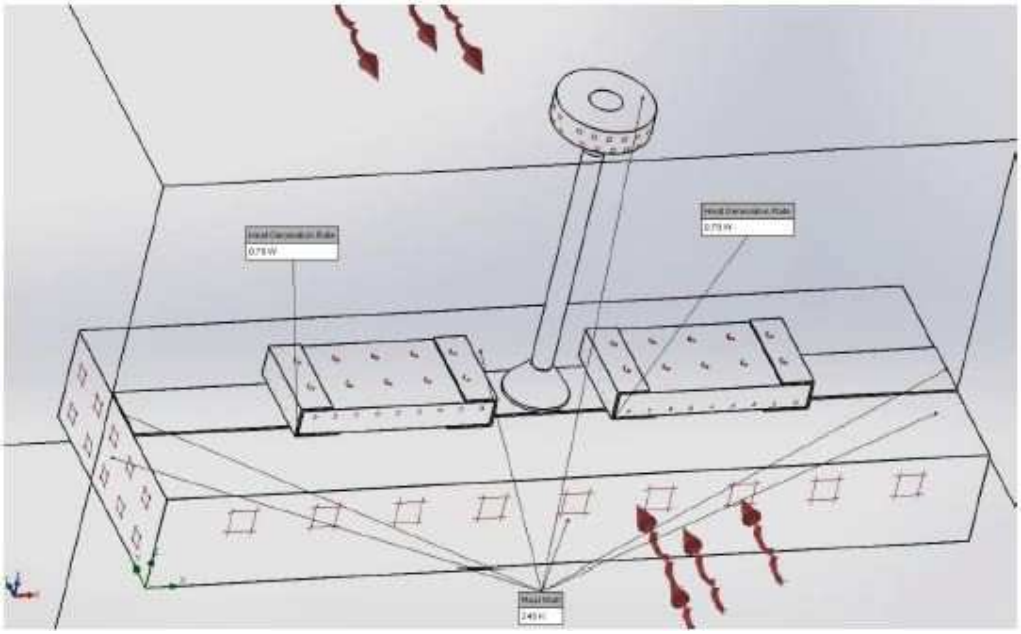


Figure 3.4. Simulation thermal model structure of a fuser

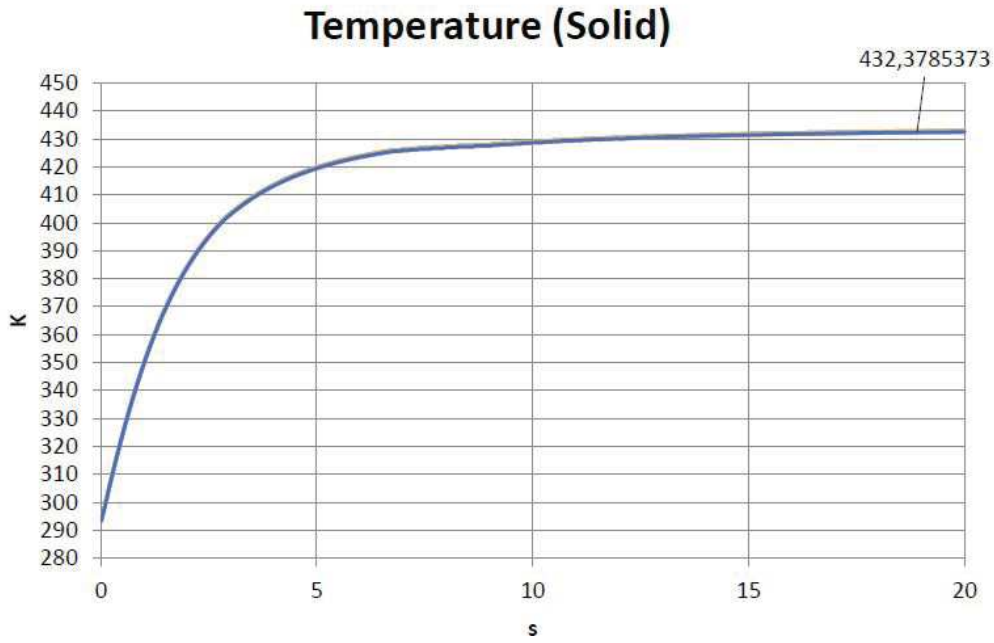


Figure 3.5. Thermal profile of the tin soldering

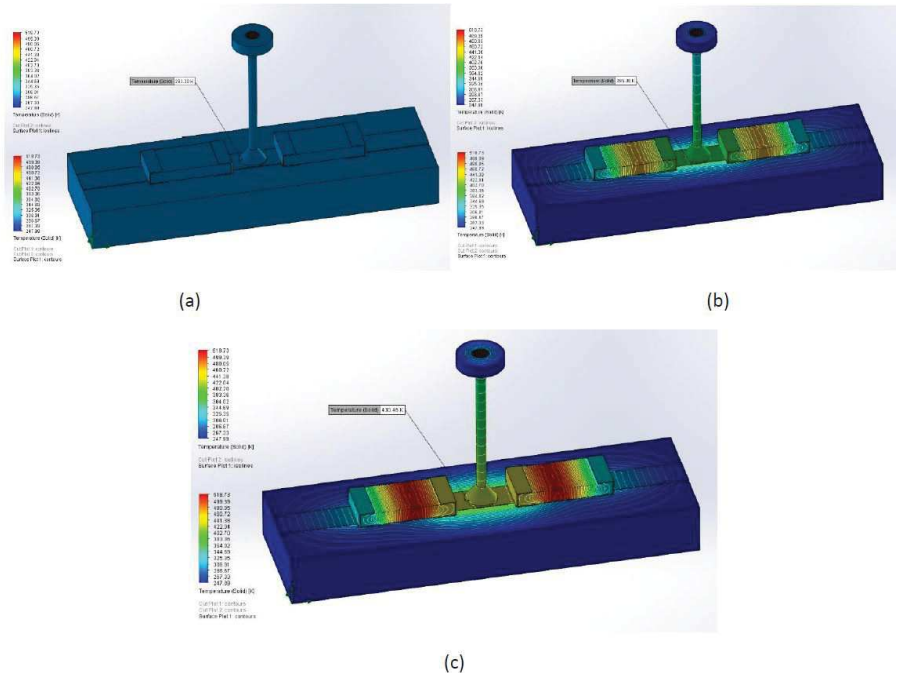


Figure 3.6. Heating phase of a thermal fuser: (a) initial condition, (b) 2 sec, (3) 10 sec

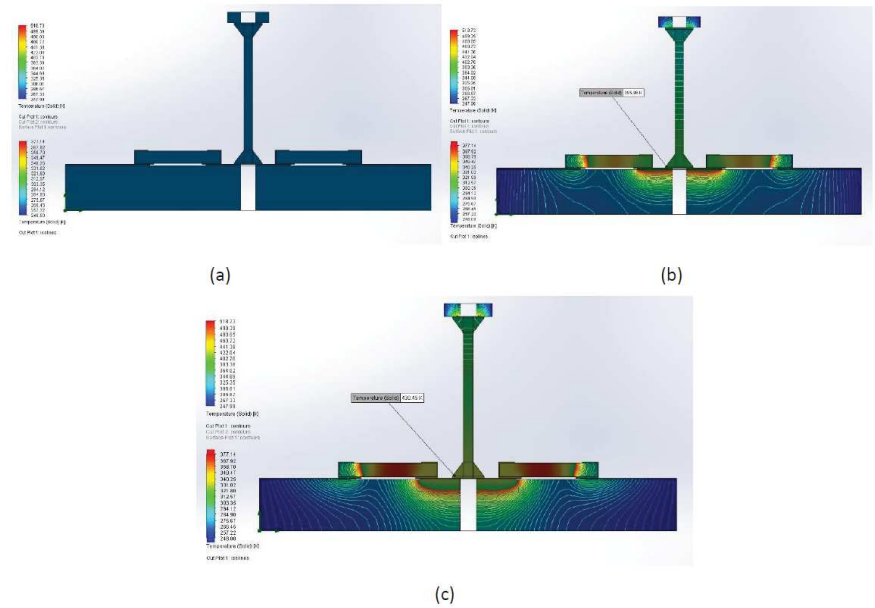


Figure 3.7. Heating phase of a thermal fuser cross section: (a) i.c., (b) 2 sec, (3) 10 sec

3.3 Electrical design

The thermal fuser technique consists to pass a current through a resistance. The deploying mechanism is based on the conversion of electric energy in heat energy by Joule effect. The power needed to deploy the 1B111E solar panels' structure depends on which material the wires are composed of. In this particular case, CuBe is the material considered. The power necessary to melt the tin where the wires are soldered is 1.5W. The circuit is designed considering the high voltage bus of 14V, according to ARAMIS specifications.
The circuit to consider is shown in figure 3.8:

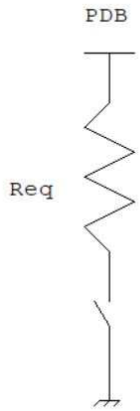


Figure 3.8. Thermal Fuser concept

The minimum current can be found keeping in mind the 14V PDB and the power required.

$$Power = V \cdot I_{min} \tag{3.14}$$

$$I_{min} = \frac{Power}{V} = \frac{Power}{PDB} = \frac{1.5}{14}\frac{W}{V} = 107mA \tag{3.15}$$

The minimum current required to detach the fixing wires is used to find the value of R_{eq} resistance.

$$Power = R_{eq} \cdot I_{min}^2 \tag{3.16}$$

$$R_{eq} = \frac{Power}{I_{min}^2} = \frac{1.5}{107}\frac{W}{mA} = 131\Omega \tag{3.17}$$

R_{eq} is the resistance needed to detach the wire that holds the 1B111E structure. Although it is possible to use only one resistance, it is better to use two, in this way the wire can be positioned between them. Two circuits can be developed according to the resistances configuration: series and parallel. As it is shown in figure 3.9.

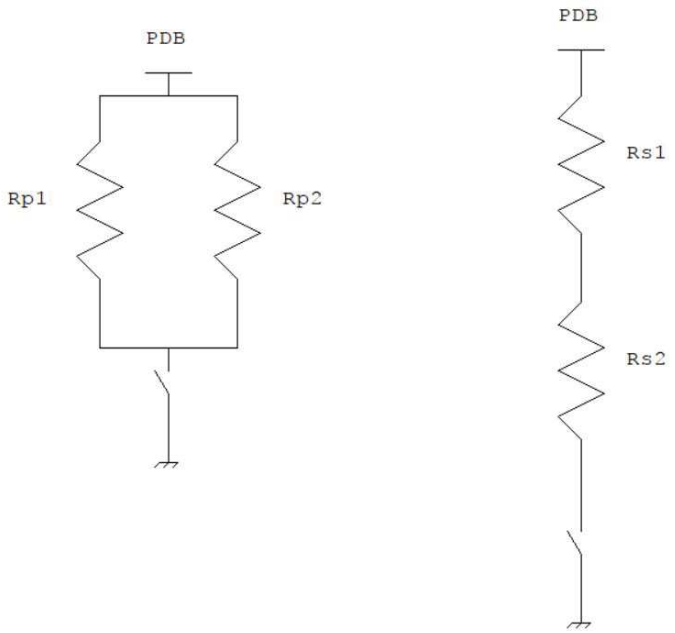


Figure 3.9. Thermal Fuser configurations: Parallel and Serial

Obviously the value of resistances changes if one configuration is chosen instead of the other. It is important to consider that the equation changes according to the configuration used. The resistors should have the same value to produce the same heat and have a symmetrical circuit, therefore $R_{s1} = R_{s2}$ and $R_{p1} = R_{p2}$.
First of all this calculation has been made for the series configuration.

$$R_{eq} = R_{s1} + R_{s2} = 2 \cdot R_{s1} \tag{3.18}$$

$$R_{s1} = \frac{R_{eq}}{2} = \frac{131}{2} = 65.5\Omega \tag{3.19}$$

Second of all it has been made for the parallel configuration.

$$R_{eq} = \frac{R_{p1} \cdot R_{p2}}{R_{p1} + R_{p2}} = \frac{R_{p1}^2}{2 \cdot R_{p1}} = \frac{R_{p1}}{2} \tag{3.20}$$

$$R_{p1} = 2 \cdot R_{eq} = 2 \cdot 131 = 262\Omega \tag{3.21}$$

In theory the values found in 3.19 and 3.21 should be enough to dissolve the tin of the fixing wire. The solar panels' structure can be deployed thanks to these two resistances. The wire is positioned between the resistors and it receives heat from both. Each resistance dissipates half power in order to be a symmetric circuit. The two resistors have been chosen in order to be small components and have a maximum power dissipation of 0.75 W.

Besides the fact their resistance values are different they also have different reliability to failure. In series configuration, if one or both of the resistors are detached from the welding because of the temperature or vibrations in the launch phase, it does not pass any current and therefore no more heat is produced by Joule effect. In the parallel configuration, however, if a resistance is damaged or disconnected and the other one is connected, it is always a source of heat that could be able to detach the wire and allow the deployment of the solar panels' structure.

As shown in figure 3.9, two configurations are possible: parallel and series, depending on how the resistances are positioned. The eight thermal fusers should be mounted on the board that represents the face of CubeSat satellite. This means that occupying small space is very important, therefore the positioning of components is a strict requirement, but it is necessary to consider that the holes where fixing wires go through the PCBs are in specific place. This means that the resistances should be positioned in such a way to have the wire between them. In this way thanks to the heat produced by resistances the tin can be dissolved in the soldering point. A single current of 107mA has been used to produce the heat needed.

3.3.1 Drive circuit

The command that allows the current to pass through the resistances should be sent when the satellite is pushed out from the P-POD module, so it is necessary to use a microcontroller. However, this can not control directly the thermal fusers with a 107mA current, so a drive circuit has to be designed.

The best choice is using a couple of transistors MOS as switches to increase the reliability to failure. If one MOSFET is damaged, the other one protects the board avoiding that PDB goes in short circuit, causing a catastrophic failure that can compromise the mission. The drive circuit of a thermal fuser is shown in figure 3.10.

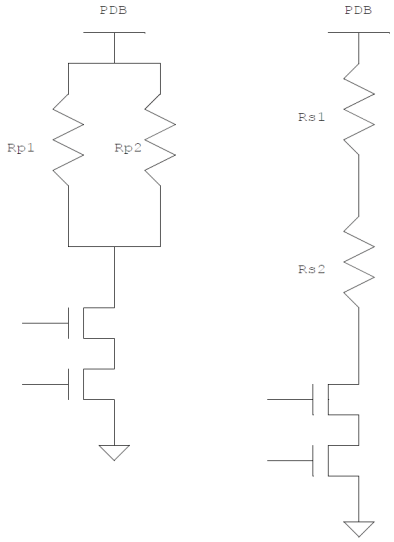


Figure 3.10. Drive circuit of thermal fuser: Parallel and Serial

Furthermore, in order to reduce as much as possible space occupation of the MOSFET, it has been chosen to use a double channel MOS integrated inside the same package. Obviously, the type of transistors are chosen taking into account a tolerance for the maximum current (1A) and a lowest possible ON resistance (few $m\Omega$ in this case).
The principle of operation is simple: the two transistors are positioned to drive the circuit. Once the voltage, applied to the gate of transistors, exceeds the threshold voltage of the MOS, they enter into conduction and because they exhibit low drain-source ON resistance, the ground potential is as if applied directly to the load. In this way the voltage drop on the MOS is negligible and the entire 14V voltage is applied directly to the load. If one of the two MOSs is damaged, the one still running is disabled and therefore it disconnects the direct path between supply and ground.

3.3.2 Feedback system

The space environment often has difficult conditions to predict with utmost precision. All thermal analysis analyzed and simulations provide an estimate of what happens when the thermal fuser are powered. The calculations have been made

considering the worst case with the temperature of T_0 = -25 °C. Unfortunately it may vary. If T_0 increases and P is constant, the final temperature T increases. It can produce catastrophic failures because it is possible to obtain the melting temperature of the soldering tin of the resistances (the melting temperature is about 220 °C). This situation can cause detachment of the resistors producing debris and causing a series of short circuits. The maximum temperature should be checked in order to avoid this situation. It is done using a temperature sensor, therefore the melting system has a feedback control, as it is described in figure 3.11.

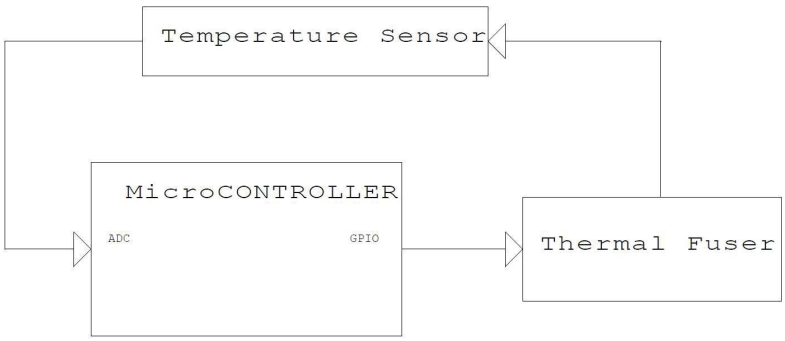


Figure 3.11. Feedback control

A microcontroller manages the control signal to activate the fuser and also the feedback control of the temperature. The microcontroller processes the value of the temperature coming from the sensor and then it can turn off the thermal fuser if temperature exceeds a certain threshold. The sensor used is a simple NTC, operating in the range of -40 °C to 150 °C. This particular type of temperature sensor is simply a resistance that changes its features through a negative temperature coefficient. The component has been chosen for its small size, in order to position it close to the thermal fuser. This sensor has a 0603 package and it should be mounted very close to the wire, but not too much to not interfere with the thermal properties of the fuser.
The NTC sensor varies its electrical resistance parameter according to the temperature variations. The NTC class is a category of thermistor that reduces its resistance when the temperature increases. Unfortunately, the non-linear behaviour of this type of sensor is a big problem, as it is shown on top figure 3.12. To avoid the non-linear condition, a linearization circuit has been designed. Although there are several types of linearization circuits, since there is no particular need to the precision of the measurement of the temperature, the simpler linearization circuit has been used. This consists of a simple voltage divider and the NTC sensor should be inserted in parallel to one of the two resistors. As it is shown in figure 3.13.

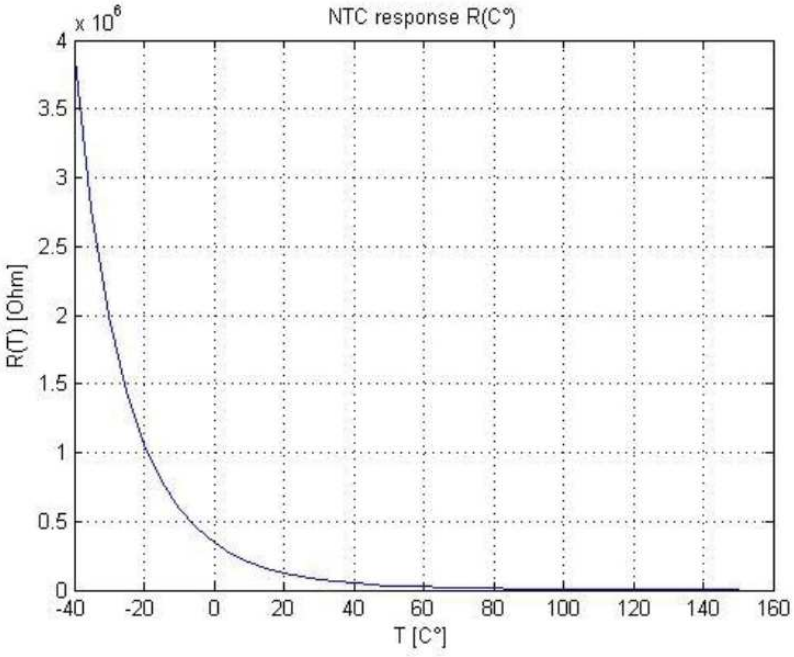


Figure 3.12. $R(T)$ response of NTC

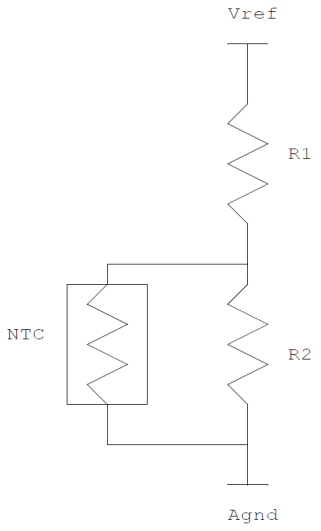


Figure 3.13. Linearization circuit of NTC

A NTC sensor of $100k\Omega$ has been used with two resistors $R2 = 56k\Omega$ and

$R3 = 22k\Omega$ for the linearization circuit. V_{temp} is the output voltage of the voltage divider and is given by the equation 3.22.

$$V_{temp} = V_{ref} \cdot \frac{R_2 // R_{NTC}}{R_1 + R_2 // R_{NTC}} = V_{ref} \cdot \frac{R_2 \cdot R_{NTC}}{R_1 \cdot R_2 + (R_1 + R_2) \cdot R_{NTC}} \tag{3.22}$$

Where V_{ref} is 3V. The output voltage V_{temp} represents the linearized response of the sensor output. By combining the linearization relationship 3.22 with the $R_{NTC}(T)$ curve from the NTC technical data sheet 3.12, $V_{temp}(T)$ has been obtained. An appropriate MatLab script has been used to trace the response of the NTC component and the output of the linearization circuit. The 3.14 shows the two responses of the curve is rather linear from 20°C to about 140°C. In this condition, the circuit linearization range is good because the maximum temperature that should be measure is about 140°C - 150°C. The figure 3.14 shows also the energy consumption of the NTC linearization circuit.

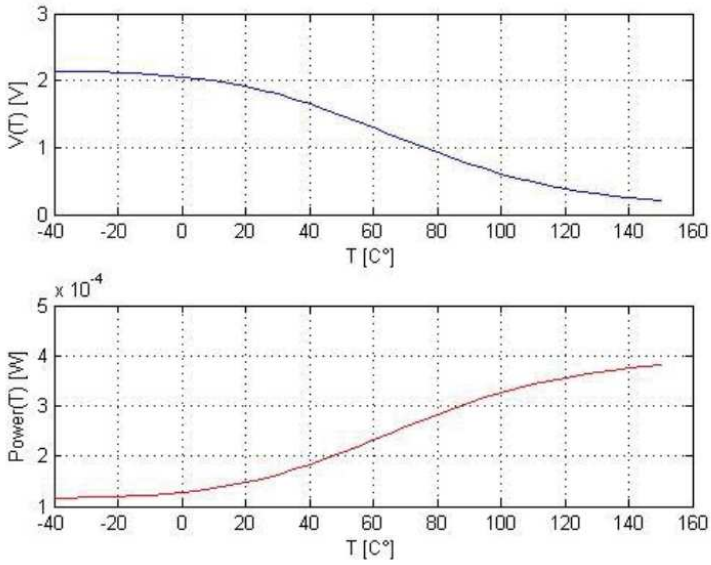


Figure 3.14. Output response V(T) and P(T) of the linearizated circuit

3.3.3 Thermal Fuser system

The deploying mechanism is based on the thermal fusers. They need different components to work properly as the drive circuit and the sensor of temperature. The figure 3.15 reports the general circuit of the thermal fuser.

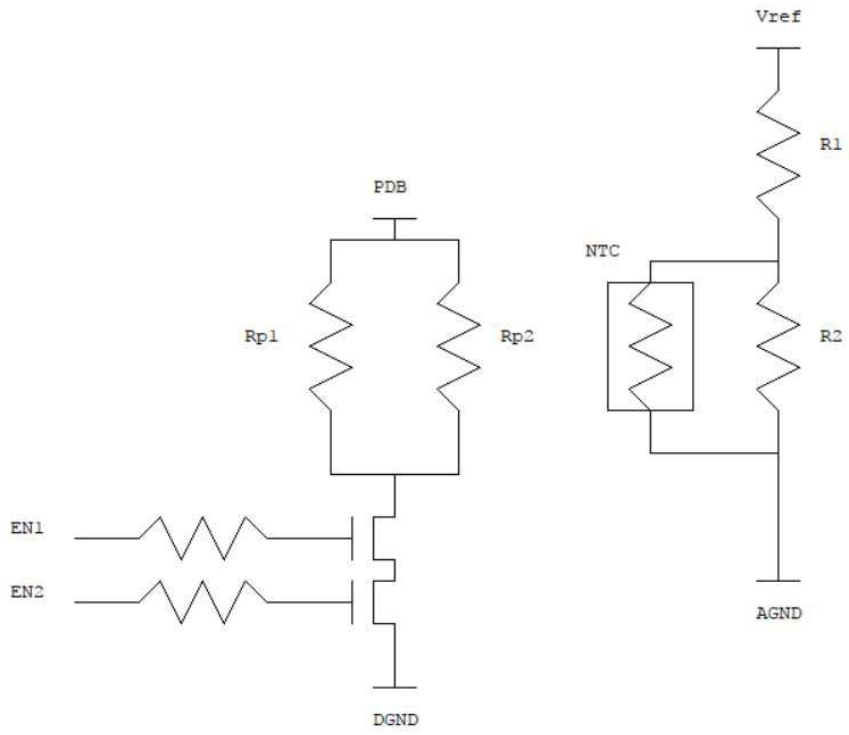


Figure 3.15. General Thermal Fuser system

In the figure 3.15 the configuration of the resistances used to produce heat is the parallel one. The wire is not represented, but should be positioned between R_{p1} and R_{p2}. EN1 and EN2 are the enable signal. They enable and disable the transistors in order to active the thermal fuser composed by the two resistances, R_{p1} and R_{p2}. The heat causes a variation of the resistance value of the NTC and thanks to the linearization circuit the temperature variation can be acquired. If the thermal fuser produce too much heat, the enable signal EN2 should be used to provide the disabling of the thermal fuser.

3.4 Components choice

The choice of components is very important to be sure of the correct operation of the circuit and therefore of the entire system. The occupation of small space is the generic specification followed to take these choices. The resistors, that form the thermal fusers, should be positioned very close to the pad of the soldered wire to concentrate the heat in that specific area. Even if the NTC needs to be positioned close to the resistors, it does not have to interfere with the deployment mechanism, therefore a 0603 package is a good choice. The idea to occupy small space can also be applied to the drive circuit of the thermal fusers, formed by the 2CH-MOS.

3.4.1 Thermal fuser components

The value of the two resistors that form the thermal fuser are chosen depending on which configuration has been used, parallel or series. Although the resistances are different in both cases, a 0603 package for both of them has been chosen. The real values of the resistances are different respect to those calculated in analytic way, because these have been adapted to the standards. The real values of the resistances and which component has been chosen are reported in the table 3.3.

	R_{ideal} [Ω]	R_{real} [Ω]	Component
Parallel	262	240	RC0603JR-07240RL
Series	65.5	68	RC0603FR-0768RL

Table 3.3. Components used in Parallel and Series configuration

Yageo is the manufacturer of the resistances and as it is possible to understand from the code they have the same package (0603). The resistor is constructed on top of a high-grade ceramic body. Internal metal electrodes are added on each end to make the contacts to the thick film resistive element. The composition of the resistive element is a noble metal embedded into a glass and covered by a second glass to prevent environmental influences. The resistor is laser trimmed to the rated resistance value. The resistor is covered with a protective epoxy coat, finally the two external terminations (matte tin on Ni-barrier) are added, as shown in figure 3.16.

The dimensions are listed in figure 3.17 and the main characteristics in 3.18.

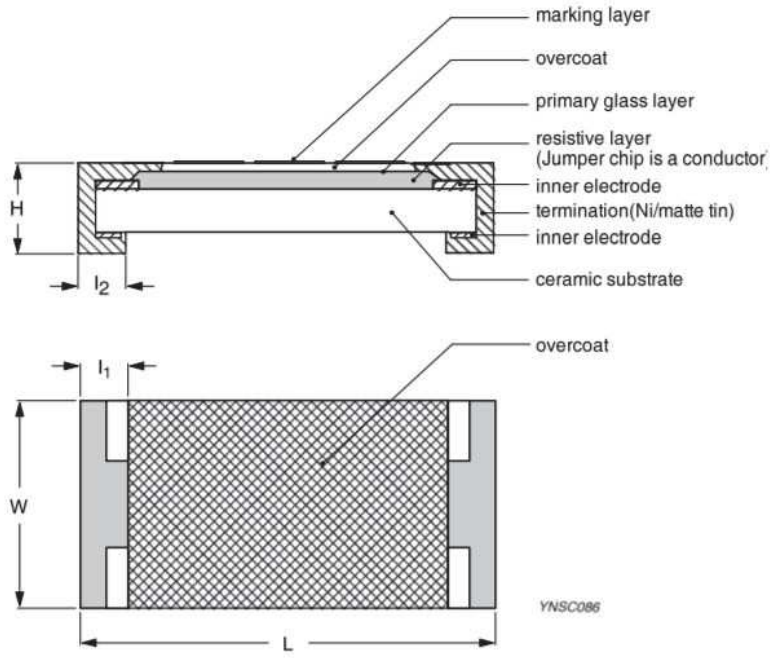


Figure 3.16. Chip resistor outlines

DIMENSION

Table I

TYPE	L (mm)	W (mm)	H (mm)	l_1 (mm)	l_2 (mm)
RC0075	0.30±0.01	0.15±0.01	0.10±0.01	0.08±0.03	0.08±0.03
RC0100	0.40±0.02	0.20±0.02	0.13±0.02	0.10±0.03	0.10±0.03
RC0201	0.60±0.03	0.30±0.03	0.23±0.03	0.10±0.05	0.15±0.05
RC0402	1.00±0.05	0.50±0.05	0.35±0.05	0.20±0.10	0.25±0.10
RC0603	1.60±0.10	0.80±0.10	0.45±0.10	0.25±0.15	0.25±0.15
RC0805	2.00±0.10	1.25±0.10	0.50±0.10	0.35±0.20	0.35±0.20
RC1206	3.10±0.10	1.60±0.10	0.55±0.10	0.45±0.20	0.40±0.20
RC1210	3.10±0.10	2.60±0.15	0.55±0.10	0.45±0.15	0.50±0.20
RC1218	3.10±0.10	4.60±0.10	0.55±0.10	0.45±0.20	0.40±0.20
RC2010	5.00±0.10	2.50±0.15	0.55±0.10	0.45±0.15	0.50±0.20
RC2512	6.35±0.10	3.10±0.15	0.55±0.10	0.60±0.20	0.50±0.20

Figure 3.17. Chip resistor dimensions

The laws of heat conduction, convection and radiation determine the temperature rise in a resistor due to power dissipation. The maximum body temperature usually occurs in the middle of the resistor and is called the hot-spot temperature. In the

CHARAC-TERISTICS	POWER	OPERATING TEMPERATURE RANGE	MAXIMUM WORKING VOLTAGE	MAXIMUM OVERLOAD VOLTAGE	DIELECTRIC WITHSTANDING VOLTAGE	RESISTANCE RANGE	TEMPERATURE COEFFICIENT	JUMPER CRITERIA
RC0603	1/10 W	-55℃ to 155℃	75V	150V	150V	5% (E24) 1Ω≦R≦22MΩ 1% (E24/E96) 1Ω≦R≦10MΩ 0.1%, 0.5% (E24/E96) 10Ω≦R≦1MΩ Jumper<50mΩ	1Ω≦R≦10Ω ±200ppm℃ 10Ω<R≦10MΩ ±100ppm℃ 10MΩ<R≦22MΩ ±200ppm℃	Rated Current 1.0A Maximum Current 2.0A
	1/5 W	-55℃ to 155℃	75V	150V	150V	5% (E24) 1Ω≦R≦1MΩ 1% (E24/E96) 1Ω≦R≦1MΩ	1Ω≦R≦1MΩ ±200ppm℃	

Figure 3.18. Chip resistor characteristics

normal operating temperature range of chip resistors the temperature rises at the hot-spot. T, is proportional to the power dissipated: $\Delta T = A \cdot P$. The proportionally constant A gives the temperature rise per Watt of dissipated power and can be interpreted as a thermal resistance in $[K/W]$. This thermal resistance is dependent on the heat conductivity of the materials used (including the PCB), the way of mounting and the dimensions of the resistor. The sum of the temperature rise and the ambient temperature is described in the equation 3.23.

$$T_m = T_{amb} + \Delta T \tag{3.23}$$

where:

- T_m = hot-spot temperature.
- T_{amb} = ambient temperature.
- ΔT = temperature rise at hot-spot.

The stability of a chip resistor during endurance tests is mainly determined by the hot-spot temperature and the resistive materials used. When specifying the performance of a resistor, the dissipation is given as a function of the hot-spot temperature, with the ambient temperature as a parameter.

$$\Delta T = A \cdot P \tag{3.24}$$

From the equations 3.24 and 3.23 it follows that:

$$P = \frac{T_m - T_{amb}}{A} \tag{3.25}$$

If P is plotted against T_m for a constant value of A, parallel straight lines are obtained for different values of the ambient temperature. The slope of these lines, $dP/dT_m = 1/A$ is the reciprocal of the heat resistance and is the characteristic for the resistor and its environment.
The temperature coefficient of the resistance is a ratio which indicates the rate of increase (decrease) of resistance per degree (°C) increase (decrease) of temperature within a specified range, and is expressed in parts per million per °C (ppm/°C). The temperature coefficient is shown in figure 3.19.

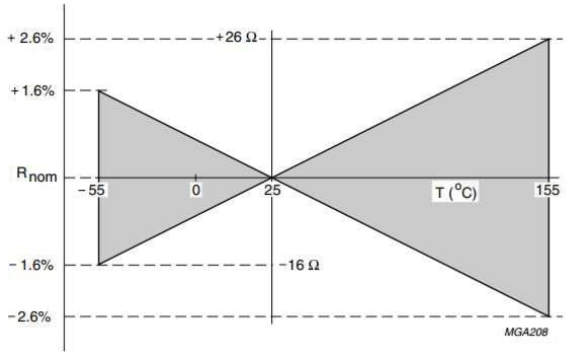


Figure 3.19. Temperature coefficient

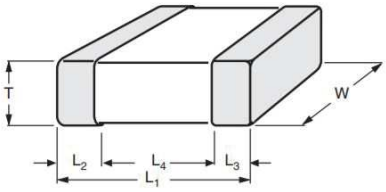
3.4.2 NTC component

The NTC is a particular type of temperature sensor, it reduces the resistance value according to increase of the temperature. The voltage resulted from the temperature variation will be read by the microcontroller, then it will decide if the temperature is too high and therefore it will disable the thermal fuser. In this way it is possible to prevent the melting of the soldering tin of the components due to the increase of temperature and therefore avoid the fail of the mission due to the detachment of components. The linearization circuit has been used in order to provide that the NTC works in the linear zone. The linearization circuit is simply based on two resistance in series configuration, where the NTC is positioned in parallel respect to one of them.
The components chosen for this purpose are shown in table 3.4 The name of resistances are related to the figure 3.13.

	Value $[k\Omega]$	**Component**
NTC	100	NTCS0603E3104FXT
R_1	22	RC0603FR-0722KL
R_2	56	RC0603FR-0756KL

Table 3.4. NTC and linearization circuit components

First of all the two resistors used for the linearization circuit (R_1 and R_2) are of the same family as those that form the thermal fuser, which is why the characteristics are not reported. Refer to the previous paragraph for information. Second of all the NTCS0603E3104FXT has been chosen in order to occupy small space. Thus a 0603 package has been chosen. It is a Vishay component where the dimensions are reported in millimeters in figure 3.20.



L_1	W	T	L_2 AND L_3 MIN.	L_4 MIN.
1.6 ± 0.15	0.8 ± 0.15	0.8 ± 0.15	0.2	0.4

Figure 3.20. NTC package

From the data sheet of the NTC, the maximum temperature of 260°C during 40s must not be exceeded to prevent the melting of the NTC welding. This limit is largely respected because the thermal fusers do not reach 220°C which could dissolve the soldering of the resistors. The change of the resistance value due to variation of temperature is shows in figure 3.21.

RESISTANCE VALUES AT INTERMEDIATE TEMPERATURES WITH R_{25} AT 33 kΩ, 47 kΩ, 68 kΩ, AND 100 kΩ								
T_{OPER} (°C)	PART NUMBER NTCS0603E3333*HT		PART NUMBER NTCS0603E3473*HT		PART NUMBER NTCS0603E3683*HT		PART NUMBER NTCS0603E3104*XT	
	R_T (Ω)	TCR (%/K)	R_T (Ω)	TCR (%/K)	R_T (Ω)	TCR (%/K)	R_T (Ω)	TCR (%/K)
- 40	1 061 183	- 6.70	1 643 693	- 6.85	2 324 376	- 6.77	3 921 252	- 7.03
- 35	764 125	- 6.44	1 174 859	- 6.59	1 667 529	- 6.52	2 774 565	- 6.77
- 30	557 158	- 6.20	850 461	- 6.34	1 211 148	- 6.28	1 988 706	- 6.52
- 25	411 058	- 5.97	623 018	- 6.11	889 917	- 6.05	1 442 861	- 6.28
- 20	306 646	- 5.75	461 557	- 5.89	661 047	- 5.84	1 058 901	- 6.06
- 15	231 157	- 5.55	345 583	- 5.69	496 103	- 5.64	785 573	- 5.85
- 10	175 977	- 5.36	261 354	- 5.49	375 941	- 5.45	588 793	- 5.65
- 5	135 223	- 5.18	199 536	- 5.31	287 504	- 5.28	445 602	- 5.47
0	104 827	- 5.01	153 714	- 5.13	221 786	- 5.11	340 346	- 5.29
5	81 946	- 4.84	119 427	- 4.97	172 502	- 4.95	262 229	- 5.12
10	64 569	- 4.69	93 541	- 4.81	135 221	- 4.79	203 723	- 4.96
15	51 262	- 4.54	73 832	- 4.66	106 786	- 4.65	159 522	- 4.80
20	40 989	- 4.40	58 703	- 4.52	84 928	- 4.51	125 851	- 4.66
25	**33 000**	**- 4.27**	**47 000**	**- 4.38**	**68 000**	**- 4.38**	**100 000**	**- 4.52**
30	26 741	- 4.14	37 881	- 4.25	54 796	- 4.26	80 003	- 4.39
35	21 804	- 4.02	30 726	- 4.13	44 427	- 4.14	64 422	- 4.26
40	17 884	- 3.91	25 073	- 4.01	36 232	- 4.02	52 200	- 4.14
45	14 751	- 3.80	20 579	- 3.89	29 714	- 3.91	42 548	- 4.02
50	12 234	- 3.69	16 984	- 3.79	24 499	- 3.81	34 879	- 3.91
55	10 198	- 3.59	14 092	- 3.68	20 304	- 3.71	28 749	- 3.80
60	8543.9	- 3.49	11 751	- 3.58	16 909	- 3.61	23 820	- 3.70
65	7191.9	- 3.40	9847.6	- 3.49	14 149	- 3.52	19 835	- 3.60
70	6081.4	- 3.31	8290.7	- 3.40	11 893	- 3.43	16 597	- 3.51
75	5164.9	- 3.22	7011.4	- 3.31	10 041	- 3.34	13 951	- 3.42
80	4405.0	- 3.14	5955.0	- 3.22	8512.2	- 3.26	11 780	- 3.33
85	3772.0	- 3.06	5078.7	- 3.14	7245.5	- 3.18	9988.4	- 3.25
90	3242.6	- 2.99	4348.7	- 3.07	6191.1	- 3.11	8504.3	- 3.17
95	2797.8	- 2.91	3737.8	- 2.99	5310.0	- 3.03	7269.4	- 3.09
100	2422.8	- 2.84	3224.6	- 2.92	4570.7	- 2.96	6237.5	- 3.02
105	2105.3	- 2.78	2791.8	- 2.85	3948.0	- 2.90	5371.7	- 2.95
110	1835.5	- 2.71	2425.3	- 2.87	3421.5	- 2.83	4642.5	- 2.88
115	1605.4	- 2.65	2113.9	- 2.72	2974.8	- 2.77	4025.9	- 2.81
120	1408.5	- 2.59	1848.4	- 2.65	2594.5	- 2.71	3502.7	- 2.75
125	1239.5	- 2.53	1621.2	- 2.59	2269.6	- 2.65	3057.1	- 2.68
130	1093.9	- 2.47	1426.1	- 2.54	1991.2	- 2.59	2676.4	- 2.62
135	968.07	- 2.42	1258.1	- 2.48	1751.9	- 2.53	2350.1	- 2.57
140	859.04	- 2.36	1112.9	- 2.42	1545.5	- 2.48	2069.5	- 2.51
145	764.28	- 2.31	987.19	- 2.37	1367.1	- 2.43	1827.4	- 2.46
150	681.69	- 2.26	877.91	- 2.32	1212.3	- 2.38	1617.9	- 2.40

Figure 3.21. Resistance variation due to temperature

3.4.3 Drivers components

The driving circuit of the thermal fusers is very important for the correct operation of the system, it prevents short circuit between the power supply and the ground. The drive circuit consists of two transistors and two resistors of a few ohms connected to the gates. It can enable the fuser when the satellite is ejected from the P-POD module and can disable it in the event of malfunction or if the temperature reached by the thermal fusers is too high. Two 0603 packages of the resistors and an integrated package for the two transistors have bee chosen to respect the specification of occupy small space. The PQFN dual 2x2 is the package chosen for the transistors. The components used to the driver circuit are describe in the table 3.5.

	Value $[\Omega]$	**Component**
$2MOS$		IRLHS6376TRPBF
R	22	RC0603FR-0722RL
R	22	RC0603FR-0722RL

Table 3.5. Driving circuit components

First of all the resistors chosen for the driving circuit (R and R) are of the same family as those that form the thermal fuser, which is why the characteristics are not reported. Refer to the paragraph 3.5.1 for information. Second of all the two channel MOS have been produced by Infineon Technologies, with a QFPN package, as it is reported in the figure 3.22 and 3.23.

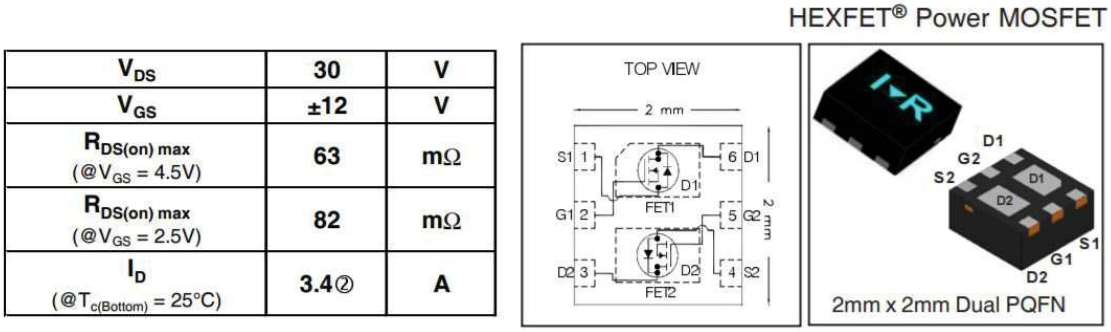
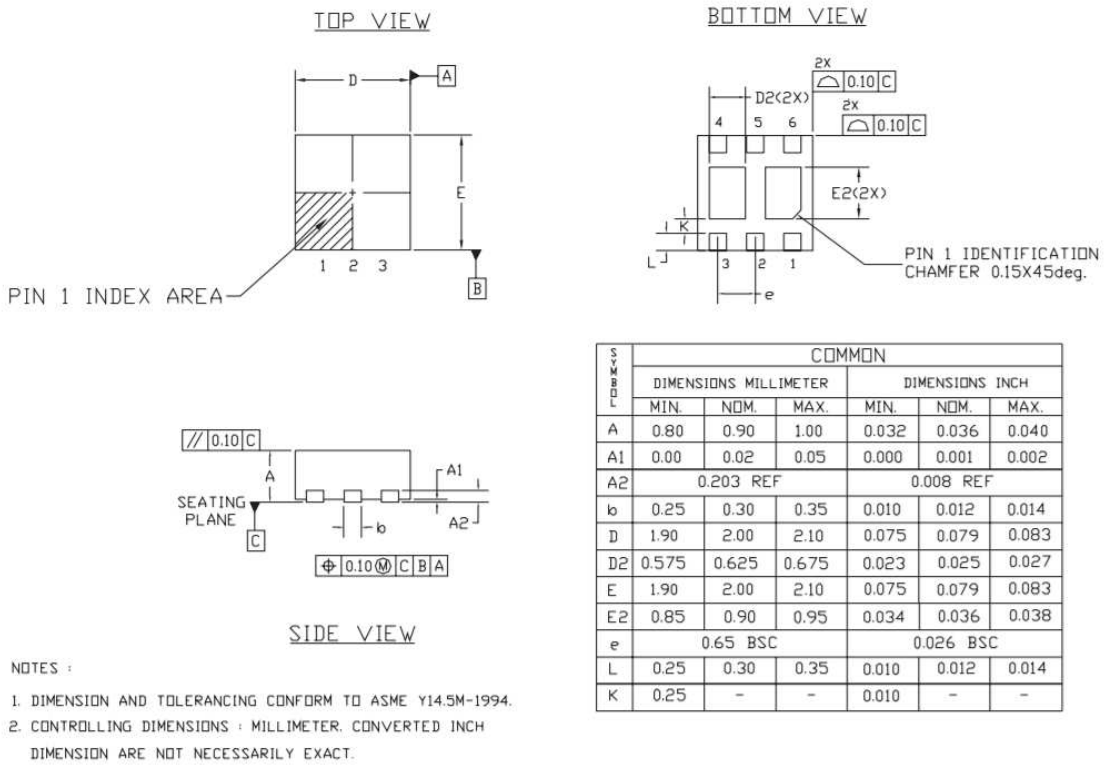


Figure 3.22. 2 channels MOSFET

The specifications of a maximum current of $1A$ and a R_{on} resistance of a few Ohms have been respected.



SYMBOL	COMMON					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.032	0.036	0.040
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.203 REF			0.008 REF		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	1.90	2.00	2.10	0.075	0.079	0.083
D2	0.575	0.625	0.675	0.023	0.025	0.027
E	1.90	2.00	2.10	0.075	0.079	0.083
E2	0.85	0.90	0.95	0.034	0.036	0.038
e	0.65 BSC			0.026 BSC		
L	0.25	0.30	0.35	0.010	0.012	0.014
K	0.25	-	-	0.010	-	-

Figure 3.23. PQFN Dual 2x2 outline package

3.5 Layout fuse series and parallel

Although the biggest difference that is possible consider for thermal fusers is between the serial and parallel configuration, there is another difference due to the placement of thermal fusers in the Bk1B6711 Test Board. The eight thermal fusers should be placed at specific points on the test board: one should be placed on the side where 1B111E structure is attached, this means that the space between connectors for the two power channels should be large enough to insert the thermal fuser, in the other seven cases there is no this restriction. The thermal fuser is conceptually composed of two resistors and an NTC, therefore if it is positioned on the side where the deployable solar panels' structure is fixed, the thermal fuser is formed only by these three components, in the other cases it is also possible to consider the 2CH-MOS and thus that space between these components can be reduced.
The layouts of these component have been made using *Altium Design*, first of all symbol has been created and then the footprint. These should respect the inputs and outputs of thermal fusers.

3.5.1 *FUSE-series* and *FUSE-MOS-series*

The symbol represents the component that will be used in the schematic. The termal fusers could be represented as a simple block with inputs and outputs, but a particular symbol has been preferred to draw in order to figure out how the components are positioned to avoid creating ambiguities.
First of all the serial configuration without 2CH-MOS has been considered, the figure 3.24 shows symbol and footprint of the thermal fuser that will be placed in the side where deployable solar panels' structure is attached.

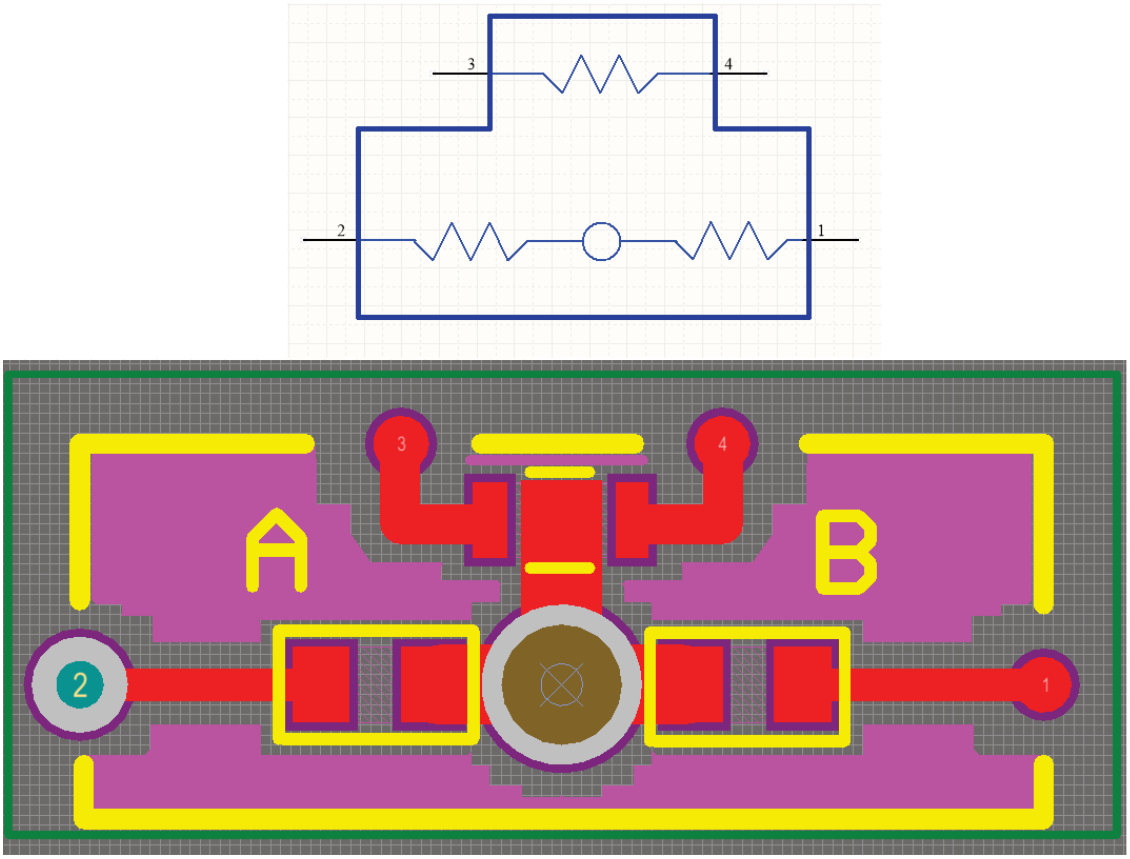


Figure 3.24. Symbol and Footprint of FUSE-series

The hole in the center represents the via where the wire, that keeps close the deployable solar panels' structure, has been soldered. This hole is also the reference origin for the positioning of components and it also represents the place where the

holes of 1B111E are aligned. The two resistances that produce heat by Joule effect are called A and B. They have been positioned at 2.325mm from the origin. A track on the top layer, of 3mm long and 1mm of width, connects the two resistances with the via where the wire has been soldered. The other two tracks from the resistances to pins are 3mm long and 0.4mm of width. These two tracks connects the thermal fuser to the power supply PDB (pad 2) and to the drain of 2CH-MOS (pad 1). The NTC has been positioned in the upper part of the footprint (see figure 3.24), it has been connected to analog ground by the pad 4. The pad 3 instead has been used to measure the temperature, for this purpose a fill of 3mm long and 1mm of width below the NTC has been positioned to better measure the temperature of via where the wire is soldered. The keepout region has been insert in order to ovoid connections next to the wire and therefore miss the measurement.
The size of the pads and vias in the thermal fuser are reported in the table 3.6.

	diameter [mm]	**Hole size** [mm]
*pad*1	0.7	0
*pad*2	1.2	0.6
*pad*3	0.7	0
*pad*4	0.7	0
wire via	2	1.5

Table 3.6. Pad dimensions

The pad 2 has different dimensions from the other ones because it should be connected to PDB. The via used to attach the wire respects the wire specification.

Second of all the serial configuration with 2CH-MOS has been considered, the figure 3.25 shows symbol and footprint of the thermal fusers that will be placed in the other seven holes. This footprint contains the 2CH-MOS in order to have a configuration where the empty space of the Bk1B6711 Test Board is reduced. This configuration allows to have more space for the positioning of other components in the PCB.
The consideration and the relative dimension of the thermal fuser are the same of the FUSE-series without 2CH-MOS, therefore these have not been inserted. The only difference is that the 2CH-MOS has been inserted in the footprint of thermal fuser and the connections have been made like in the schematic, considering obviously the data sheet of the component.

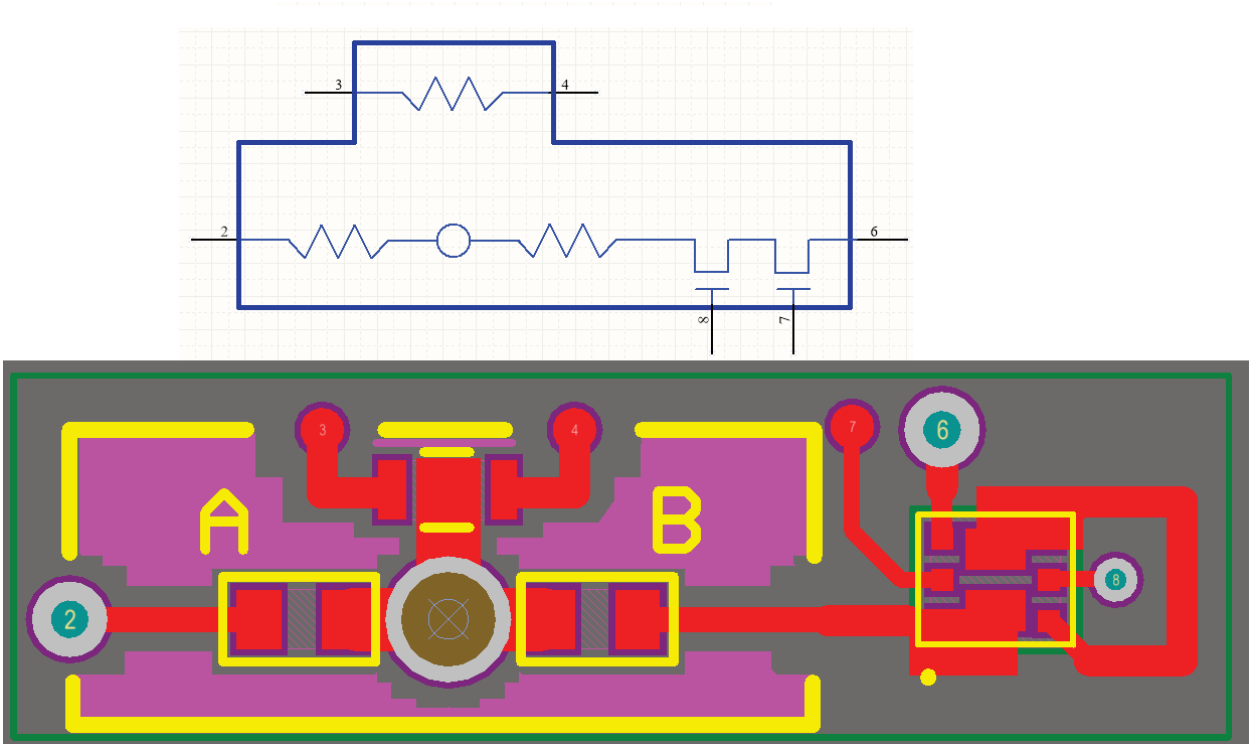


Figure 3.25. Symbol and Footprint of FUSE-MOS-series

As it can be seen in the figure 3.25, pad 1 is directly connected with the 2CH-MOS drain. The source of first MOS is connected to the drain of the second one, through a 0.5mm track. The via 6 connects the 2CH-MOS to DGND, it has dimension similar to that one used to connect the thermal fuser to PDB. Pads 7 and 8 are the gates of the two transistor and they will be connected to two resistors of 22Ω to drive the thermal fuser. For pad 8 has been chosen a via because the drain-source connection of the two MOS is around the gate of the second transistor, so it will has to switch to another layer to make the connection. Two metal zones have been inserted below the two drain pads to have no problems due to heat dissipation. This metal area in the top layer is 1.722 mm long and 1.046 mm of width.

3.5.2 *FUSE-parallel* and *FUSE-MOS-parallel*

The symbol represents the component that will be used in the schematic. It could be represented as a simple block with inputs and outputs, but it has been preferred to draw a particular symbol to figure out how the components are positioned to avoid creating ambiguities.
The two configurations are reported in the figure 3.26 and 3.27.

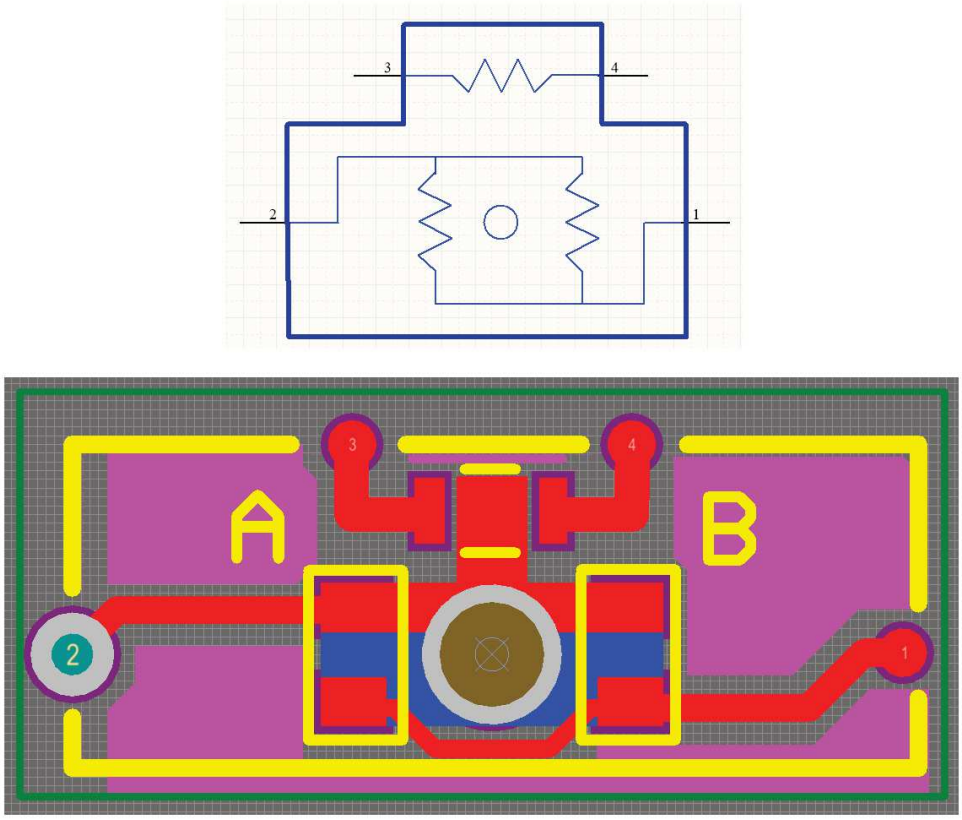


Figure 3.26. Symbol and Footprint of FUSE-parallel

The considerations made for FUSE-series and FUSE-MOS-series are the same in these two others configurations. One of the changes made has been the positioning of the resistors, in this case they are at a distance of 2 mm from the hole of the wire. A track of 4.9 mm long and 0.71 mm of width connects the resistances to the soldering of the wire. Another track connects the resistances to the 2CH-MOS and in this case the particular shape of the connection has been made to ovoid the touching of the wire. The blue region is a area of metal in the bottom layer used to heat dissipation, the dimensions are 4.9 mm long and 2.6 mm of width.
No other changes have been made between the series and parallel configuration, this means that they are interchangeable and could be used indifferently. It is important consider why these two configuration have been made. If a resistance of the thermal fuser has been damaged or desoldered, only the parallel configuration guarantees the operation of the other resistance, although it does not produce enough heat, there is the possibility that the wire will be disconnected.

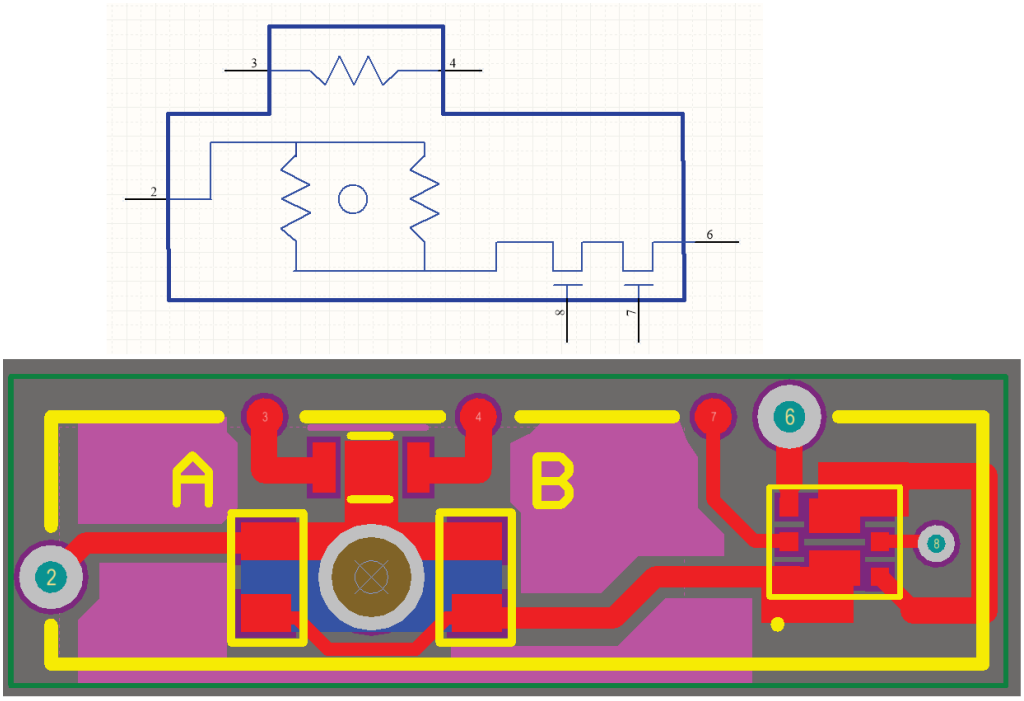


Figure 3.27. Symbol and Footprint of FUSE-MOS-parallel

3.6 UML class diagram

The UML class diagram has been used to describe the whole project, so the class diagram of the thermal fuser has been created. UML class diagram describes only the parallel configuration because it has been chosen in the Bk1B6711 Test Board. The labels are related with those used in Altium Design. The class diagram of the thermal fusers is shown in the figure 3.28.
Two classes have been generated to describe the different configuration of the thermal fusers, with and without the 2CH-MOS. *Fuser MOS* and *Fuser* are the name of thermal fuser with and without the integrated MOS respectively. RA and RB are the resistance used to produce the heat required to detach the soldered wire, these are the same in both of cases. As it is described in the previous paragraph these resistances have been used in parallel configuration, therefore the value is 240Ω. The part number of the resistances is DK_311-240GRCT-ND, it is a DigiKey component. The NTC, obviously, is also the same for both of configurations, it is a temperature sensor that controls the heat produced by thermal fusers. The part number of the component used for the NTC is RS_684-1273, it is a RS component.

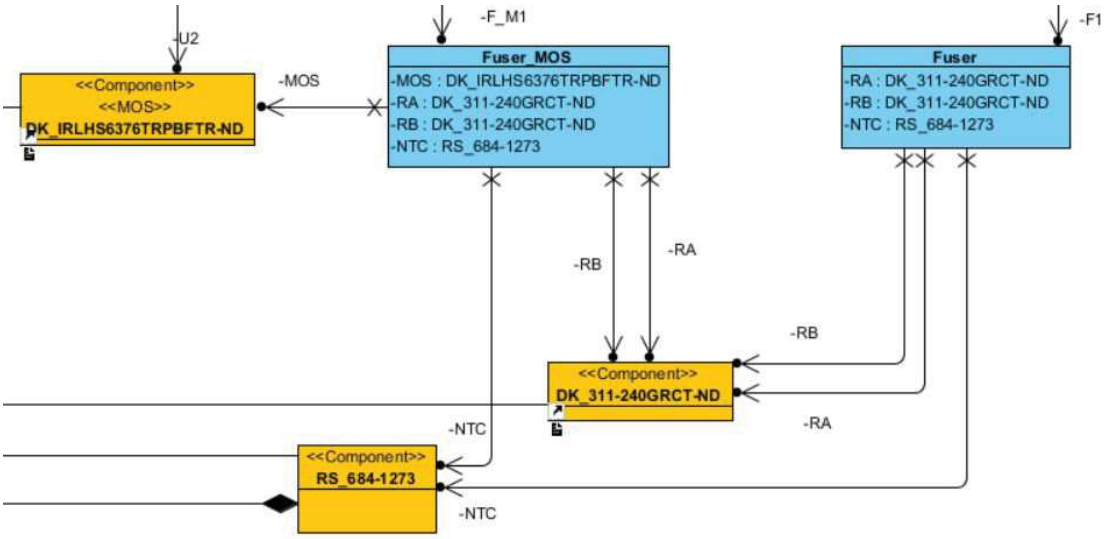


Figure 3.28. Class diagram of thermal fusers

The *Fuser* is fully described. The *Fuser MOS* has another component integrated, the 2CH-MOS used to drive the thermal fuser. The part number is DK_IRLHS6376TRPBFTR-ND and it is a DigiKey component. In the *Fuser* the 2CH-MOS has not been integrated because the space occupation in the side where the 1B111E deployable solar panels' structure is fixed, is not enough to allow the positioning of this component. For this reason the integrated MOS has been positioned on the Bk1B6711 Test Board like a single component.

Chapter 4

Bk1B6711_Test_Board

The Bk1B6711 is the test board used to deploy the 1B111E solar panels' structure. The generic system has been described in the figure 4.1.

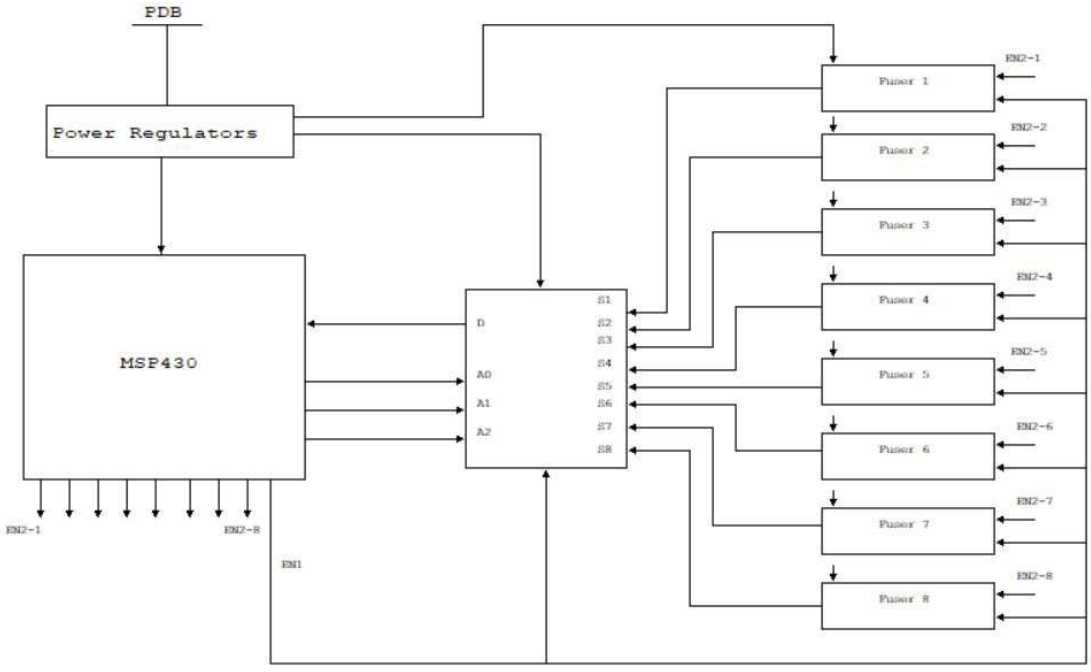


Figure 4.1. Test Board blocks diagram

PDB is the power bus where the 14V come from. It supplies a block, called power

regulator that provides the 3.3V supply for the microcontroller and 3V for the thermal fusers and for the multiplexer. The system is composed by eight thermal fusers, these have two enable signal for each ones. Since the thermal fuser should be enabled all together, the EN1 is the same signal for all of them. There are other eight enable signals, called EN2-1 to EN2-8, used to disable the thermal fuser when it generates too high heat or when the 1B111E solar panel structure has been deployed and no more heat is required. The analog output signal (V_{temp}) of the thermal fuser come from the NTC, it should be read by the microcontroller to obtain the themperature of each thermal fuser. Thanks to the multiplexer, the analog outputs of the NTC only need an ADC. The microcontroller provides three logic input signals of selection (A0, A1, A2) to the analog MUX. These inputs allow to switch from one analog input to another (S1 to S8). All enable and control signals will be connected to the microcontroller, where appropriate firmware will be implemented to handle them.

Altium Designer has been used to describe the Bk1B6711 Test Board. The figure 4.2 shows how the project is organized. Since it is complicated, multi sheets have been made to better describe the system.

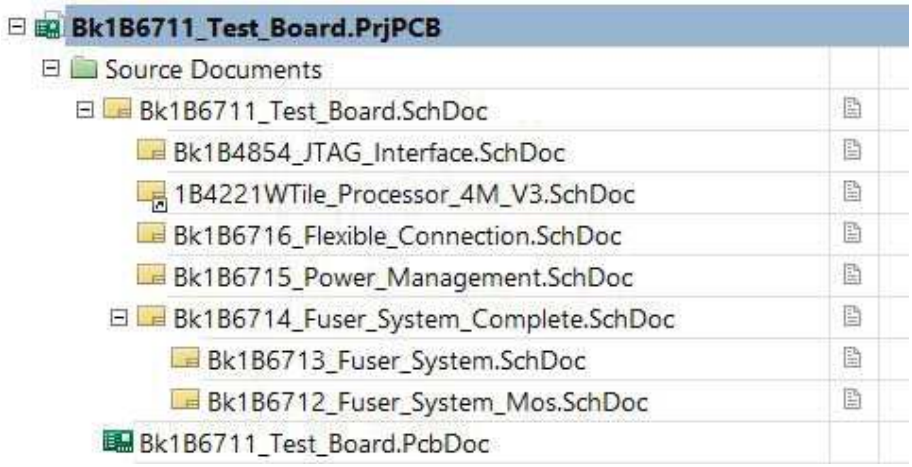


Figure 4.2. Altium project

The figure 4.3 shows Bk1B6711 Test Board.SchDoc, it is the top sheet where all the main elements are represented and connected together. The Bk1B6714 Fuser System Complete is the sheet where the thermal fusers have been described, it is connected to MODULE_A and MODULE_B of the processor. The Bk1B6715 Power Management provides the different power supplies for all the component of the Test Board processing the 14 V PDB, which come from the connector J2. The Bk1B6716 Flexible Connection is the sheet where the connection with the deployable

solar panels' structure have been described, it is connected to the processor by the MODULE_D. The Bk1B4854 JTAG Interface should be used to upload the firmware in the MSP430 through the MODULE_JTAG.

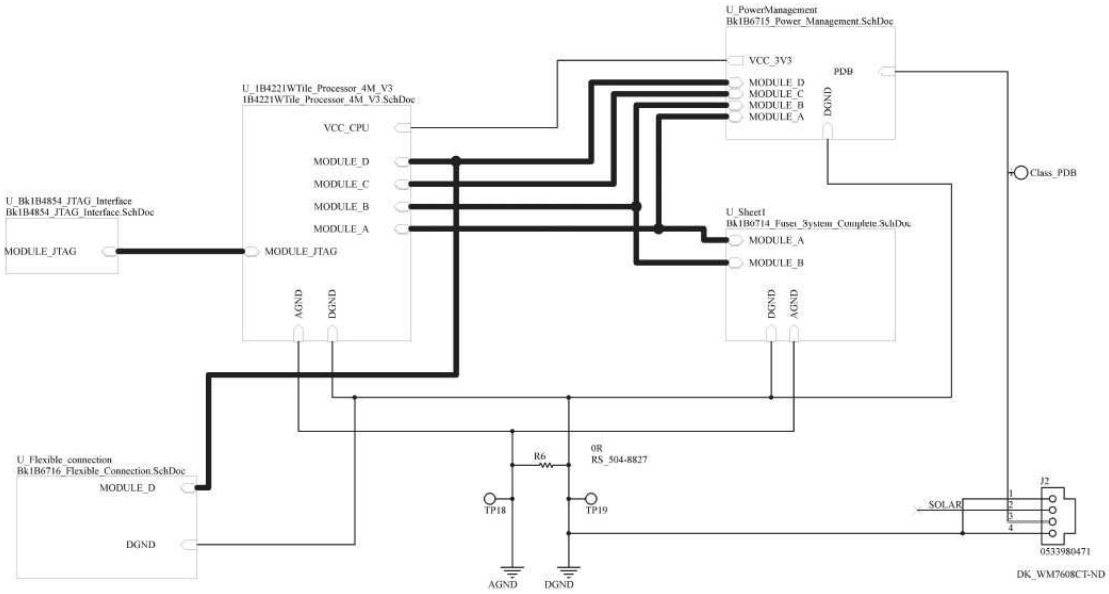


Figure 4.3. Bk1B6711_Test_Board

4.1 Bk1B6712 and Bk1B6713

The Bk1B6712 Fuser System and Bk1B6713 Fuser System Mos are systems composed by: the thermal fuser, the resistances for the linearization circuit of the NTC and resistance connected to the gates of the 2CH-MOS to enable and disable the thermal fuser. The figures 4.4 and 4.5 shown the sheets that describe the concept of thermal fuser express in the figure 4.1.

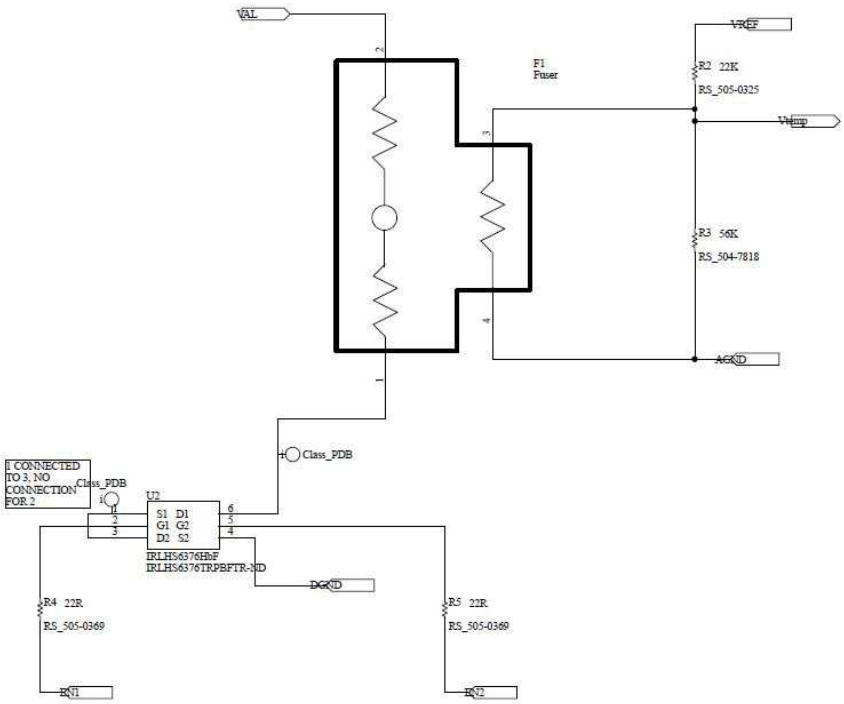


Figure 4.4. Altium sheet of Bk1B6713_Fuser_System

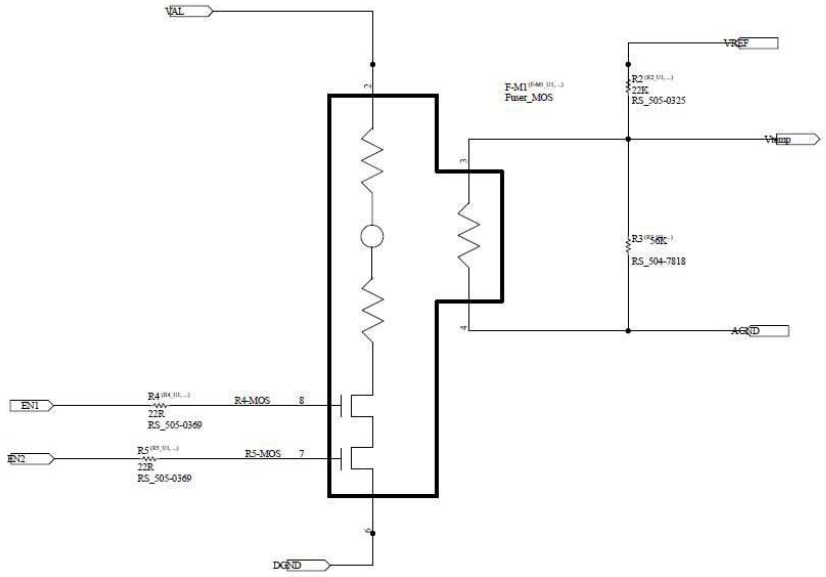


Figure 4.5. Altium sheet of Bk1B6712_Fuser_System_Mos

The symbol used to describe the thermal fuser is in series configuration, but it is not important to the system.
The Bk1B6712 Fuser System and Bk1B6713 Fuser System Mos have been also described into Visual Paradigm using the UML class diagram, as is reported in the figure 4.6.

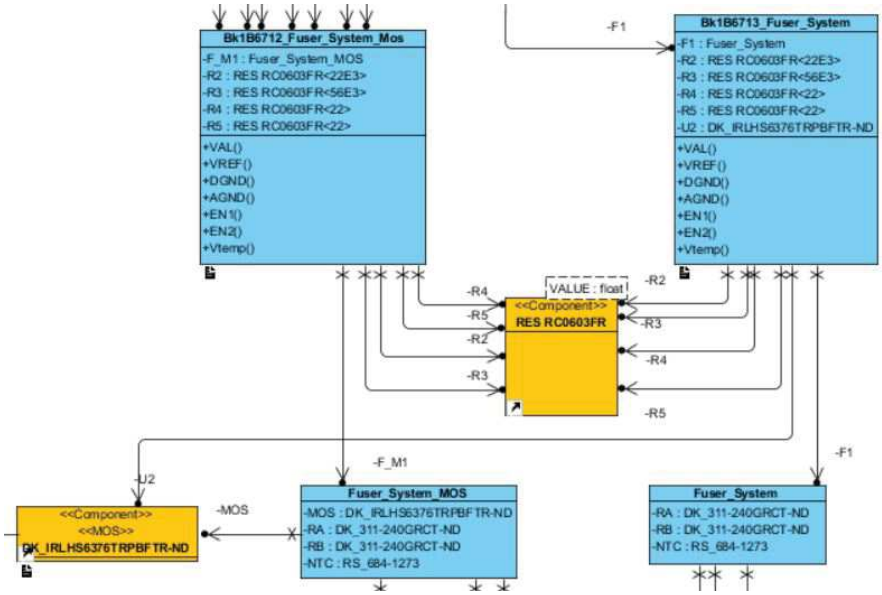


Figure 4.6. Class diagram of Bk1B6712 and Bk1B6713

The Bk1B6712 Fuser System Mos has as thermal fuser component the Fuser System MOS that includes the thermal resistances and the NTC but also the 2CH-MOS. The Bk1B6713 Fuser System has as thermal fuser component the Fuser System that includes the thermal resistances and the NTC but not the 2CH-MOS. For this reason, the two transistors are inserted in the Bk1B6713 Fuser System like an external component of the thermal fuser as it is described in the figure 4.4. The connections have been made in order to guarantee the correct behaviour of the thermal fuser. The *Class_PDB* has been created to make a rule, in the PCB design, in order to have the width of the connection of 0.4 mm, the same in the case of the Bk1B6712 Fuser System Mos.
The same family of resistances is used to drive the DK_IRLHS6376TRPBFTR-ND MOSFET and to build the linearization circuit of the NTC. The value of these resistances have been reported in the class diagram 4.6 and in the table 4.1.

Resistance	Value
R_2	22 $[k\Omega]$
R_3	56 $[k\Omega]$
R_4	22 $[\Omega]$
R_5	22 $[\Omega]$

Table 4.1. Resistances value

The Bk1B6712 Fuser System and Bk1B6713 Fuser System Mos have the same inputs and output. DGND is the digital ground used by the 2CH-MOS and AGND is the analog ground used by the NTC and its linearization circuit. VAL is the 14V PDB used by the thermal fuser to produce heat and VREF is 3V and it is the power supply of the linearization circuit. The other two inputs, EN1 and EN2, are the signals capable to enable and disable the thermal fuser. The voltage of the NTC is the only output of the thermal fusers, it has been used for the feedback control of the temperature.

4.2 Bk1B6714_Fuser_System_Complete

Eight thermal fusers and the multiplexer compose the Bk1B6714 Fuser System Complete. The MUX connects the voltage output of the NTC to the microcontroller.

The Bk1B6714 Fuser System Complete has been described also in UML class diagram in figure 4.10 and in a sheet of *Altium Designer* in figure 4.9.

First of all the multiplexer chosen is 296-43931-2-ND. The figure 4.7 shows functional block of the MUX. The device is actuated in single-end mode, as the output signal of the NTC ranges from 0 to 2.2 V. The output dynamics of the MUX are rail-to-rail so the output can reach the power supply voltage of the device. Thus, since the NTC output range has a maximum value of about 2.2V, the power supply voltage of the MUX has been chosen 3V. A decoupling capacitance is insert following the datasheet of the component. The MUX36S08 has very low on and off leakage currents, allowing this multiplexer to switch signals from high input impedance sources with minimal error. A low supply current of 45 μA enables use in portable applications.

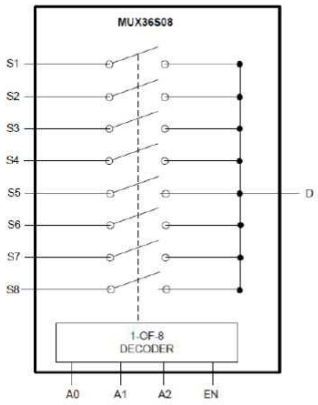
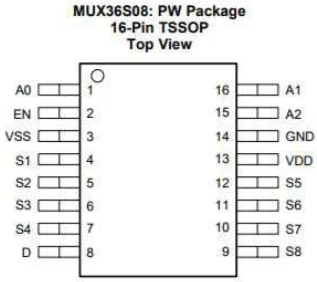


Figure 4.7. Functional block of the multiplexer



Pin Functions: MUX36S08

PIN		FUNCTION	DESCRIPTION
NAME	NO.		
A0	1	Digital input	Address line 0
A1	16	Digital input	Address line 1
A2	15	Digital input	Address line 2
D	8	Analog input or output	Drain pin. Can be an input or output.
EN	2	Digital input	Active high digital input. When this pin is low, all switches are turned off. When this pin is high, the A[2:0] logic inputs determine which switch is turned on.
GND	14	Power supply	Ground (0 V) reference
S1	4	Analog input or output	Source pin 1. Can be an input or output.
S2	5	Analog input or output	Source pin 2. Can be an input or output.
S3	6	Analog input or output	Source pin 3. Can be an input or output.
S4	7	Analog input or output	Source pin 4. Can be an input or output.
S5	12	Analog input or output	Source pin 5. Can be an input or output.
S6	11	Analog input or output	Source pin 6. Can be an input or output.
S7	10	Analog input or output	Source pin 7. Can be an input or output.
S8	9	Analog input or output	Source pin 8. Can be an input or output.
VDD	13	Power supply	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VDD and GND.
VSS	3	Power supply	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VSS and GND.

Figure 4.8. Pin configuration and functions of the multiplexer

Second of all it is possible consider the Bk1B6714 Fuser System Complete. There is one Bk1B6712 Fuser System connected to the input S1 of the multiplexer, the others seven thermal fusers are Bk1B6713 Fuser System Mos connected to the inputs S2 to S8 of the multiplexer. A0, A1 and A2 are used by the microcontroller to decoder the eight thermal fusers. The enable signal EN is the same as that used in the thermal fusers. D is the output of the multiplexer and the input of the microcontroller.

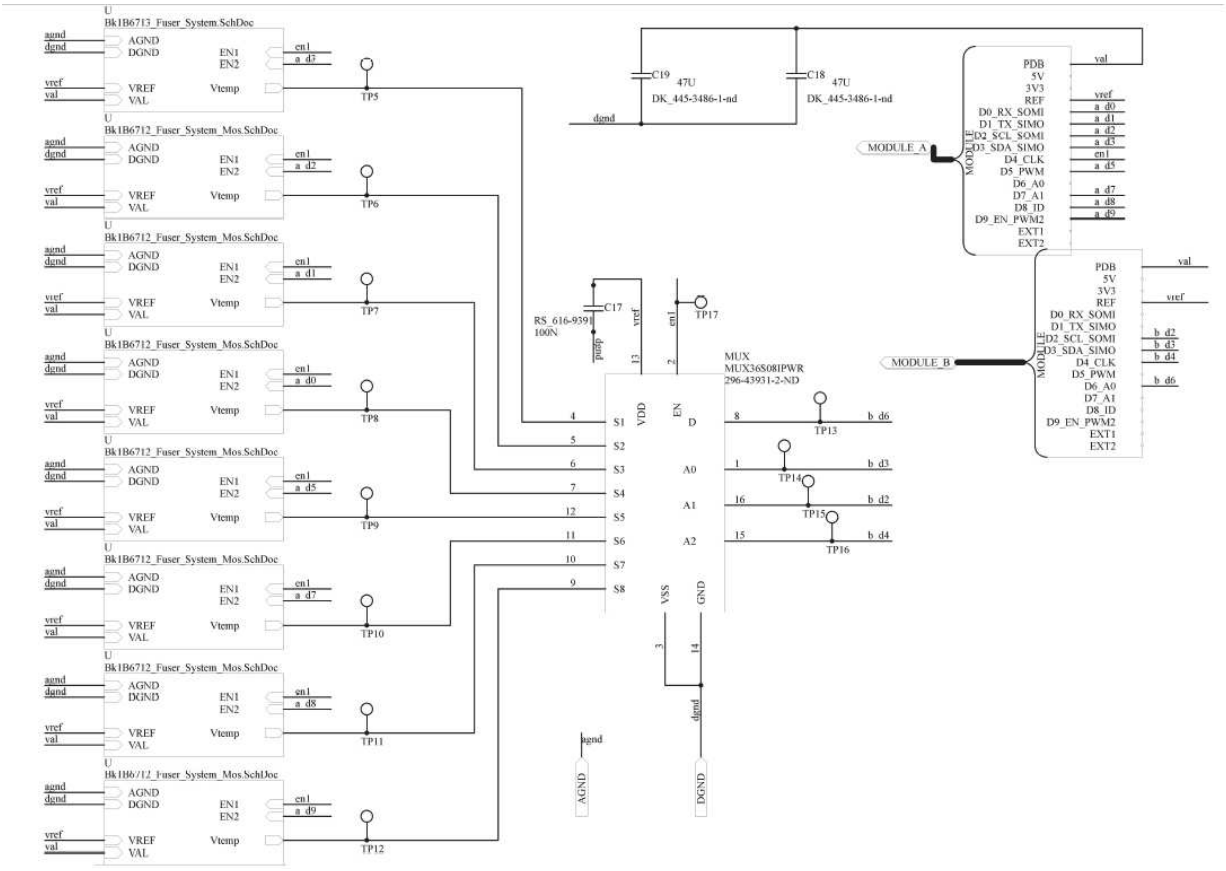


Figure 4.9. Altium sheet of Bk1B6714_Fuser_System_Complete

Modules A and B are used to handle the connections between the Bk1B6714 Fuser System Complete and microcontroller. The tables 4.2 and 4.3 shown the connections between thermal fusers and MODULE_A and between multiplexer and MODULE_B respectively. The MODULE_B decodes V_{temp} and the MODULE_A disable the thermal fusers.

Thermal Fuser connection	MODULE_A
$VREF$	REF
VAL	PDB
$EN1$	D4_CLK
F1 $EN2$	D3_SDA_SIMO
F_M1_U1 $EN2$	D2_SCL_SOMI
F_M1_U2 $EN2$	D1_TX_SIMO
F_M1_U3 $EN2$	D0_RX_SOMI
F_M1_U4 $EN2$	D5_PWM
F_M1_U5 $EN2$	D7_A1
F_M1_U6 $EN2$	D8_ID
F_M1_U7 $EN2$	D9_EN_PWM2

Table 4.2. Thermal fusers connection

MUX connection	MODULE_B
D	D6_A0
$A0$	D3_SDA_SIMO
$A1$	D2_SCL_SOMI
$A2$	D4_CLK

Table 4.3. Multiplexer connection

Focusing on the figures 4.9 and 4.10, two more capacitances are added in the Bk1B6714 System Complete, C18 and C19. These two capacitors of 47μF have been used to decouple the PDB and DGND in order to stabilize the power supply. For this reason they have been chosen with a 2220 package, it is bigger than the 0603 package used for the resistances of the thermal fusers. The bypass capacitor is a condenser used to eliminate any interference with the main signal. In fact, it has a widespread use to bring only parasitic signals into the mass without mass-flowing the DC polarization voltages. This effect is only achieved through a high capacity of the bypass capacitor.

The Bk1B6714 System Complete has been fully described in UML class diagram as it shown in the figure 4.10. How it can be see seven Bk1B6713 Fuser System Mos and only one Bk1B6712 Fuser System have been used. These are called F_M1_U1 to F_M1_U7 as reference for the thermal fusers that include 2CH-MOS and F1 as reference for the thermal fuser without 2CH-MOS.

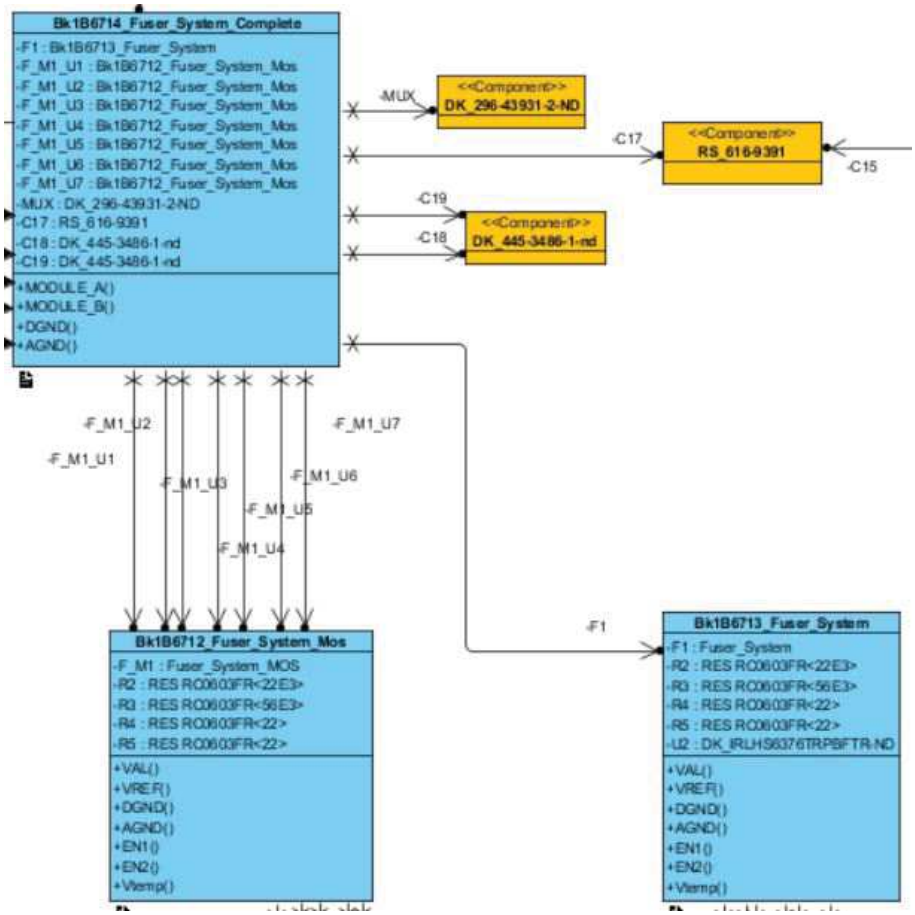


Figure 4.10. Class diagram of Bk1B6714_Fuser_System_Complete

4.3 1B4221WTile_Processor_4M_V3

The microcontroller is the element used in managing the thermal fusers. In the Bk1B6711 Test Board will only be used for this purpose, since the thermal fusers has been designed to be integrated with other systems and will not have its own microcontroller control unit. The MSP430 microcontroller used for the Bk1B6711 Test Board is the same as used for other types of ARAMIS subsystems. It is a 16-bit RISC architecture and a low power MCU. The system clock can work up to 18 MHz. Of all the MCU features, only two are important for the thermal fusers: the ADC and timers. The MCU has a 12-bit ADC with 14 external and two internal channels and also has three different 16-bit timers that will be useful when switching between input signals from NTC sensors. For proper operation, the requirements are decoupling capacitors to filter power noise. It also needs quartz oscillators for the system's main clock (8Mhz) and for correct timer synchronization (32.768kHz).

All capacitor values are derived from those indicated in the component data sheet. Also from the datasheet a 47kΩ resistor is placed at the reset pin (RST). Table 4.4 shows the synthesis of MCU pin mappings and for what purpose they are used. Unused pins such as those used for power supply, those used for JTAG or unconnected ones are not listed.

MODULE	**Connection**	**pin name**
A	D4_CLK	P3.0/UCB0STE/UCA0CLK
A	D3_SDA_SIMO	P3.1/UCB0SIMO/UCB0SDA
A	D2_SCL_SOMI	P3.2/UCB0SOMI/UCB0SCL
A	D1_TX_SIMO	P3.4/UCA0TXD/UCA0SIMO
A	D0_RX_SOMI	P3.5/UCA0RXD/UCA0SOMI
A	D5_PWM	P4.6/TB0.6
A	D7_A1	P6.1/A1
A	D8_ID	P1.0/TA0CLK/ACLK
A	D9_EN_PWM2	P1.3/TA0.2
B	D6_A0	P6.2/A2
B	D3_SDA_SIMO	P3.1/UCB0SIMO/UCB0SDA
B	D2_SCL_SOMI	P3.2/UCB0SOMI/UCB0SCL
B	D4_CLK	P3.3/UCB0CLK/UCA0STE

Table 4.4. Microcontroller unit pins configuration

- *D4_CLK* of *MODULE_A* is the global enable of the thermal fusers. When this pin is low, the multiplexer, the linearization circuits and the drivers of thermal fusers are all disabled. When this pin is high, all the normal functions of the thermal fusers are enable.

- The other pins of *MODULE_A* are the individual enable of the thermal fusers drivers. When this pin is low thermal fusers is disabled. When this pin is high the it is enabled.

- *D6_A0* of *MODULE_B* is the analog input pin of the ADC used for the conversion of output D of the multiplexer.

- The last pins of the *MODULE_B* are digital output pin for the input selection (A0, A1, A2) of the multiplexer.

4.4 Bk1B6715_Power_Management

The subsystems of the Bk1B6711 Test Board needs several power supply to work properly. The 14V PDB must be adjusted to have different values of power supply, therefore the test board needs of three voltage regulators. The microcontroller requires a power supply of 3.3V while the linearization circuit for NTC needs a power supply of 3V. The regulators provide 3.3V, 5V and 3V, and these voltage levels can be used also for other satellite subsystems. Thus, sequence of voltage regulators has been used to provide the power supplies needed to the Bk1B6711 Test Board, as it is shown in the figure 4.11.

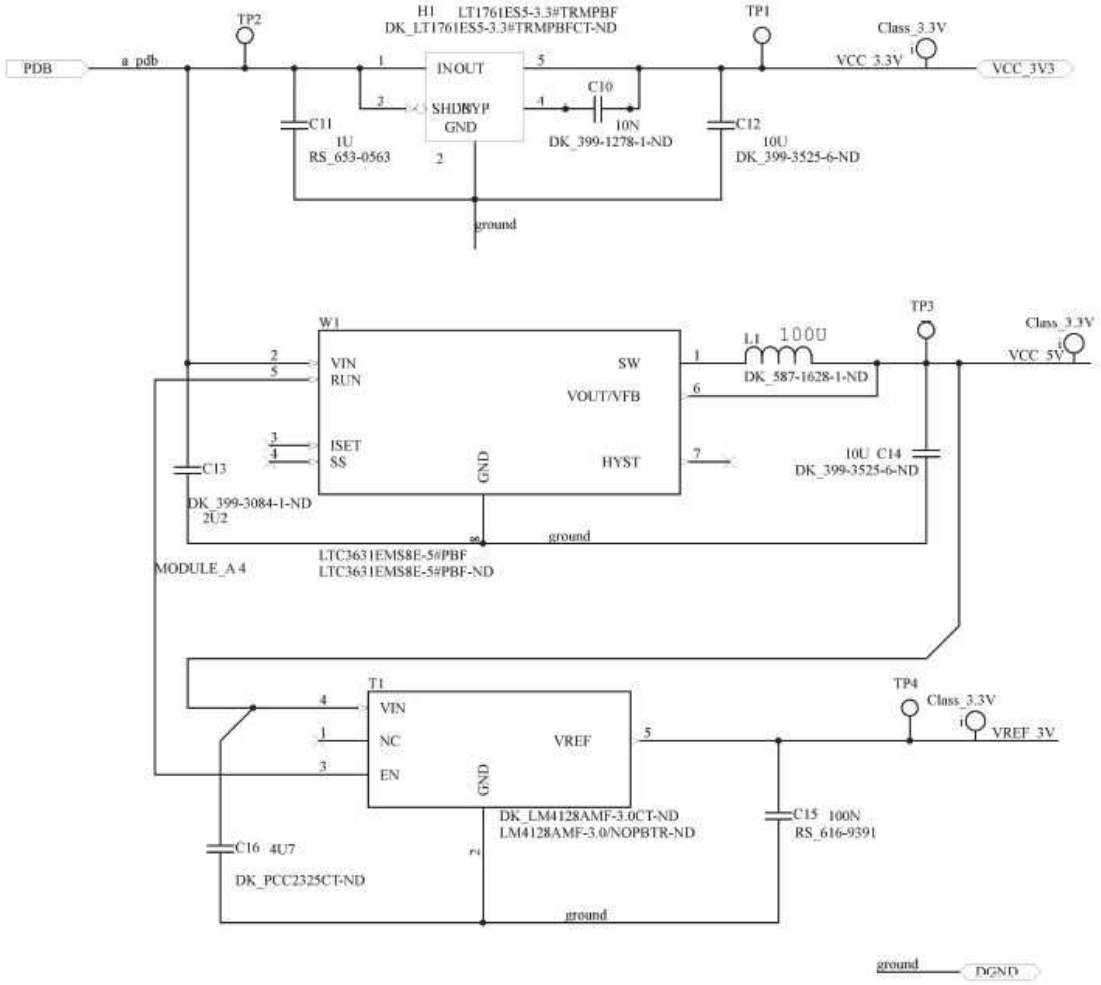


Figure 4.11. Bk1B6715_Power_Management

Three different regulators are used to provide two power supply needed to the system.
The first one is LT1761ES5-3.3#TRMPBFCT-ND, called H1, it produces the 3.3V required using 14V PDB. The LT1761 is micropower, low noise, low dropout regulator. With an external $0.01\mu F$ bypass capacitor, output noise drops to $20\mu V_{RMS}$ over a 10Hz to $100k$Hz bandwidth. Designed for use in battery-powered systems, the low 20μ quiescent current makes them an ideal choice. In shutdown, quiescent current drops to less than $0.1\mu A$. The devices are capable of operating over an input voltage from 1.8V to 20V, and can supply $100mA$ of output current with a dropout voltage of 300mV. Quiescent current is well controlled, not rising in dropout as it does with many other regulators. The LT1761 regulator is stable with output capacitors as low as $1\mu F$. Small ceramic capacitors can be used without the series resistance required by other regulators Internal protection circuitry includes reverse battery protection, current limiting, thermal limiting and reverse current protection. The function of every pins is reported:

- **IN** (PIN1): Input. Power is supplied to the device through IN pin. A bypass capacitor is required on this pin if the device is more than six inches away from the main input filter capacitor. In general, the output impedance of a battery rises with frequency, so it is advisable to include a bypass capacitor in battery-powered circuits. A bypass capacitor of $1\mu F$ is sufficient. The LT1761 regulator is designed to withstand reverse voltages on the IN pin with respect to ground and the OUT pin. In the case of a reverse input, which can happen if a battery is plugged in backwards, the device will act as if there is a diode in series with its input. There will be no reverse current flow into the regulator and no reverse voltage will appear at the load. The device will protect both itself and the load.

- **GND** (PIN2): ground.

- $\overline{\textbf{SHDN}}$ (PIN3): Shutdown. The $\overline{\text{SHDN}}$ pin is used to put the LT1761 regulator into a low power shutdown state. The output will be off when the $\overline{\text{SHDN}}$ pin is pulled low. The $\overline{\text{SHDN}}$ pin can be driven either by 5V logic or open-collector logic with a pull-up resistor. The pull-up resistor is required to supply the pull-up current of the open-collector gate, normally several microamperes, and the $\overline{\text{SHDN}}$ pin current, typically $1\mu A$. If unused, the $\overline{\text{SHDN}}$ pin must be connected to VIN. The device will not function if the $\overline{\text{SHDN}}$ pin is not connected.

- **BYP** (PIN4): Bypass. The BYP pin is used to bypass the reference of the LT1761 regulator to achieve low noise performance from the regulator. The BYP pin is clamped internally to ± 0.6V (one V_{BE}) from ground. A small capacitor from the output to this pin will bypass the reference to lower the

output voltage noise. A maximum value of $10nF$ can be used for reducing output voltage noise to a typical $20\mu V_{RMS}$ over a 10Hz to 100kHz bandwidth.

- **OUT** (PIN 5): : Output. The output supplies power to the load. A minimum output capacitor of $1\mu F$ is required to prevent oscillations. Larger output capacitors will be required for applications with large transient loads to limit peak voltage transients. In this case, the capacitor used is chosen of $10\mu F$.

The second one is LTC3631EMS8E-5#PBF-ND, called W1, it produces the 5V required by the third regulator, using 14V PDB. The LTC3631 is a high voltage, high efficiency step-down DC/DC converter with internal high side and synchronous power switches that draws only $12\mu A$ typical DC supply current at no load while maintaining output voltage regulation. The LTC3631 can supply up to $100mA$ load current and features a programmable peak current limit that provides a simple method for optimizing efficiency in lower current applications. With its wide 4.5V to 45V input range and internal overvoltage monitor capable of protecting the part from 60V surges, the LTC3631 is a robust converter suited for regulating a wide variety of power sources. The function of every pins is reported:

- **SW** (PIN1) : Switch Node Connection to Inductor. This pin connects to the drains of the internal power MOSFET switches.
- **VIN** (PIN2) : Main Supply Pin. A ceramic bypass capacitor should be tied between this pin and GND (Pin 8).
- **ISET** (PIN3) : Peak Current Set Input. A resistor from this pin to ground sets the peak current trip threshold. Leave floating for the maximum peak current ($225mA$). Short this pin to ground for the minimum peak current ($50mA$). A $1\mu A$ current is sourced out of this pin.
- **SS** (PIN4) : Soft-Start Control Input. A capacitor to ground at this pin sets the ramp time to full current output during start-up. A $5\mu A$ current is sourced out of this pin. If left floating, the ramp time defaults to an internal $0.75ms$ soft-start.
- **RUN** (PIN5) : Run Control Input. A voltage on this pin above $1.2V$ enables normal operation. Forcing this pin below $0.7V$ shuts down the LTC3631, reducing quiescent current to approximately $3\mu A$. This pin is connected to D4_CLK of MODULE_A.
- **VOUT/VFB** (PIN6) : Output Voltage Feedback. For the fixed output versions, connect this pin to the output supply. For the adjustable version, an external resistive divider should be used to divide the output voltage down for comparison to the $0.8V$ reference.

- **HYST** (PIN7) : Run Hysteresis Open-Drain Logic Output. This pin is pulled to ground when RUN (Pin 5) is below $1.2V$. This pin can be used to adjust the RUN pin hysteresis. In this case is no connected.
- **GND** (PIN8) : Ground. The exposed pad must be soldered to the printed circuit board ground plane for optimal electrical and thermal performance.

The third one is LM4128AMF-3.0CT-ND, called T1, it produces the 3V required using the 5V output of the second regulator. Ideal for space critical applications, the LM4128 precision voltage reference is available in the SOT-23 surface-mount package. The LM4128 advanced design eliminates the need for an external stabilizing capacitor while ensuring stability with capacitive loads up to $10\mu F$, thus making the LM4128 easy to use. Series references provide lower power consumption than shunt references, since they do not have to idle the maximum possible load current under no load to conditions. This advantage, the low quiescent current ($60\mu A$), and the low dropout voltage ($400mV$) make the LM4128 ideal for battery-powered solutions. The LM4128 is available in four grades (A, B, C, and D) for greater flexibility. The best grade devices (A) have an initial accuracy of 0.1% with ensured temperature coefficient of 75 ppm/°C or less, while the lowest grade parts (D) have an initial accuracy of 1.0% and a temperature coefficient of 100 ppm/°C . The pin descriptions is reported in the following table 4.5.

Pin #	**Name**	**Function**
1	N/C	No connected pin, leave floating
2	GND	Ground pin
3	EN	Enable pin, connected to D4_CLK of MODULE_A
4	VIN	Input supply, 5V from the second regulator
5	VREF	Reference output, 3V output

Table 4.5. Pin descriptions

The part of power management of the Bk1B6711 Test Board has been fully described in UML class diagram. All the capacitances have been chosen and the connections to microcontroller have been made.
The figure 4.12 shows the class diagram of the Bk1B6715 Power Management.

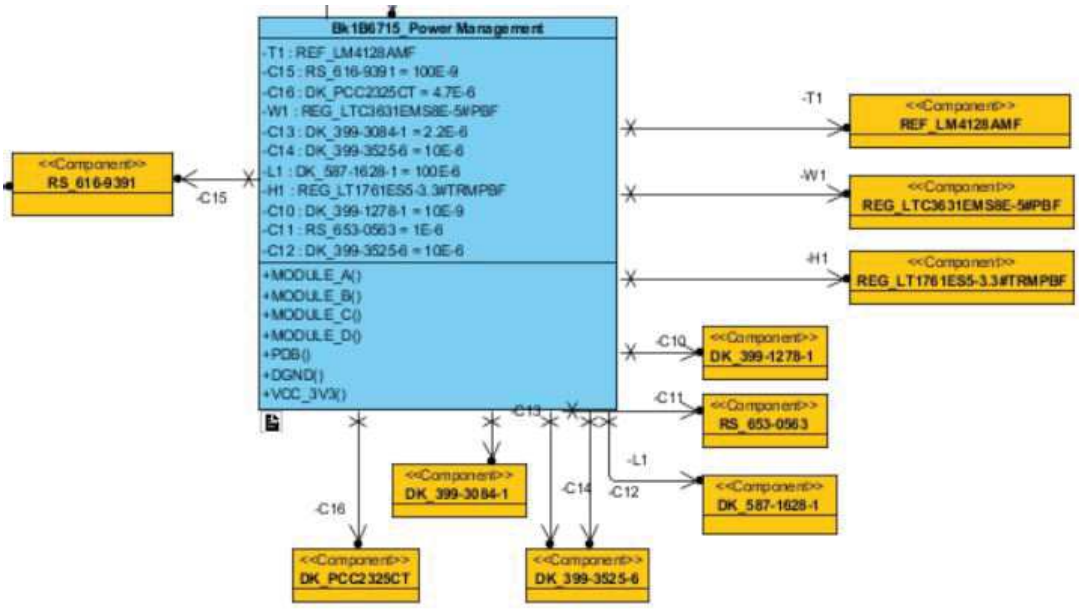


Figure 4.12. Class diagram of Bk1B6715_Power_Management

The Bk1B6715 Power Management provides the supply voltage for the entire Bk1B6711 Test Board, for this reason it must be connected to all the module of 1B4221WTile_Processor_4M_V3. Each module has a wire for these voltage supplies. In the table 4.6 have been reported these connections. The D4_CLK of the MODULE_A has been used to enable the second and the third regulator.

Connection	Net name	Supply
PDB	a_pdb	14V
5V	VCC_5V	5V
3V3	VCC_3V3	3.3V
REF	VREF_3V	3V

Table 4.6. Power Management connections

4.5 Connections

The Bk1B6711 Test Board requires to be connected with the two power channels coming from the 1B111E deployable solar panels' structure and also a connector should be used to upload the firmware into the microcontroller. These connections

have been described in Visual Paradigm using the class diagram representation shown in figure 4.13.
The Bk1B4854 JTAG describes the connector used to upload the firmware into microcontroller and the Bk1B6716 Flexible Connection how the Bk1B6711 Test Board is connected to the deployable solar panels' structure.

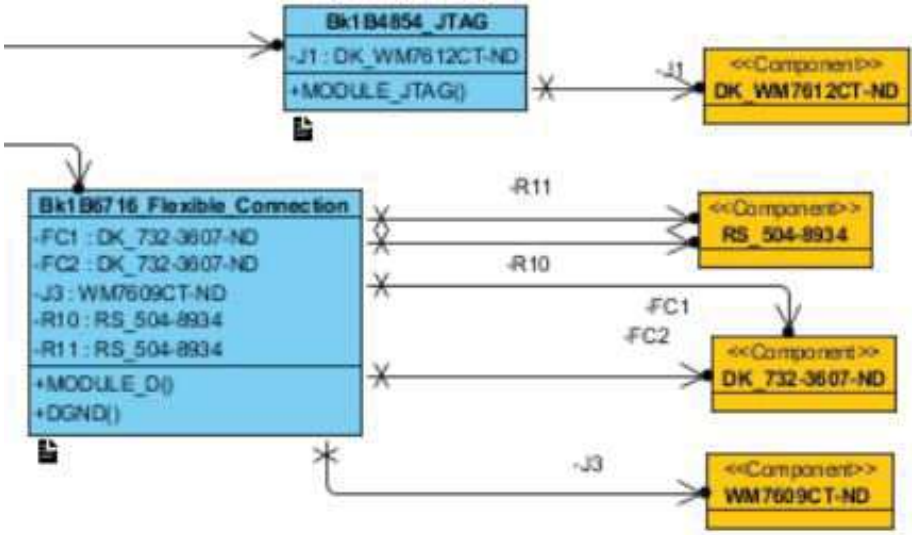


Figure 4.13. Class diagram of Connections

4.5.1 Bk1B4854_JTAG

The Bk1B4854 JTAG is simply a connector used to upload the firmware in MSP430 by MODULE_JTAG. It is a MOLEX connector of PicoBlade series with six position and rectangular shape. The physical characteristics have been described in the figure 4.14. The vertical dimension is too high to be positioned in the top layer of the Bk1B6711 Test Board, therefore it has been mounted in the bottom layer because the P-POD compatibility.

In the table 4.7 is shown how the Bk1B4854 JTAG should be connected to MODULE_JTAG of the MSP430.

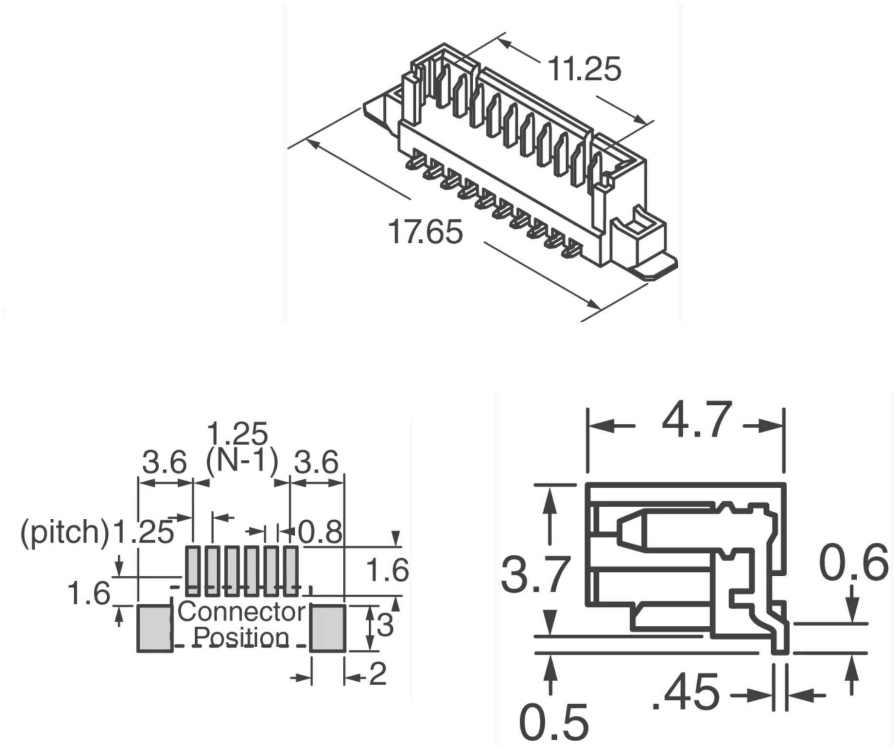


Figure 4.14. JTAG connector

Pin Connector	MODULE_JTAG
1	TDO
2	J_GND
3	TDI
4	J_VDD
5	TMS
6	TCK
7	TEST
8	RST

Table 4.7. JTAG connections

4.5.2 Bk1B6716_Flexible_Connection

The Bk1B6716 Flexible Connection describes how is possible to connect the Bk1B6711 Test Board and the two power channels that transfer the power accumulated in the solar cells of the 1B111E structure. Two flexible cable have been chosen to do that. They are connected to the MSP430 by MODULE_D. A connector with two pull

up resistor have been inserted to verify the correct behaviour of the Bk1B6711 Test Board. The figure 4.15 shows the Altium schematic.

The connector J3 is of the same series of the JTAG connector, for this reason the main characteristic are not reported. The only difference is the number of position that in this case is 5 instead of 8. Two pull-up resistors of $10k\Omega$ with 0603 package have been used to force pin 3 and 4 to high logic level to test the power coming from the channel of the solar panels' structure. For the same reason as in the case of JTAG connector, the too high vertical dimension, J3 is mounted in the bottom layer of the Bk1B6711 Test Board.

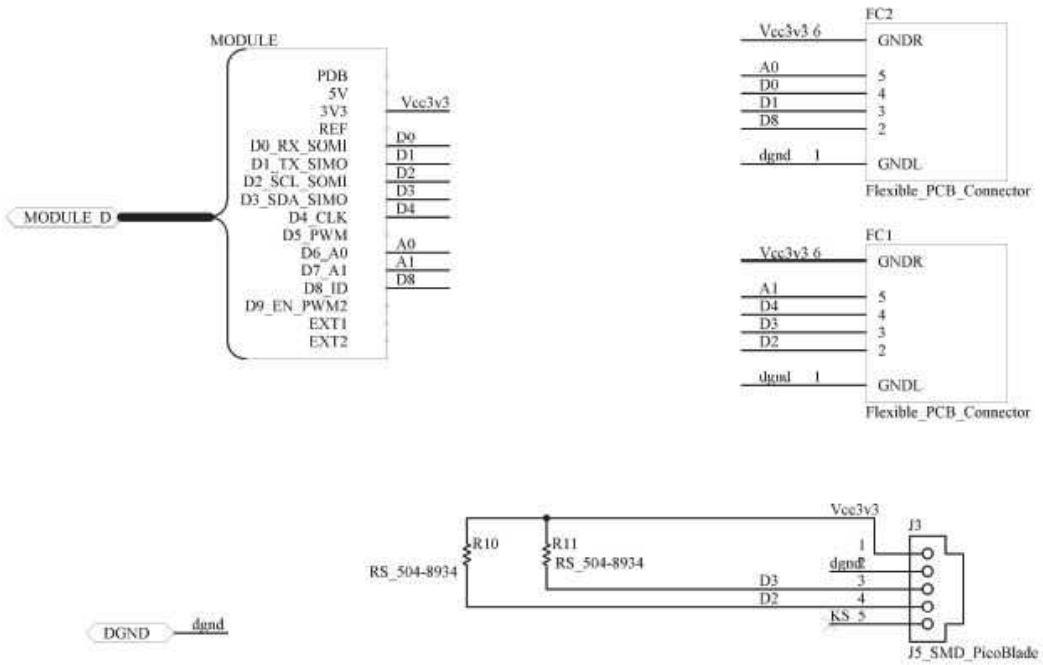


Figure 4.15. Bk1B6716_Flexible_Connection

FC1 and FC2 are flexible cable with 8 position. They are 50mm long, 1mm of pitch and 5mm of length between the exposed extremities. The material characteristics have been reported in the table 4.8.

The footprint was created respecting the main characteristic of the flexible cable 686608050001 (manufacturer code), as it is reported in figure 4.16.

Rated current	1 A
Conductor resistance	$< 1.09\ \Omega$/km
Isolation resistance	550 VDC $> 1.000\ M\Omega$
Working voltage	60 V (AC)
Dielectric withstanding voltage	500 VAC/min

Table 4.8. Flexible cable material features

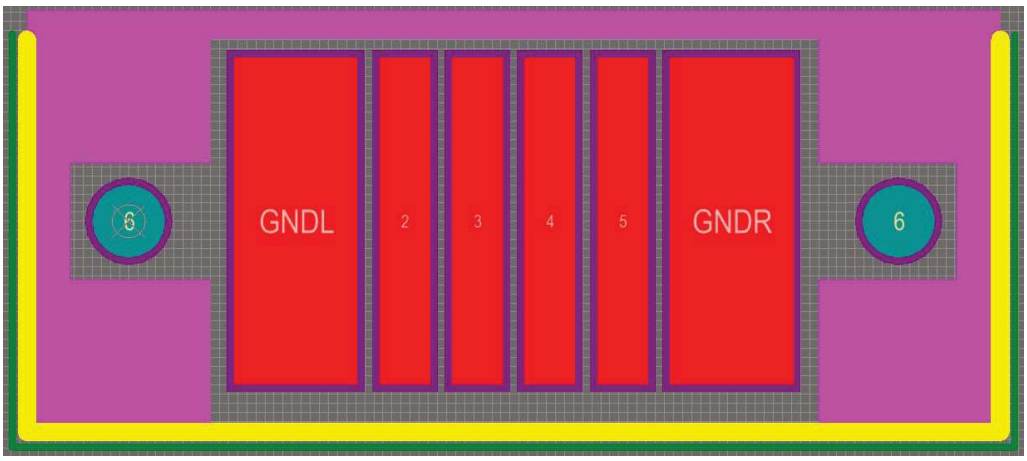


Figure 4.16. Flexible cable footprint

Although the component has 8 positions, there are only six pads in the figure 4.16, but the outer ones have been designed in order to be connected to two flexible cable positions.

The flexible cables have been connected to the MSP430 in order to receive the power accumulated in the solar cells of the 1B111E structure. These connections have been listened in the table 4.9.

The GNDL pads of both flexible cable have been connected to the ground (DGND) of the entire system, for this reason in the table this connection are not reported. The solar panels' need also the power supply of 3.3V, thus the GNDL connections have been used to do that.

It would be better to use a flexible PCB for electrical connections between tiles, without using annoying cables. The connectors may be designed to be SMD so that the flexible PCB can simply be welded without using uncomfortable and bulky connectors. This solution is perfect to minimize the overall dimensions of the cables that may be an obstacle during the deployment phase. In addition, since the flexibility of the PCBs is very subtle, they can be folded over them in a small space to

Flexible Cable	FC pin	MODULE_D
FC1	GNDL	–
FC1	2	D2_SCL_SOMI
FC1	3	D3_SDA_SIMO
FC1	4	D4_CLK
FC1	5	D7_A1
FC1	GNDR	3V3
FC2	GNDL	–
FC2	2	D8_ID
FC2	3	D1_TX_SIMO
FC2	4	D0_RX_SOMI
FC2	5	D6_A0
FC2	GNDR	3V3

Table 4.9. Flexible cables connections

meet the rigid requirements of the P-POD module. But for the purpose of the test board these are not necessary and it is possible use flexible cables.

4.6 Power estimation

The power estimation is the last step for the entire system. The microcontroller does not be inserted in this analysis because it is used by other subsystems and not only by the thermal fusers. The power consumption of the multiplexer has low leakage current. The power estimation is composed by three elements: the eight thermal fusers with the drivers, the eight NTCs and theirs linearization circuit and the voltage regulators. The power consumption of each thermal fuser has been analyzed in chapter 3. The power consumption of each NTC and its linearization circuit can be obtained from the figure 3.14.
The resistance value of the NTC should be considered in the worst case, following the figure 3.14 it is possible consider the $P \simeq 4 \cdot 10^{-4}$ due to the high temperature. The table 4.10 shows the power estimation.

The total power consumptions is less than 13 W required from the specification.

Element	Power	Number of elements	Total Power
Thermal Fuser	1.5 W	8	12 W
NTC and l.c.	400 μW	8	3.2 mW
5V reg	0.35 W	1	0.35 W
3V reg	0.1 W	1	0.1 W

Table 4.10. Flexible cables position

4.7 Bk1B6711_Test_Board Design

The Bk1B6711 Test Board is the system that allows to deploy the 1B111E solar panels' structure. It should respects strictly requirement to be compatible with the solar panels' structure and with the skeleton of the CubeSate. The main components of the system are the Bk1B6714 Fuser System Complete, the 1B4221WTile_Processor_4M_V3, the Bk1B6715 Power Management, the Bk1B4854 JTAG and the Bk1B6716 Flexible Connection.

First of all, the skeleton of the CubeSate and the compatibility with the P-POD module should be respect. The test board has been created following this specification, therefore the dimensions are 98x82.6 mm. Four holes have been made to fix the Bk1B6711 Test Board to the skeleton of the CubeSat. Two holes have been used to fix the hinge where the solar panels' structure has been mounted and other two holes to fix the slide block to avoid the touching between the deployable structure and the Test Board. All the dimensions are reported in in figure 4.17.

The thermal fuser should be mounted in a specific position followed the holes created in the solar panels' structure. The bottom left hole of the board has been used as origin. The thermal fusers have been positioned in the correct position on the top layer as it is reported in the table 4.11. It is important to remember that the thermal fusers have as origin the via where the wire should be soldered.

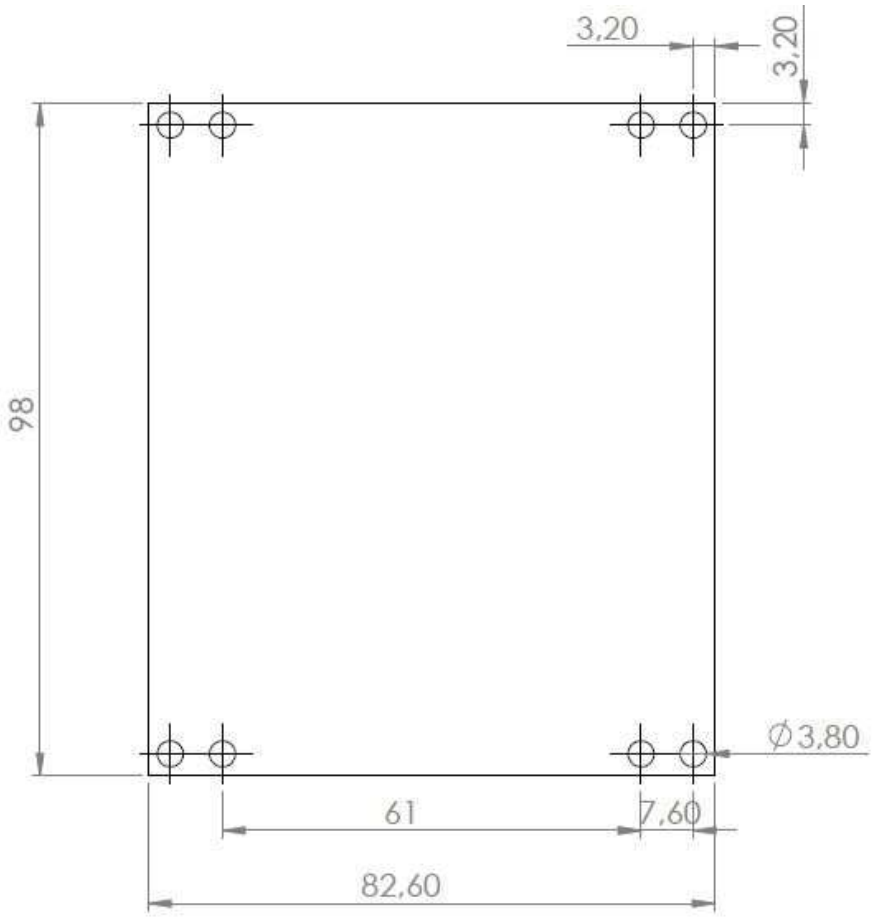


Figure 4.17. Test Board draw

Thermal Fuser	x	y
F1	37.05 mm	91.2 mm
F-M1_U1	-1.65 mm	71.5 mm
F-M1_U2	-1.65 mm	45.5 mm
F-M1_U3	-1.65 mm	19.5 mm
F-M1_U4	37.05 mm	-0.2 mm
F-M1_U5	75.75 mm	19.5 mm
F-M1_U6	75.75 mm	45.5 mm
F-M1_U7	75.75 mm	71.5 mm

Table 4.11. Thermal fusers position

The flexible cables should be positioned in the top part of the figure 4.17. The thermal fuser F1 has been mounted between these cables, their origin is the left holes used to fix firmly the cable. The coordinates have been reported in the table 4.12.

Flexible Cable	**x**	**y**
FC1	17.25 mm	91.3 mm
FC2	46.25 mm	91.3 mm

Table 4.12. Flexible cables position

The components of the Bk1B6714 Fuser System Complete have been positioned on the top layer of the board, only the two capacitors C18 and C19 have been mounted in the bottom layer because their package. All the other components have been positioned in the bottom layer to avoid the touching between the Bk1B6711 Test Board and the 1B111E deployable solar panels's struture. The thermal fusers and the flexible cables are positioned in their specific position, all the other components do not have any restriction about the positioning. The 3D view of the test board is reported in figures 4.18 and 4.19. The top and the bottom of the PCB is reported in figures 4.20 and 4.21 respectively.
The Bk1B6711 Test Board is a four layers board. The two more layer have been used to GND and PDB. They do not reach the area where the thermal fusers have been positioned in order to avoid interferences to the heat generation and measurement. The table 4.13 shows all the layers that compose the Test Board, starting from the top to the bottom.

Layer Name	**Type**	**Material**	**Thickness** (mm)
Top Overlay	Overlay		
Top Solder	Solder Mask/Coverlay	Surface Material	0.01016
Component Side	Signal	Copper	0.03556
Dielectric 1	Dielectric	Core	0.32004
GND	Internal Plane	Copper	0.03599
Dielectric 5	Dielectric	Prepreg	0.127
PDB	Internal Plane	Copper	0.036
Dielectric 6	Dielectric	Core	0.254
Solder Side	Signal	Copper	0.03556
Bottom Solder	Solder Mask/Coverlay	SurfaceMaterial	0.01016
Bottom Overlay	Overlay		

Table 4.13. Layers of the Bk1B6711_Test_Board

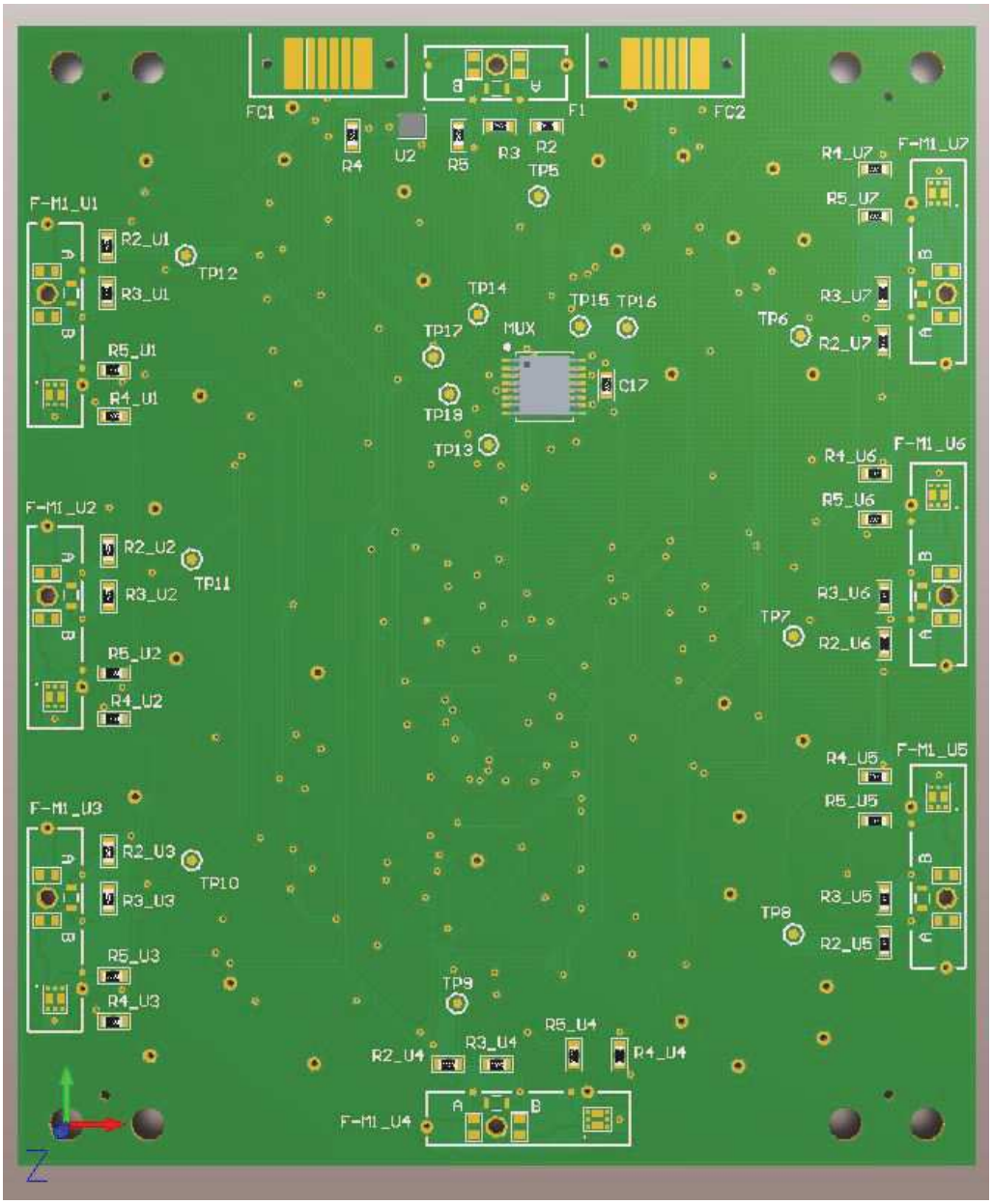


Figure 4.18. Top 3D view

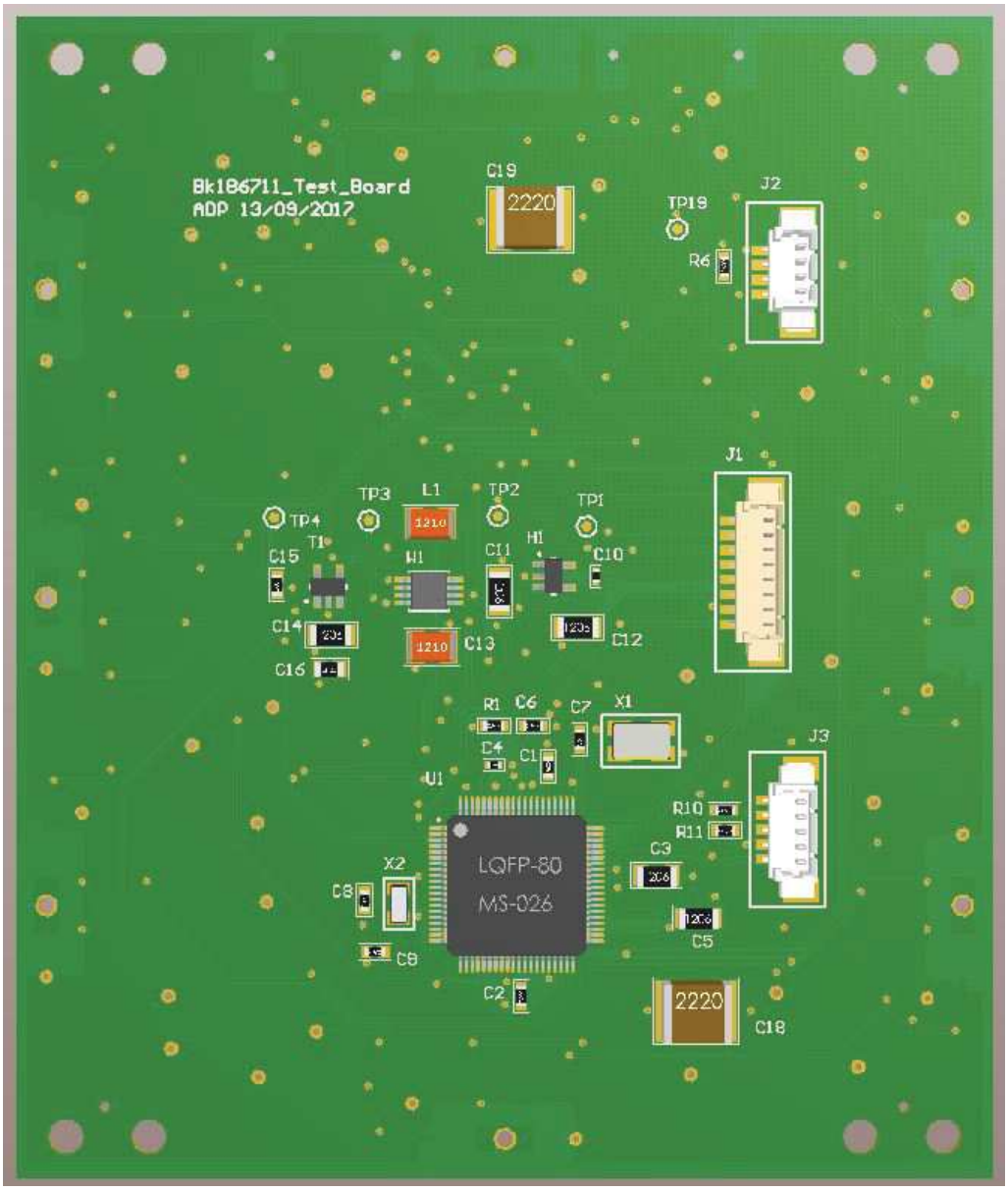


Figure 4.19. Bottom 3D view

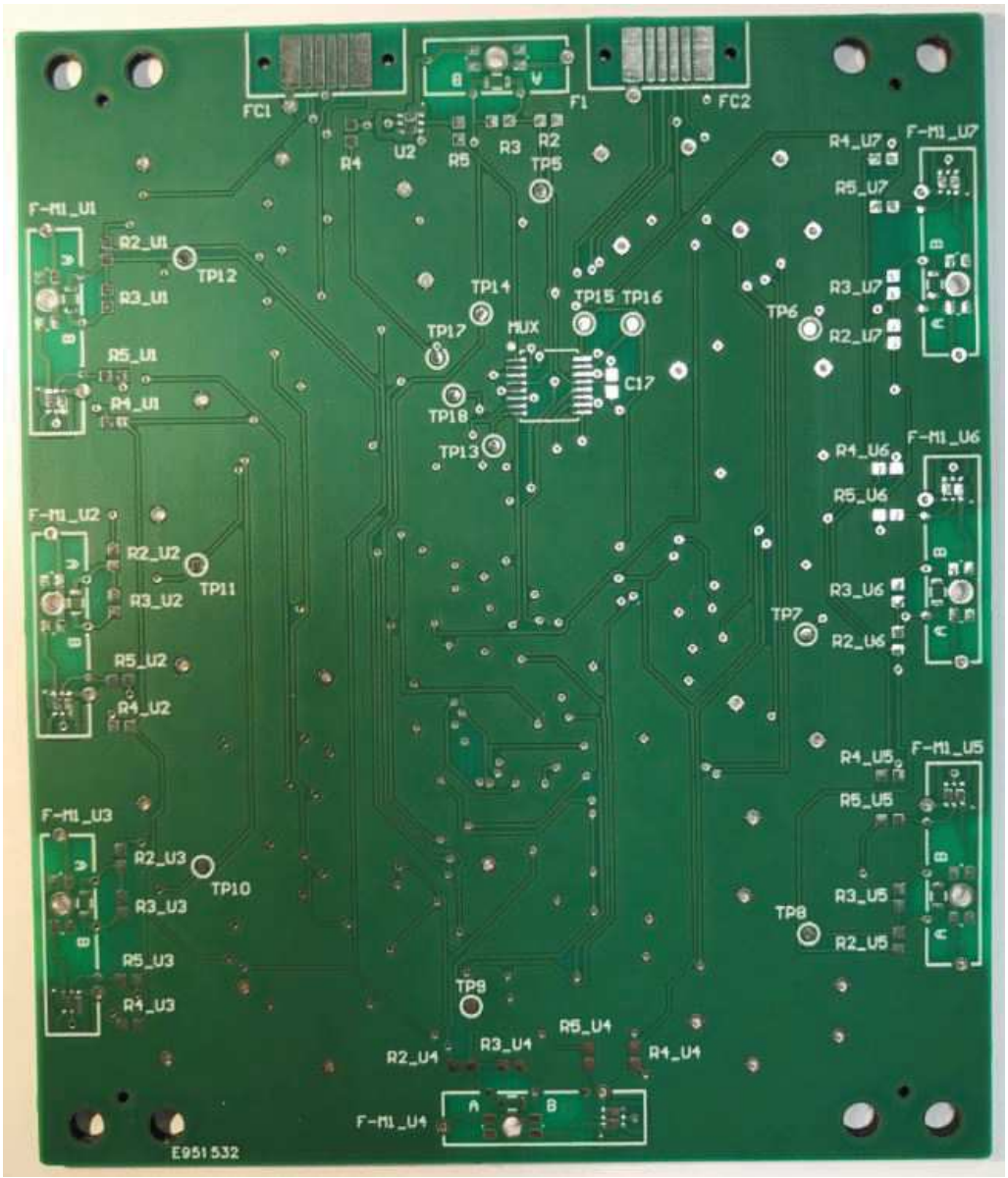


Figure 4.20. Top real view

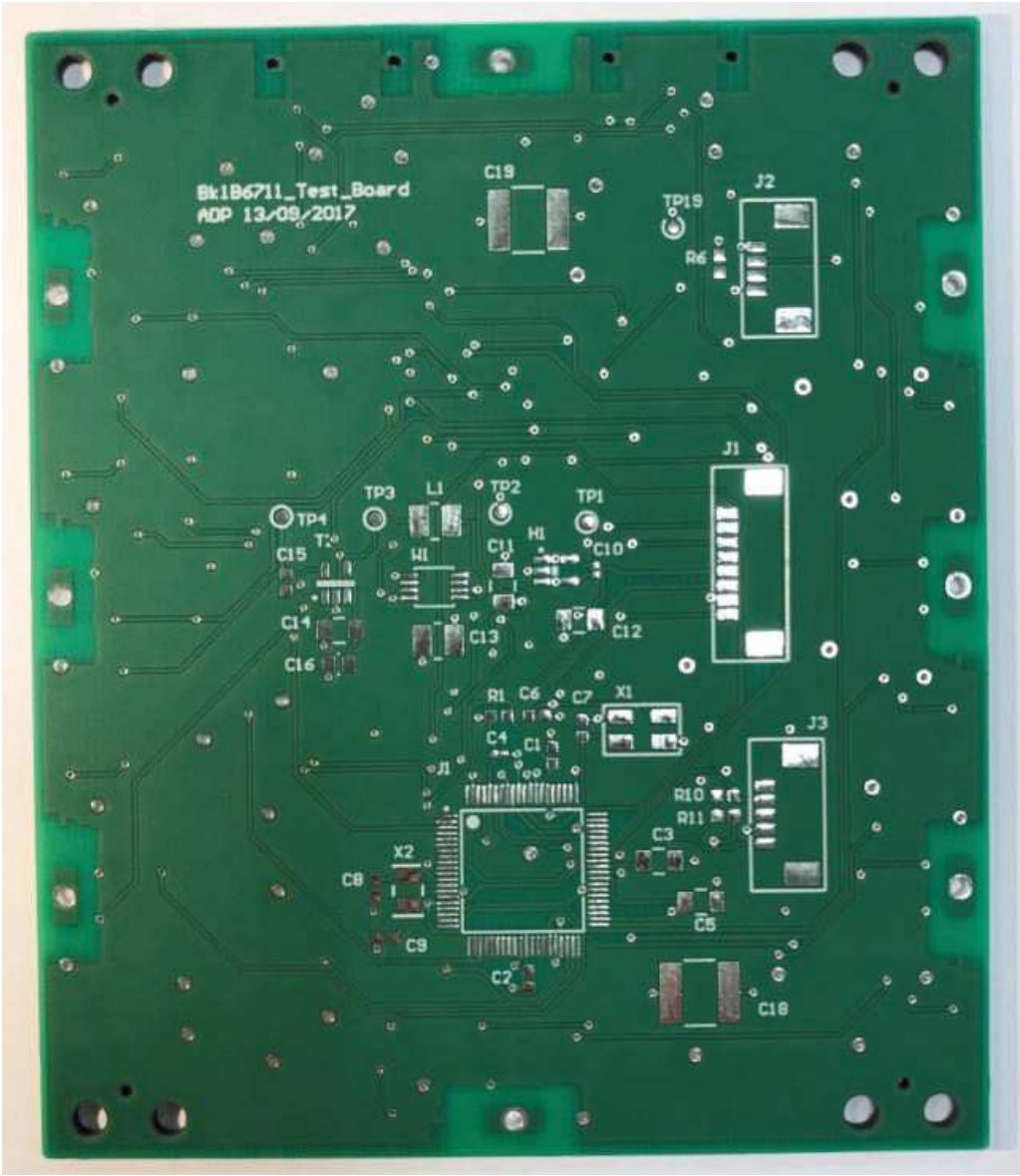


Figure 4.21. Bottom real view

Chapter 5

Bk1B6711_Test_Board Management Software

The microcontroller used for the Test Board management has to be appropriately programmed to realize the correct control of all elements of the Thermal fusers. For the software of Bk1B6711 Test Board has been followed the approach to make the code highly versatility, because it has to be easily handled in order to be implemented and integrated into another future software system of another satellite application. The Firmware has been wrote in C++ and it uses all class libraries and functions ones written for the ARAMIS project. In the in following paragraphs, the UML is used to better understand the software development.

5.1 Software Operation

The main task of the software is the thermal fusers management for the opening phase of the 1B111E deployable solar panels' structure. In the test board, the opening algorithm has been implemented to perform a complete opening phase. The main operations of the management algorithm are described through use case diagram showen in figure 5.1.

The main actors of the test board outer plate are a *Configurator* and a *Ground Mission Controller*. The first represents the user involved into the configuration of the Test Board. Two use cases are possible: the setting of the maximum temperature that the fusers can achieve, and the setting of the number of fusers that can be used. The setting of the max temperature, makes the thermal fusers compatible with a large amount of other applications that require lower temperatures. Also the number of thermal fusers can be set in order to make the Bk1B6714 Fuser System Complete more versatile. The second actor is the *Ground Mission Controller*. This is the main element involved into the control of the entire satellite. It send commands to the on board computer that interprets the instruction, interacting

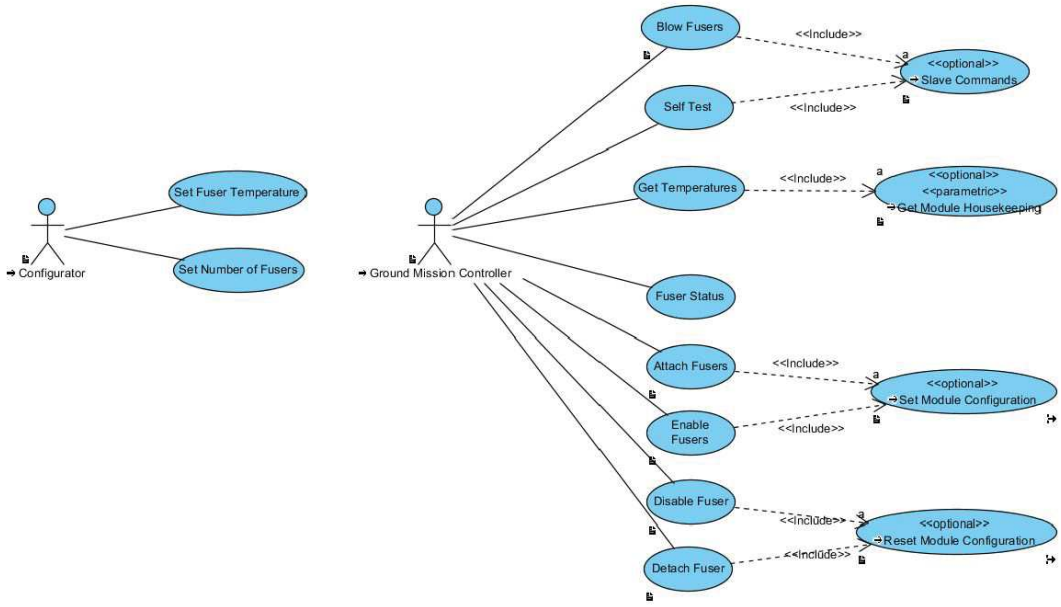


Figure 5.1. Use Case Diagram of the Test Board

with the satellite subsystems. The thermal fusers are triggered by the on board computer thanks to an appropriate command sent from the ground. The firmware of the Bk1B6711 Test Board has been designed taking into account a command incoming from a ground mission controller. This latter has different use cases. A *Blow Fusers* has been used to start the operation of all the thermal fusers of the test board, which are enabled and attached. The temperature of all the fusers enabled, is increased to a set threshold value, and then kept constant. After a certain time from the beginning, all the thermal fusers are turned off automatically. *Get temperatures* gives the possibility to obtain the actual temperature of the thermal fusers. *Self-test* is a useful function, because before a launch, a self-test of heating for the fusers improves the reliability of the Bk1B6714 Fuser System Complete. The use of *Fuser Status* is needed, because the status of the fusers has to be continuously monitored, to maintain the temperature constant and to verify the correct operation of the thermal fusers. All the use cases, *Enable* and *Disable*, and the *Attach* and *Detach* are also needed to instantiate the thermal fusers. These work together a *Configuration Module*. This latter acts on a configuration register, where each bit represents an enable configuration bit for a fuser. In the same register there is also an attach configuration bit. Only the *Disable* case and the *Detach* case, need the *Reset Module Configuration*. This is used to reset all configuration bits of the configuration register. *Blow Fusers* and *Self-Test* use Slave commands to be activated. Instead *Get Temperatures* need the *Get Module Housekeeping* to store the values of

temperature of the thermal fusers.

Now, focusing on the main operation of the thermal fuse. The opening phase basic algorithm is explained using a simple flowchart shown in figure 5.2.

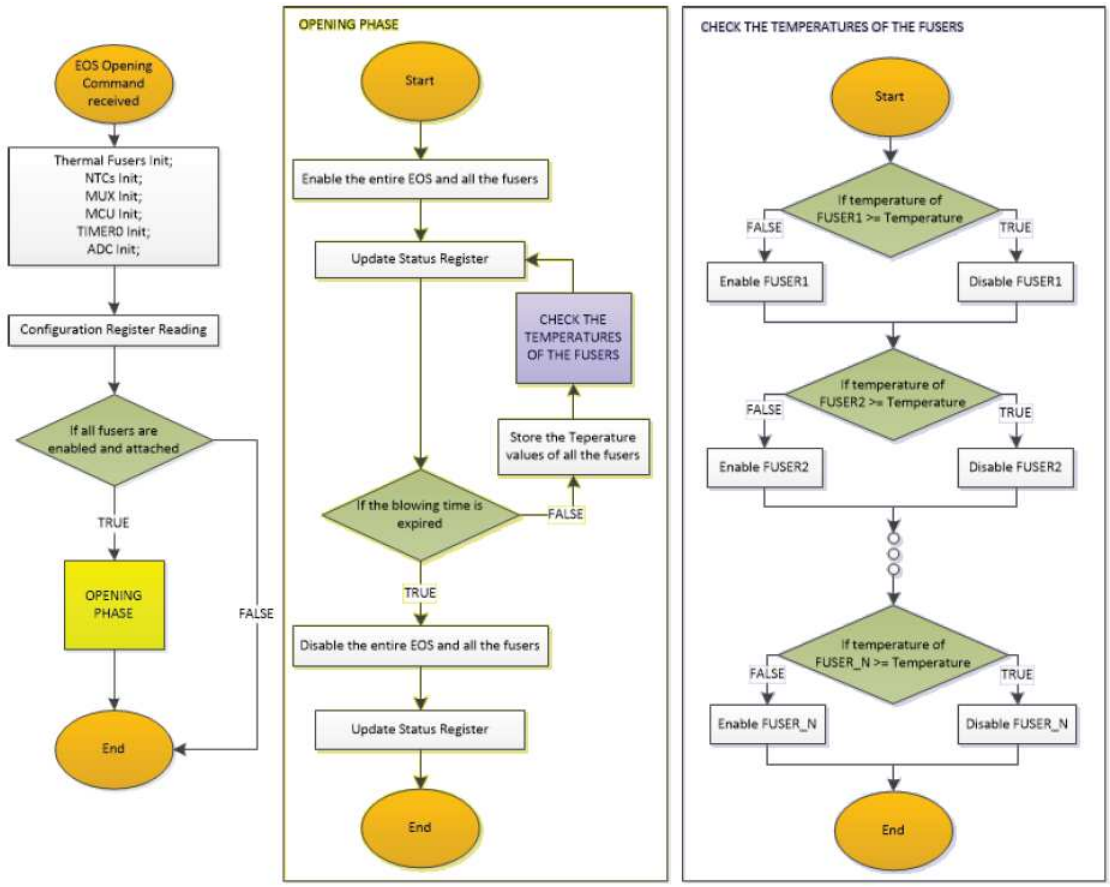


Figure 5.2. Opening Phase Algorithm

The software triggers when the on board computer sent the command of opening to the microcontroller of the Bk1B6711 Test Board. The first state is the initialization of the all devices. Since the software is objects oriented, all devices represent object classes that have to be instantiated and initialised. The initialization involves also the setting of the pins of the microcontroller as outputs or inputs. The configuration register contains all the setting configurations for the enabling of the fusers. These information are used to physically rise or drop, the logic values of the enable pins of the Bk1B6711 Test Board (figure 4.1). If all *enable* bits and the *attach* bit are true, the thermal fusers can be activated and the *OPENING PHASE*

starts. Otherwise the software ends. In these conditions the fusers begin to heat up. Once the *opening phase* starts, the fusers are enabled and the software enters in a first loop. The software, cycles for a certain time. An microcontroller timer is used for counting the time. When a maximum time is reached, the *opening phase* ends, and all the thermal fusers are turned off and disabled. During this time, all temperature from the NTCs sensors are stored into an appropriate vector and are also checked to avoid the exceeding of a maximum temperature threshold. In other words, what happens is that all the thermal fusers are kept to a constant temperature. In the phase of checking, each fuser is disabled if its temperature exceed a maximum threshold, and it is enabled again if its temperature decrease below the same threshold. In this way all fusers can be maintained to a constant temperature, allowing the desoldering of the sealing wires.

5.2 Main Classes

The previous paragraph has been used to introduce the main software system and the base algorithm of the opening phase. In this section all main software classes have been described. The management software has been written following the use case diagram of figure 5.1. Since the software has been written in C++, all devices are instantiated using software classes. For the software designing, a large amount of other classes that already existed, are used. These are the main classes designed for the on board computer taken from the ARAMIS project. For this reason in this section are deals only the specific classes designed for the thermal fusers. All the support classes from the ARAMIS project are described in a marginal way. The software classes have been described in a particular application of the thermal fusers. Since the deploying mechanism can be adapted for many applications, this section is referred to Bk1B213A1 Outer Plate PCB, it is the PCB used for the reaction wheel.

The software classes of the thermal fusers and the NTC sensors are the first classes that have been implemented as it shown in figure 5.3.

Since each thermal fuser contains a NTC sensor, the better choice to organize the software was to instantiate the sensor class directly inside the thermal fuser class. In this way each time a fuser class is instantiated, at the same time, the related sensor class is also instantiated. Each device class is divided into attribute and methods. In the methods are always present a function of initialization (*init()*), a function of housekeeping (*housekeeping()*), an interpreter function (*interptret()*), a supervisor function (*supervise()*) and refresh function (*refresh()*). The init function is employed for the initialization of the device class. The housekeeping performs the main function of the class. The interpreter function has the task to decode the instruction commands. The supervise function performs monitoring tasks.

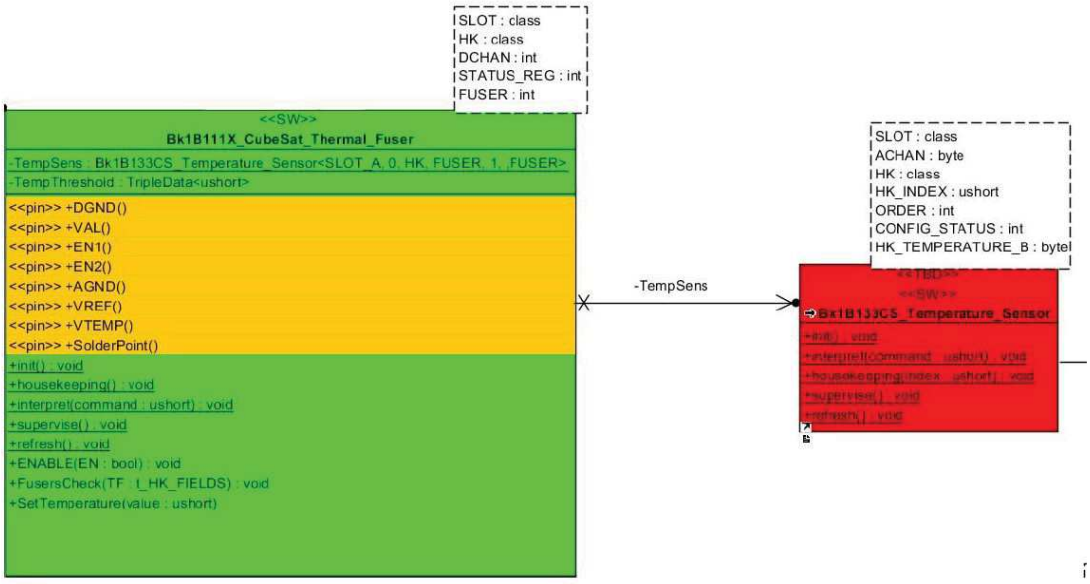


Figure 5.3. Thermal fusers and NTC sensors classes

Instead the refresh function is used to refresh all the variables instantiated, and in particular the variable types most interesting that are those instantiated as *TripleData*. This format is part of a class appropriately designed to improve the robustness of the code to space radiations. When the environment in the space becomes harsher, and the radiations increase, all data stored in the memory elements are easily exposed to problems of switching from a logic state to another. To avoid this, a statistic technique is used to protect the data and thus reduce the possibility of failures. If a variable is instantiated as *TripleData*, three copies of the data of that variable are performed in memory. The statistical probability that a data changes in two of the three memory locations, for effect of radiation, is low. In this way, each time the refresh function is launched, it is performed a triple check on the three copies of the data. If one location of data is changed, the refresh function restores to all the three memory locations the value of the other two locations not changed. The most critical data are all protected by a *TripleData* type. For example, the temperature maximum threshold (*TempThreshold*) is a *TripleData* because if the temperature changes in a higher value, the fusers can reach a very high temperature thus damaging the system. All classes present also a set of template parameters, used for the instantiation of the classes. The init function of the thermal fuser class performs the enabling of the right microcontroller pin as output, used for the enable signal of the fuser.

The housekeeping methods launch the houskeeping of the sensor class, which

store the value of temperature in the *HK::housekeeping[]* vector. Furthermore, it runs the *FuserCheck()* method that performs the comparison of the temperature with the *TempThreshold*. The result of the *FuserCheck()* can be a fuser enabling or disabling, depending on the result of the comparison. *SetTemperature()* is used to give the value to the *TempThreshold* variable. The temperature value is passed by template parameter. *ENABLE()* is a function used to physically rise or drop the logic level of the microcontroller pin of enable of the corresponding thermal fuser. The sensor method *init()* performs the initialization of the pin of the A0 channel of the ADC used. The housekeeping of the same class instead performs an algorithm of conversion from the value obtained by the ADC, to the right value of temperature. The algorithm is based to the possibility of use different linearization circuits for the NTC sensors, characterized by different orders of linearization. In my case, the linearization circuit is of the 1th order, thus no equation of linearization has been applied to the ADC value.

The other class used is for the MUX. The class is shown in Figure 5.4.

Figure 5.4. MUX class

The *init()* function of the class has been used to set the output type for the microcontroller pin used for the selection controls of the MUX. The *housekeeping* and the *SELECT* functions, are used together for the correct switching from a channel of the MUX to another. An incrementing index provided by the *TIMER* used for the counting in the microcontroller, has been used to select the time instants where the switching between the channels of the MUX have to occur. For now, the index of the *TIMER* is incremented each 1ms. So the software, switches from a channel of the MUX to another each 1ms. Instead for the temperature readings of the thermal fusers, each polling of eight sensors is performed each 1 second. Also in this case, the

MUX class is designed with the maximum of versatility and portability, using the template parameters to pass the channel of the *SLOT*s that are following assigned to the control pins of the MUX. No other devices of the thremal fusers need to be instantiated with a separate class. Thus only two classes remain to be defined: the class of the *main()*, and the Test Board main class. The figure 5.5 shown the last one.

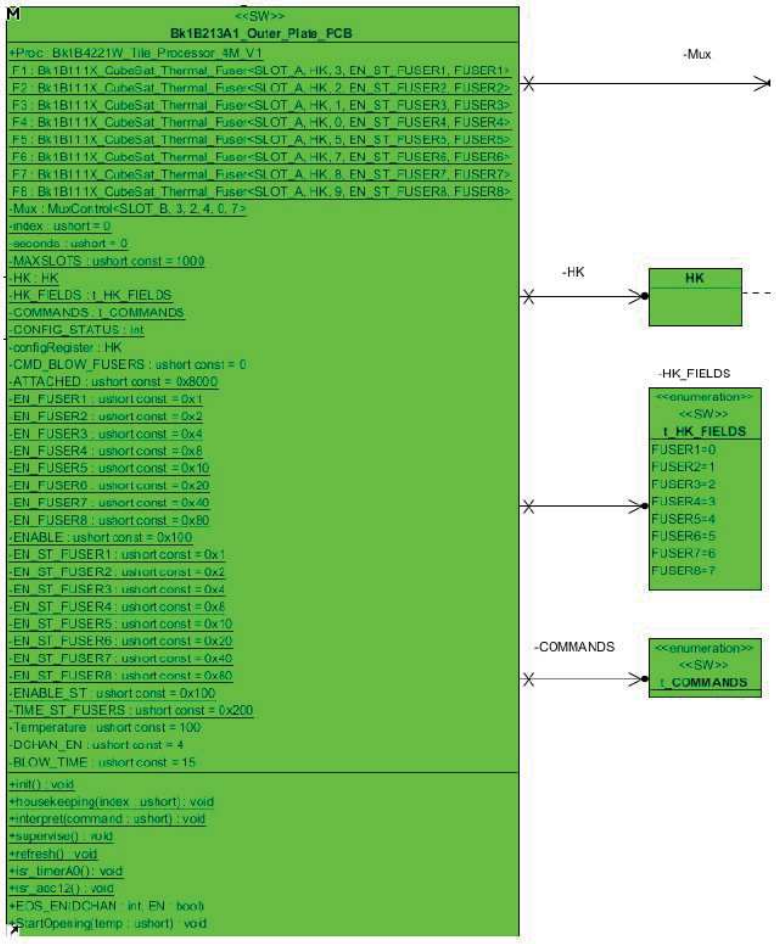


Figure 5.5. main class of the software

A software, must to have always a *main()*. Generally, the *main()* is instantiated in a specific class. This class is used to instantiate the main class of the software, in this case the Outer Plate main class. In the *main()* are launched the initialization of all devices and the main *cpu.proc* initialization class for the microcontroller. This latter is necessary, to initialize all the peripherals of the microcontroller and all the main configuration registers, as that used for example for the clock frequency setting of the microcontroller. In the main class Outer Plate, all the eight

instances of the fusers, the MUX class and the main variables are instantiated as attributes. A set of bits are declared for the correct pointing of the enable bits in the configuration register (*EN_FUSER1* to *EN_FUSER8*), and in the status register (*EN_ST_FUSER1* to *EN_ST_FUSER8*). Other bits are used for the global enable (*ENABLE* and *ENABLE_ST*), and a status bit to flag the end of the *TIMER* counting (*TIME_ST_FUSERS*). The configuration register, the status register and the housekeeping vector used, are all contained into an appropriate class called *Housekeeping*. This class is necessary because has been used for the storing of global *housekeeping*, status and configuration data for AraMiS compatible *AraModules*. For this reason the *Housekeeping* class is also instantiated into the attributes of the main class, by means of an intermediate class called *HK*. In the Outer Plate class are further contained the function for the timer interrupt management (*isr_timerA0()*), the function for the ADC interrupt management (*isr_adc12*), and a function for the global enable activation (*EOS_EN()*). Its housekeeping function is employed to collects the temperature data from the fusers instances. Finally it contains a *StartOpening()* function that is employed to manage the opening phase of the thermal fusers.

Chapter 6

Testing

The testing phase is really important to guarantee that the test board works properly. Two type of test could be made: in-circuit and functional. The first one checks if the board has any problem considering each component separately. The second one checks if the behaviour of the system. Both of test should stress the board considering the worst case. Many test points have been insert in the *Altium* sheets in order to do the functional test.

6.1 ICT: In-Circuit Test

The ICT is the first phase of the testing that it is possible to do in the PCB. It verifies: the integrity of the components, their correct orientation and if there are short circuits.
The parametric test, through the fixture, connects the testing machine to the Bk1B6711 Test Board. Firstly, no powered trials are performed, it means preliminary testing to verify the correct contact of the channels and to verify the correctness of the interconnections between the Test Board and instrumentation. Then the short circuit test should be made to prevent catastrophic events when the board is supplied. The test path continues with the verification of discrete components (resistances, capacities, inductances and diodes). Conduction and interdiction of the transistors should be test.
When the power supply is activated, the voltage generated on the pcb occurs, at which time the various test sequences that stimulate all parts of the circuit start, with control of each output.
If previous tests have a positive result, it passes on tests such as analogue functional tests, operational control and comparators, oscillator testing, linear voltage test and switching test.

The figure 6.1 shows an example of how the in-circuit test can be done using a

fixture to check the contact of the components.

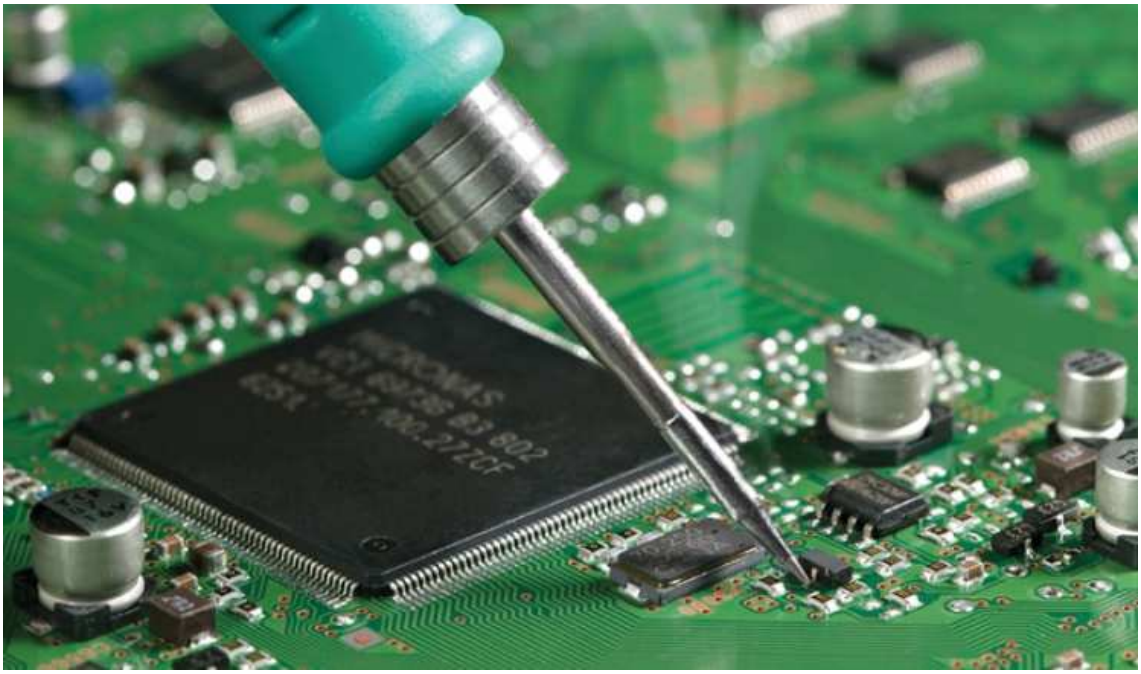


Figure 6.1. In-Circuit Test

6.2 Functional test

Functional testing is the only secure method to verify the good functioning of PCBs and complex electronic devices. The device should be tested through a series of simulations that recall and reproduce in the most realistic manner the standard operating conditions of the Bk1B6711 Test Board as well as the environmental conditions in which it will operate. For this purpose many test point have been inserted in the PCB in order to do the functional test.

The testes that should be done are:

- Check if the firmware has been uploaded.
- Check if the enable signal EN1 for the multiplexer and the thermal fusers works through the TP17.
- Check the correct address coming from the MODULE_B to the multiplexer, and verify if it corresponds to the correct V_{temp}. Then check if the output D of the multiplexer corresponds to that V_{temp}.

- Check the voltage level of the regulators varying the power supply PDB.
- Check if the power coming from the solar panels' structure is correct.

The third test should be done for all the thermal fusers, through TP5 to TP16.

Other testes that can be done to the Bk1B6711 Test Board are relative of the mechanical specification. First of all the CubeSate should be developed with the deploying mechanism and the solar panels' structure. Then mechanical vibration should be applied to verify the stability of the structure and the resistance of the wires that keep the solar panels' structure closed. The mechanical stress should be more than safety condition in order to measure the reliability to failure of the entire system. This test can be done considering also the case when one or more wires has been broken. Then is possible verify if the deploying mechanism allow to open the solar panels' structure and how much time is required to do that.

At this point the entire CubeSat can be mounted with four solar panels' structures and therefore four Test Board and repeat all the testes. The figure 6.2 describes before and after the deployment of the solar panels' structures.

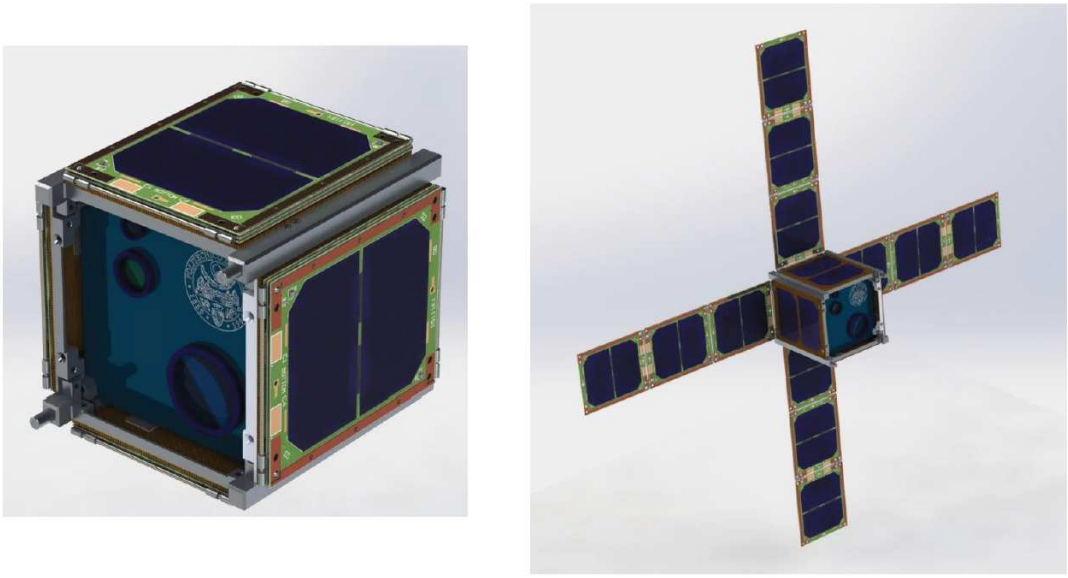


Figure 6.2. CubeSat before and after the deployment of four 1B111E

Chapter 7

Conclusion and Future works

The deploying mechanism and the Bk1B6711 Test Board discussed in the thesis is an innovative design of how the 1B111E solar panels' structure can be deployed. The test board has been developed with the lowest possible impact on weight and cost of its components. The P-POD compatibility has been respected considering the maximum thickness that the deployable solar panels' structure can be reach. All the electronic components have been selected to allow the operation of system within the safety limits. The deploying mechanism consists on a current that pass through two resistances. The parallel configuration is the best choice to have more reliability to failure than the series configuration. When the current pass through the resistances, heat is generated by Joule effect. The wire that keeps the solar panels's structure folded is detached thanks to the heat produced by the resistances. The wire must be soldered in the test board by the tin with low melting temperature and all the other components by a tin with a standard melting temperature. Follow this instruction the heat reached by the thermal fusers should melt only the tin used to solder the wire in the Bk1B6711 Test Board. If the heat exceeds the melting temperature of the tin where the wire is soldered, should be guaranteed that it does not melt the tin of the other components in order to do not fail the mission. For this reason a temperature control is really important.

The deploying mechanism composed by thermal fusers can be adapted for all the configurations of the CubeSat satellite. Their versatility allows the deploying mechanism to be positioned at every point in the board in order to be adapted on which deployable solar panels' structure has been used.

The Bk1B6711 Test Board is the test board used to verify the correct behaviour of the thermal fusers. Although some components have been added to test the deploying mechanism, the entire system can be used to manage other functions of the satellite like sensors, telescopes and other. Therefore the test board represents the components that must be used to guarantee the correct behaviour of the thermal fusers, but they can also be used for other applications. Obviously the subsystems

should respect the P-POD compatibility. The examples of the possible configurations of the CubeSat and of the deployable structure is reported in the figure 7.1.

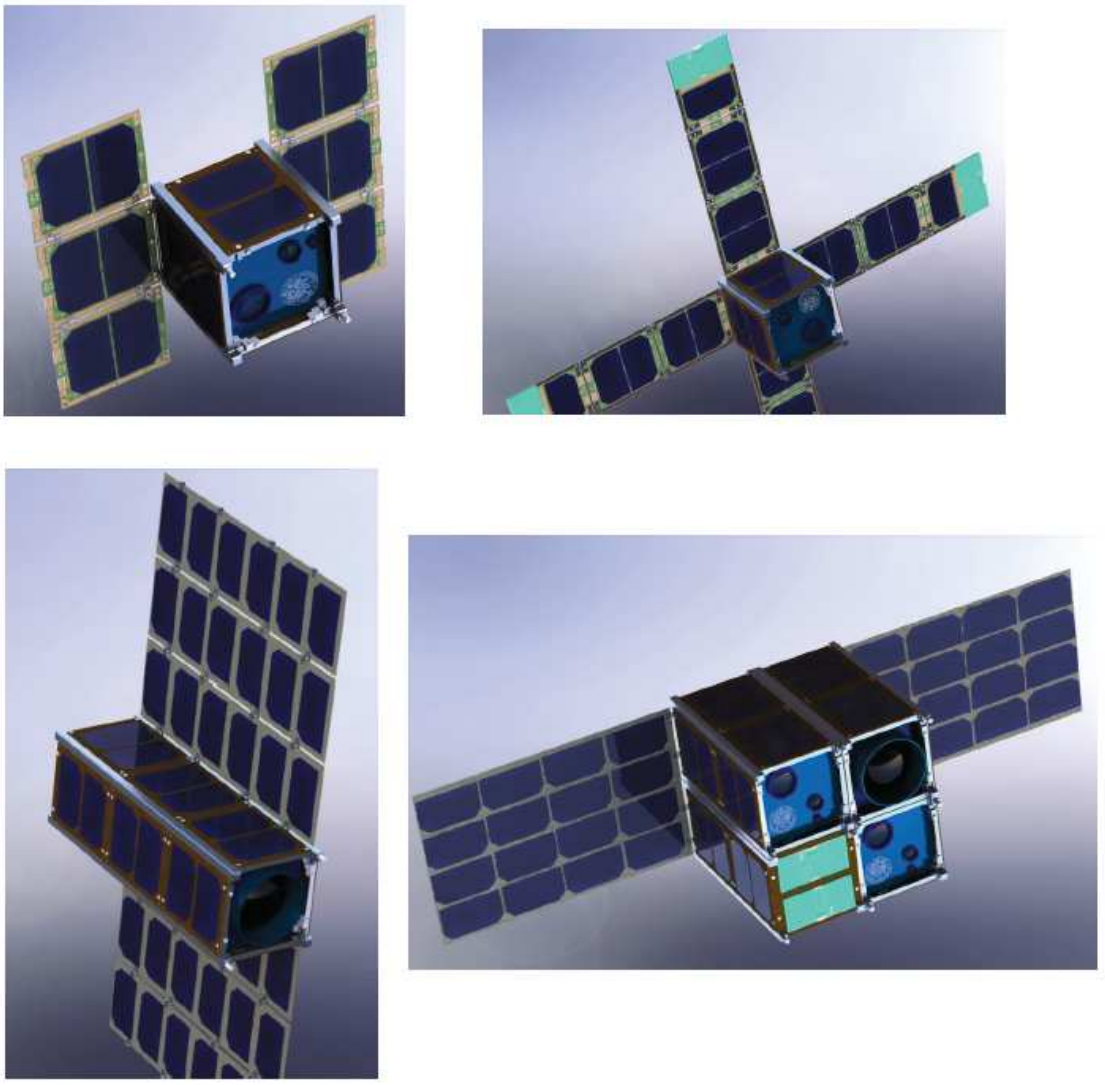
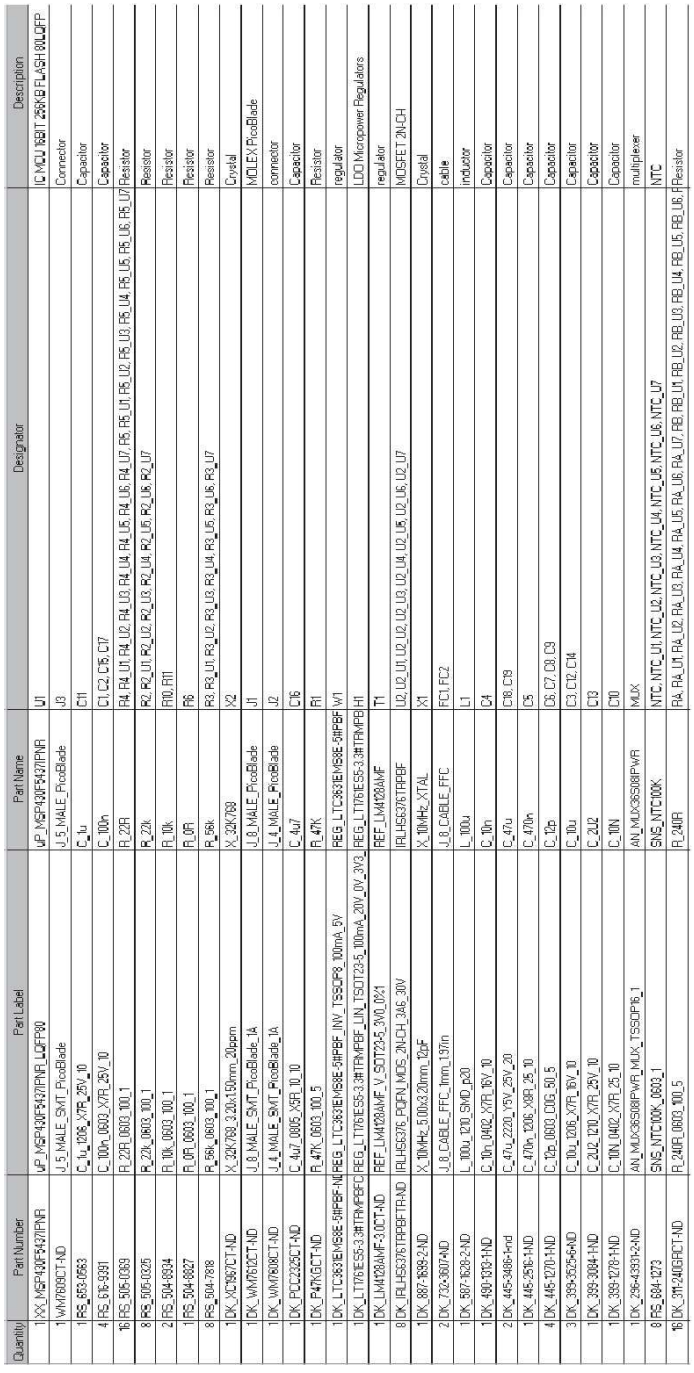


Figure 7.1. Example of different configurations of the CubeSat

The deploying mechanism is complete but just few things are missing to finish Bk1B6711 Test Board: the firmware should be developed and the testing phase is necessary to guarantee the correct behaviour of the test board.

7.1 BOM



Quantity	Part Number	Part Label	Part Name	Designator	Description
1	XX_MSP430F5437IPNR	uP_MSP430F5437IPNR_LQFP80	uP_MSP430F5437IPNR_LQFP80	U1	IC MCU 16BIT 256KB FLASH 80LQFP
1	WM7609CT-ND	J_5_MALE_SMT_PicoBlade	J_5_MALE_PicoBlade	J3	Connector
1	RS_663-0663	C_1u_X7R_25V_10	C_1u	C11	Capacitor
4	RS_616-9391	C_100n_0603_X7R_25V_10	C_100n	C1, C2, C16, C17	Capacitor
16	RS_505-0069	R_22R_0603_100_1	R_22R	R34, R4_U1, R4_U2, R4_U3, R4_U4, R4_U5, R4_U6, R4_U7, R5, R5_U1, R5_U2, R5_U3, R5_U4, R5_U5, R5_U6, R5_U7	Resistor
8	RS_505-0025	R_22k_0603_100_1	R_22k	R2, R2_U1, R2_U2, R2_U3, R2_U4, R2_U5, R2_U6, R2_U7	Resistor
2	RS_504-6934	R_10k_0603_100_1	R_10k	R10, R11	Resistor
1	RS_504-6827	R_0R_0603_100_1	R_0R	R6	Resistor
8	RS_504-7388	R_56k_0603_100_1	R_56k	R3, R3_U1, R3_U2, R3_U3, R3_U4, R3_U5, R3_U6, R3_U7	Resistor
1	DK_XC3967CT-ND	X_32K768_320x150mm_20ppm	X_32K768	X2	Crystal
1	DK_WM7612CT-ND	J_8_MALE_SMT_PicoBlade_1A	J_8_MALE_PicoBlade	J1	MOLEX PicoBlade
1	DK_WM7608CT-ND	J_4_MALE_SMT_PicoBlade_1A	J_4_MALE_PicoBlade	J2	connector
1	DK_PCC2325CT-ND	C_4u7_0805_X5R_10_10	C_4u7	C16	Capacitor
1	DK_P47KGCT-ND	R_47K_0603_100_5	R_47K	R1	Resistor
1	DK_LTC3631EMS8E-5#PBF-ND	REG_LTC3631EMS8E-5#PBF_INV_TSSOP8_100mA_5V	REG_LTC3631EMS8E-5#PBF	W1	regulator
1	DK_LT1761ES5-3.3#TRMPBF-ND	REG_LT1761ES5-3.3#TRMPBF_LIN_TSOT23-5_100mA_20V_0V_3V3_	REG_LT1761ES5-3.3#TRMPBF	H1	LDO Micropower Regulators
1	DK_LM4128AMF-3.0CT-ND	REF_LM4128AMF_V_SOT23-5_3V0_0%1	REF_LM4128AMF	T1	regulator
8	DK_IRLHS6376TRPBFTR-ND	IRLHS6376_PQFN_MOS_2N-CH_3A6_30V	IRLHS6376TRPBF	U2, U2_U1, U2_U2, U2_U3, U2_U4, U2_U5, U2_U6, U2_U7	MOSFET 2N-CH
1	DK_887-1638-2-ND	X_10MHz_5.00x3.20mm_12pF	X_10MHz_XTAL	X1	Crystal
2	DK_732-9607-ND	J_6_CABLE_FFC_1mm_137m	J_6_CABLE_FFC	FC1, FC2	cable
1	DK_587-1628-2-ND	L_100u_1210_SMD_p20	L_100u	L1	inductor
1	DK_490-1013-1-ND	C_10n_0402_X7R_16V_10	C_10n	C4	Capacitor
2	DK_445-3486-1-nd	C_47u_2220_Y5V_25V_20	C_47u	C18, C19	Capacitor
1	DK_445-2516-1-ND	C_470n_1206_X5R_25_10	C_470n	C5	Capacitor
4	DK_445-1270-1-ND	C_1p_0603_C0G_50_5	C_1p	C6, C7, C8, C9	Capacitor
3	DK_399-5025-6-ND	C_10u_1206_X7R_16V_10	C_10u	C3, C12, C14	Capacitor
1	DK_399-3084-1-ND	C_2U2_1210_X7R_25V_10	C_2U2	C13	Capacitor
1	DK_399-1278-1-ND	C_10N_0402_X7R_25_10	C_10N	C10	Capacitor
1	DK_296-43931-2-ND	AN_MUX36S08IPWR_MUX_TSSOP16_1	AN_MUX36S08IPWR	MUX	multiplexer
8	RS_684-1273	SNS_NTC100K_0603_1	SNS_NTC100K	NTC, NTC_U1, NTC_U2, NTC_U3, NTC_U4, NTC_U5, NTC_U6, NTC_U7	NTC
16	DK_311-240GRCT-ND	R_240R_0603_100_5	R_240R	R4, R4_U1, R4_U2, R4_U3, R4_U4, R4_U5, R4_U6, R4_U7, RB, RB_U1, RB_U2, RB_U3, RB_U4, RB_U5, RB_U6, R	Resistor

Figure 7.2. Bill Of Materials

7.2 Gerber

7.2.1 Top and Bottom layers

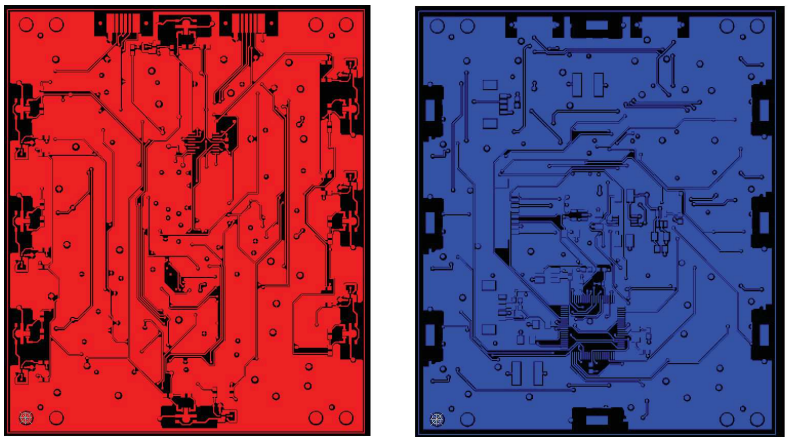


Figure 7.3. Top and bottom layers

7.2.2 PDB and GND layers

The PDB and GND layers are represented in negative way.

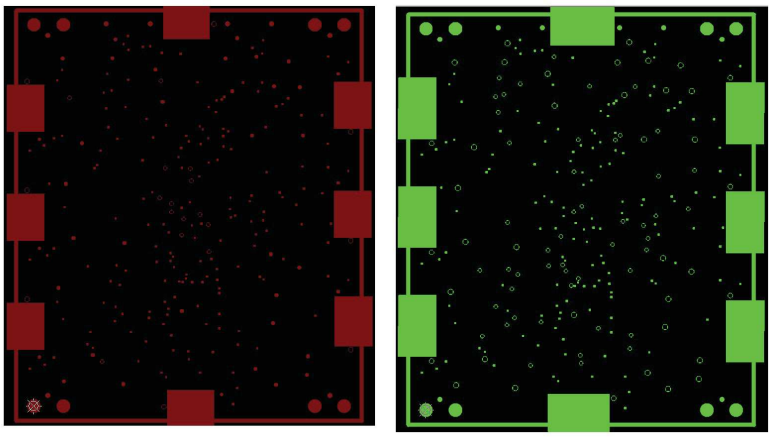


Figure 7.4. PDB and GND layers

7.3 Altium sheets

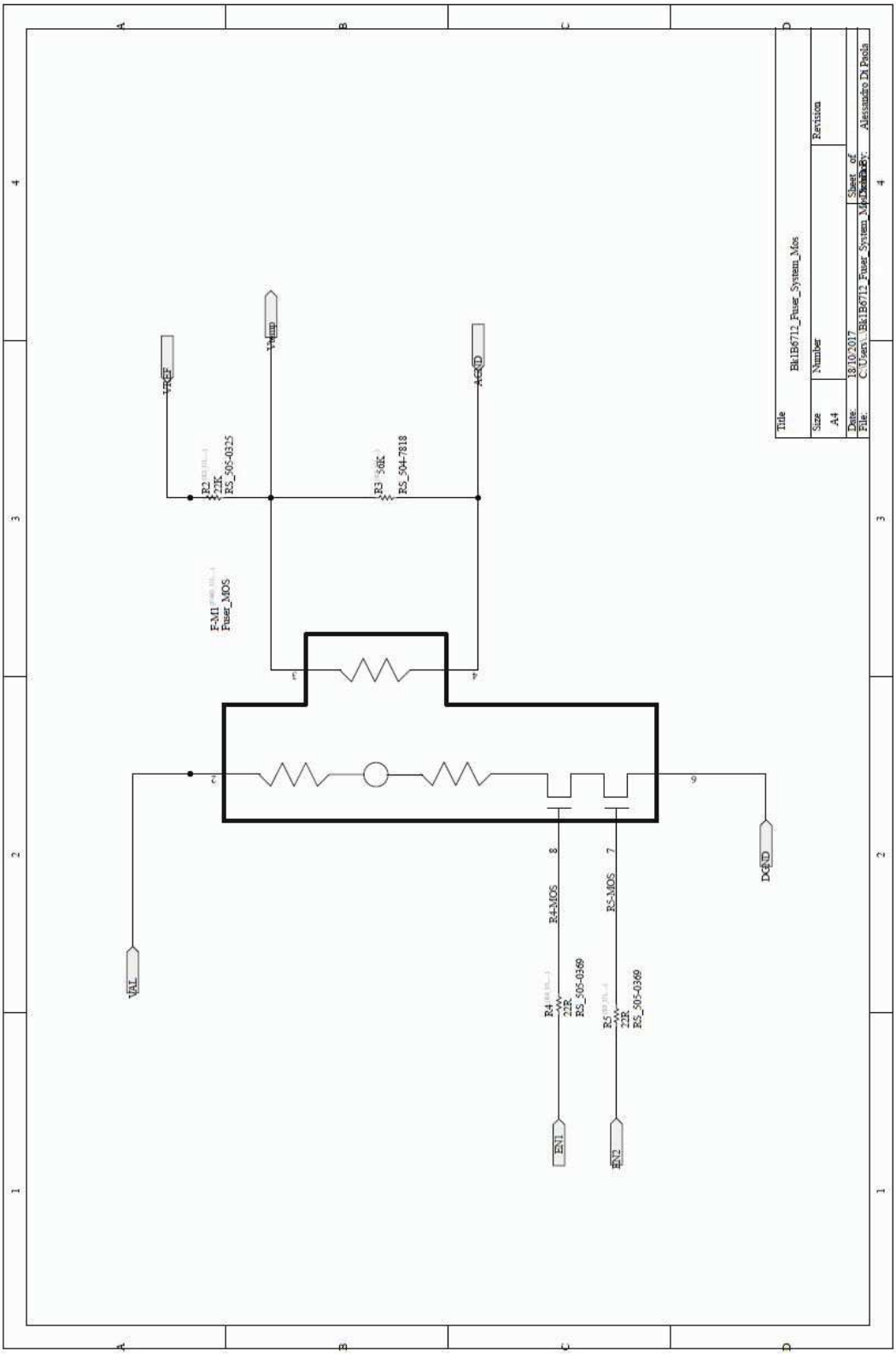


Figure 7.5. Bk1B6712_Fuser_System_Mos

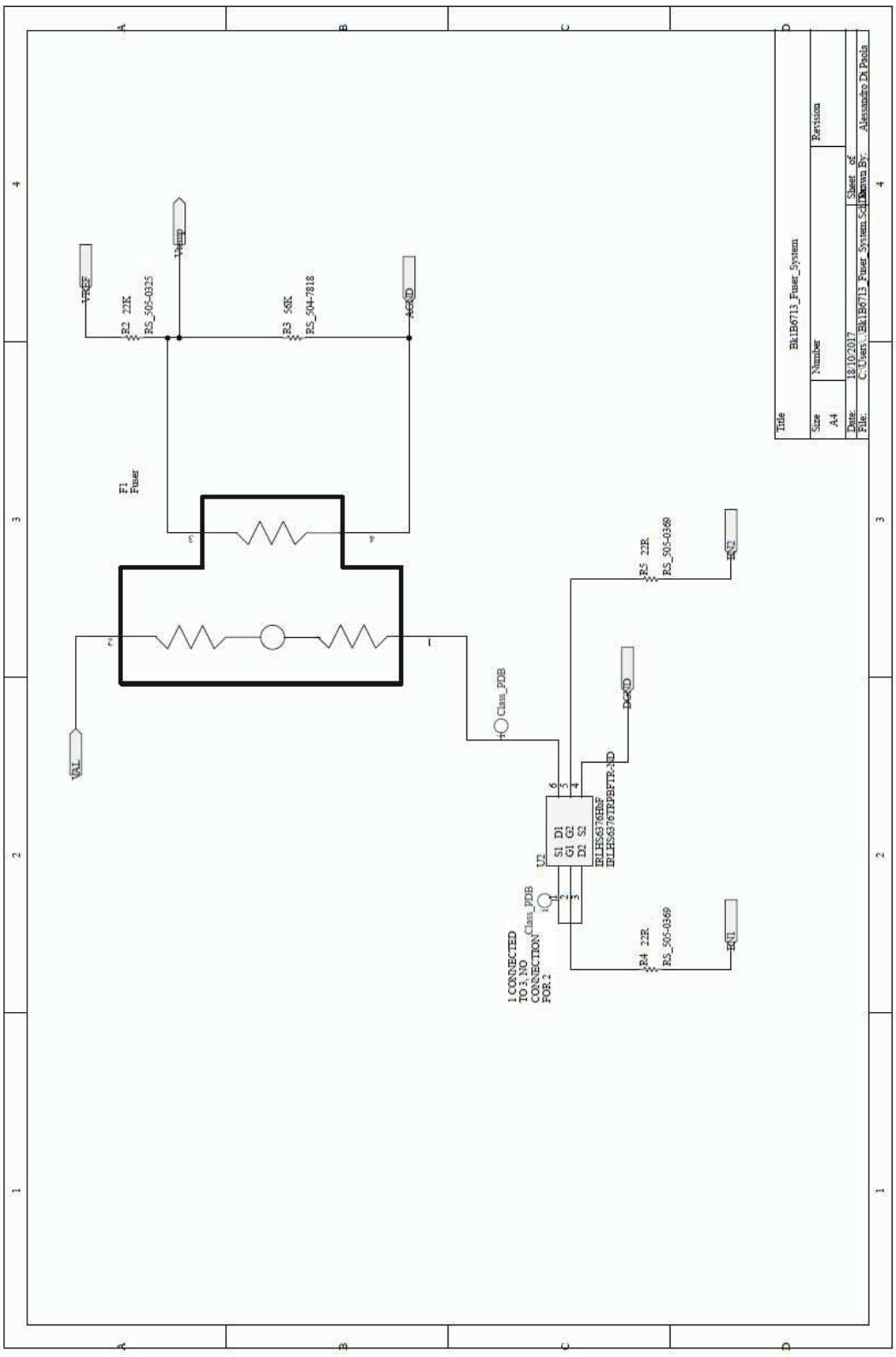


Figure 7.6. Bk1B6713_Fuser_System

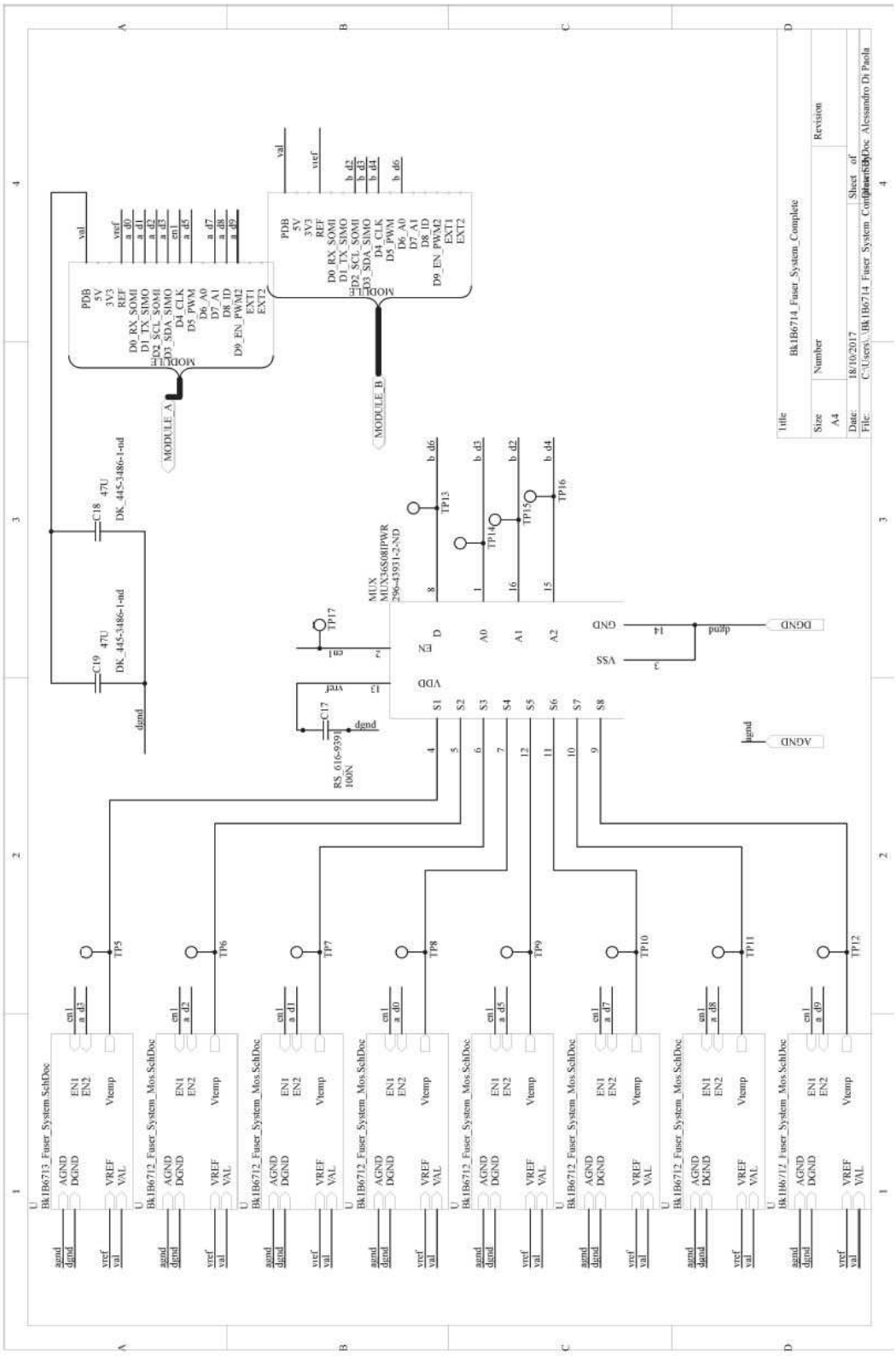


Figure 7.7. Bk1B6714_Fuser_System_Complete

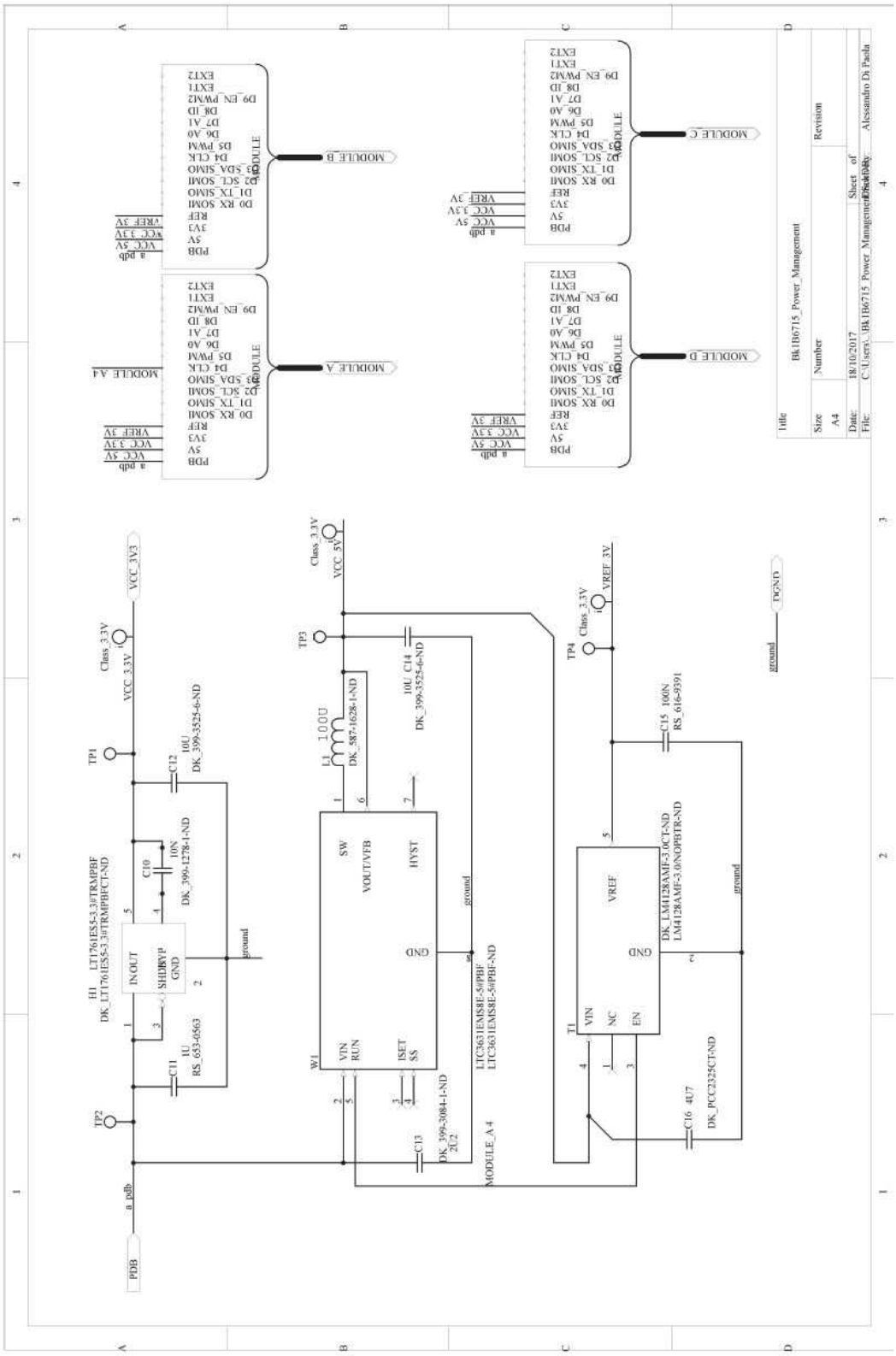


Figure 7.8. Bk1B6715_Power_Management

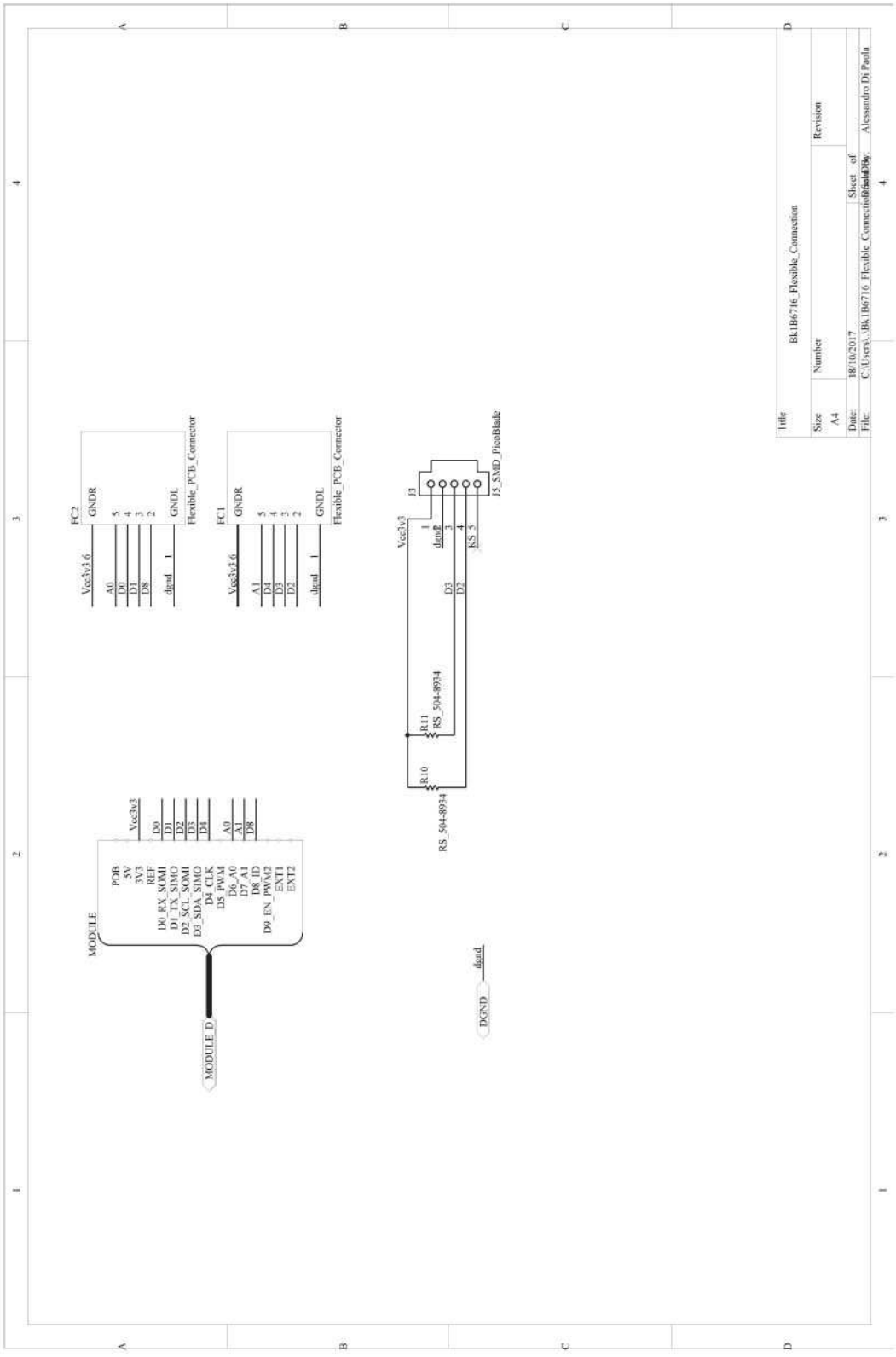


Figure 7.9. Bk1B6716_Flexible_Connection

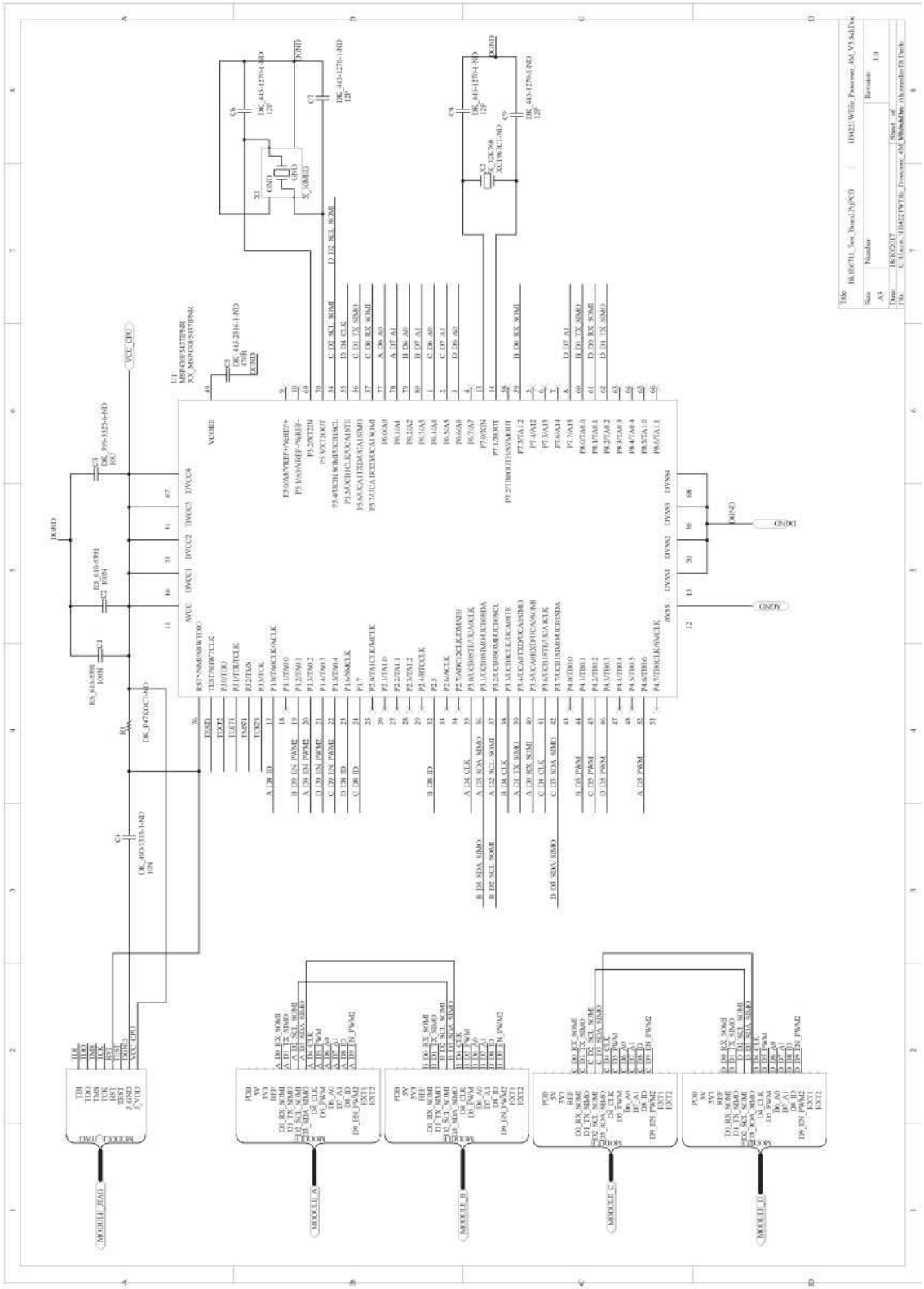


Figure 7.10. 1B4221WTile_Processor_4M_V3

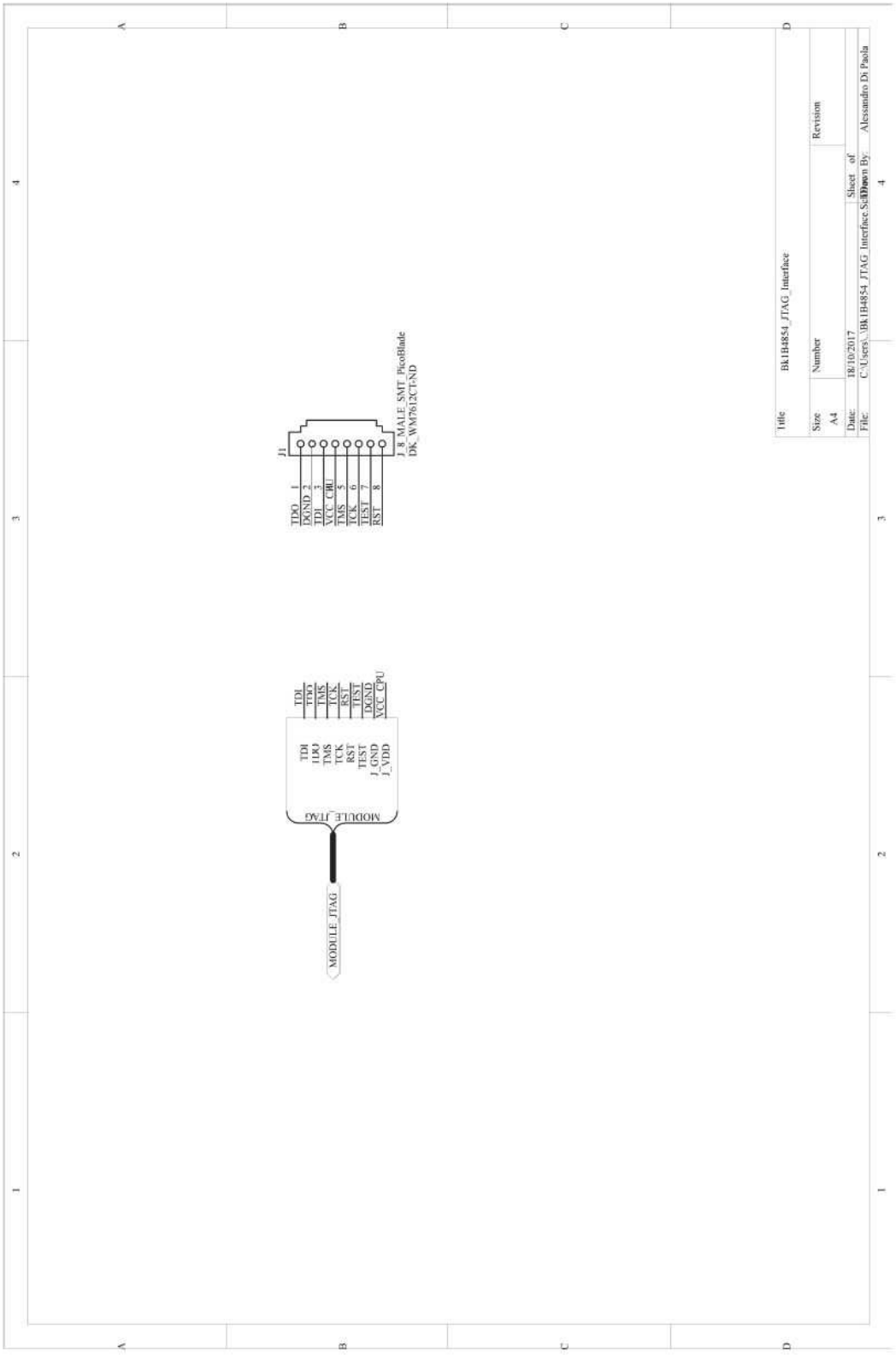


Figure 7.11. Bk1B4854_JTAG_Interface

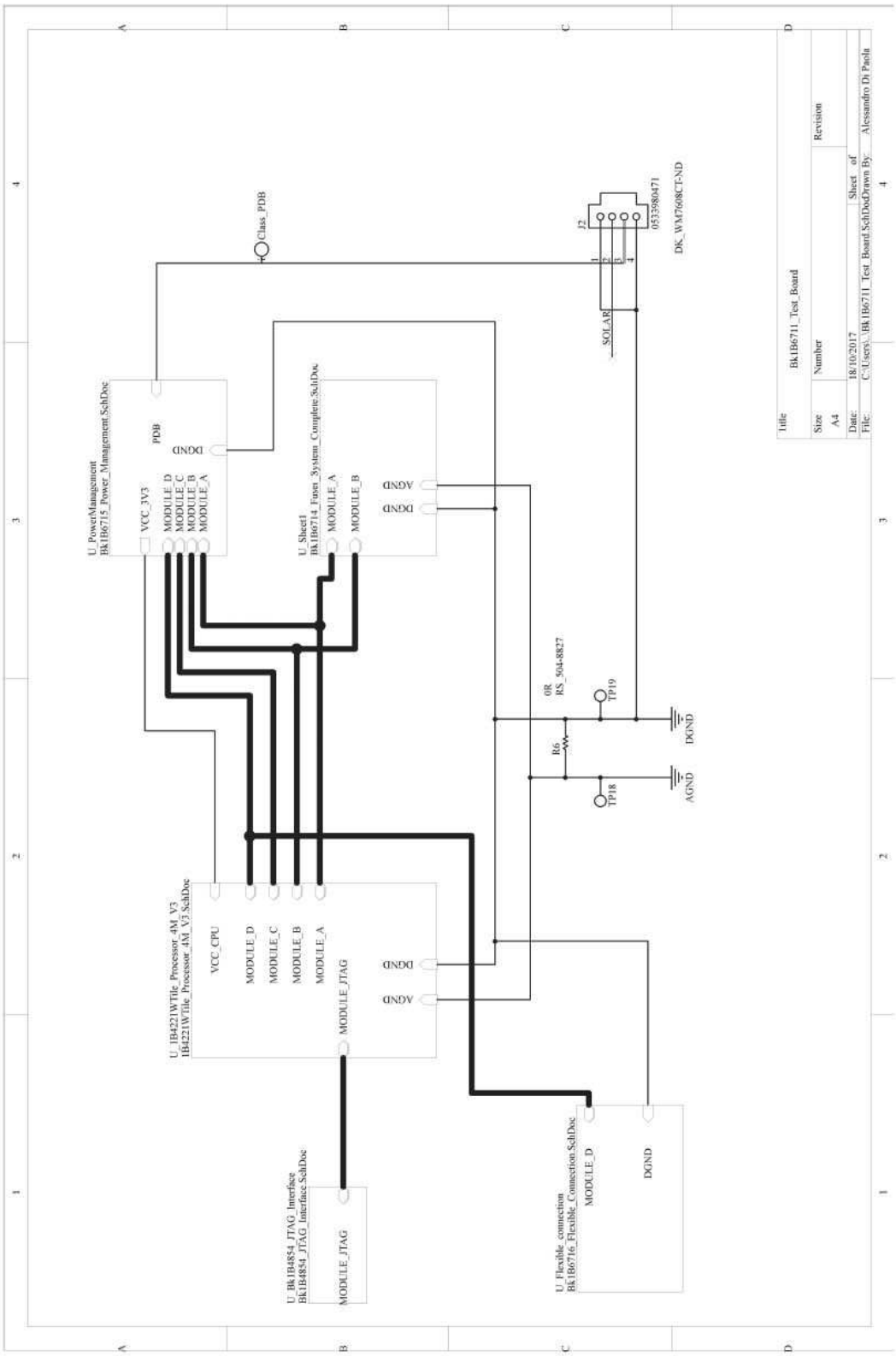


Figure 7.12. Bk1B6711_Test_Board

Bibliography

[1] M. B. D. D. C. A. H. C. P. D. R. C. S. S. S. M. T. N. U. A. V. A. C. M. B. L. S. L.M. Reyneri, *ARAMIS an alternative approach to CubeSats for more demanding satellite applications*, Würzburg, 2009.

[2] C. Space, *Deployable CubeSat Solar Panels*, [Online]. Available: http://www.clyde-space.com/cubesat_shop/solar_panels_-_deployable.

[3] A. Ali, *«1B111B Solar Panel» in Power Management, Attitude Determination and Control Systems of Small Satellites*, Turin, 2014.

[4] G. Bruni, *Development and testing of innovative solar panels with deployable structure for ARAMIS satellite platform*, Turin, 2016.

[5] Texas Instruments, *16-bit Microcontrollers - MCU 16Bit Ultra-Low-Pwr Microcontroller*, [Online]. Available: http://www.ti.com/lit/ds/symlink/msp430f5437.pdf.

[6] Molex LLC, *CONN HEADER 5POS 1.25MM VERT SMD*, [Online]. Available: http://www.molex.com/pdm_docs/sd/533980571_sd.pdf.

[7] Molex LLC, *CONN HEADER 8POS 1.25MM VERT SMD*, [Online]. Available: http://www.molex.com/pdm_docs/sd/533980871_sd.pdf.

[8] Molex LLC, *CONN HEADER 4POS 1.25MM VERT SMD*, [Online]. Available: http://www.molex.com/pdm_docs/sd/533980471_sd.pdf.

[9] Murata, *Condensatore ceramico multistrato (MLCC) Murata GRM* $1\mu F, \pm 10\%, 25Vcc, SMD$, [Online]. Available: http://docs-europe.electrocomponents.com/webdocs/1423/0900766b81423c9e.pdf.

[10] Phycomp, *Condensatore ceramico multistrato (MLCC) Phycomp Standard* $100nF, \pm 10\%, 25Vcc, SMD$, [Online]. Available: http://docs-europe.electrocomponents.com/webdocs/0c10/0900766b80c10176.pdf.

[11] Yageo, *Resistore SMD a film spesso Yageo* $22\Omega \pm 1\%, 0{,}1W, 0603, serieRC$, [Online]. Available: http://docs-europe.electrocomponents.com/webdocs/0c66/0900766b80c66297.pdf.

[12] Yageo, *Resistore SMD a film spesso Yageo* $22k\Omega? \pm 1\%, 0{,}1W, 0603, serieRC$, [Online]. Available: http://docs-europe.electrocomponents.com/webdocs/0c66/0900766b80c66297.pdf.

[13] Yageo, *Resistore SMD a film spesso Yageo* $10k\Omega \pm 1\%, 0{,}1W, 0603, serieRC$, [Online]. Available: http://docs-europe.electrocomponents.com/webdocs/0f96/0900766b80f96399.pdf.

[14] Yageo, *Resistore SMD a film spesso Yageo* 0Ω*, 0,1W, 0603, serie RC*, [Online]. Available: http://docs-europe.electrocomponents.com/webdocs/0c66/0900766b80c66297.pdf.

[15] Yageo, *Resistore SMD a film spesso Yageo* $56k\Omega \pm 1\%, 0{,}1W, 0603, serieRC$, [Online]. Available: http://docs-europe.electrocomponents.com/webdocs/0c66/0900766b80c66297.pdf.

[16] ECS Inc., *CRYSTAL 32.7680KHZ 12.5PF SMD*, [Online]. Available: http://www.ecsxtal.com/store/pdf/ECX_34S.pdf.

[17] Panasonic Electronic Components, *CAP CER 4.7UF 10V X5R 0805*, [Online]. Available: https://media.digikey.com/pdf/Data%20Sheets/Panasonic%20Capacitors%20PDFs/ECJ(HighCapacitance).pdf.

[18] Panasonic Electronic Components, *RES SMD 47K OHM 5% 1/10W 0603*, [Online]. Available: https://industrial.panasonic.com/cdbs/www-data/pdf/RDA0000/AOA0000C301.pdf.

[19] Linear Technology, *IC REG BUCK INV 5V 0.1A 8MSOP*, [Online]. Available: http://cds.linear.com/docs/en/datasheet/3631fe.pdf.

[20] Linear Technology, *IC REG LIN 3.3V 100MA TSOT23-5*, [Online]. Available: http://cds.linear.com/docs/en/datasheet/1761sff.pdf.

[21] Texas Instruments, *IC VREF SERIES 3V SOT23-5*, [Online]. Available: https://media.digikey.com/pdf/Data%20Sheets/National%20Semiconductor%20PDFs/LM4128.pdf.

[22] Infineon Technologies, *MOSFET 2N-CH 30V 3.6A PQFN*, [Online]. Available: https://www.infineon.com/dgdl/irlhs6376pbf.pdf?fileId=5546d462533600a401535663bef425af.

[23] TXC CORPORATION, *CRYSTAL 10.0000MHZ 12PF SMD*, [Online]. Available: http://www.txccorp.com/download/products/automotive_crystals_oscillators/2015TXC_%20AB_38.pdf.

[24] Wurth Electronics Inc., *CABLE FFC 8POS 1.00MM 1.97"*, [Online]. Available: http://katalog.we-online.de/em/datasheet/6866xxxxx001.pdf.

[25] Taiyo Yuden, *FIXED IND 100UH 340MA 1.82 OHM*, [Online]. Available: https://www.yuden.co.jp/productdata/catalog/en/wound02_e.pdf.

[26] Murata Electronics North America, *CAP CER 10000PF 16V X7R 0402*, [Online]. Available: http://search.murata.co.jp/Ceramy/image/img/A01X/G101/ENG/GRM155R71C103KA01-01.pdf.

[27] TDK Corporation, *CAP CER 47UF 25V Y5V 2220*, [Online]. Available: https://media.digikey.com/pdf/Data%20Sheets/TDK%20PDFs/C_Series_GeneralAppl_B11.pdf.

[28] TDK Corporation, *CAP CER 0.47UF 25V X8R 1206*, [Online]. Available: https://product.tdk.com/info/en/catalog/spec/mlccspec_commercial_hightemp_en.pdf.

[29] TDK Corporation, *CAP CER 12PF 50V C0G 0603*, [Online]. Available: https://product.tdk.com/info/en/catalog/spec/mlccspec_commercial_general_midvoltage_en.pdf.

[30] KEMET, *CAP CER 10UF 16V X7R 1206*, [Online]. Available: https://content.kemet.com/datasheets/KEM_C1002_X7R_SMD.pdf.

[31] KEMET, *CAP CER 2.2UF 25V X7R 1210*, [Online]. Available: https://content.kemet.com/datasheets/KEM_C1002_X7R_SMD.pdf.

[32] KEMET, *CAP CER 10000PF 25V X7R 0402*, [Online]. Available: https://content.kemet.com/datasheets/KEM_C1002_X7R_SMD.pdf.

[33] Texas Instruments, *IC MUX 8:1 LOCAP CMOS 16TSSOP*, [Online]. Available: http://www.ti.com/lit/ds/symlink/mux36d04.pdf.

[34] Vishay, *Termistore Vishay NTCS0603E3104FXT,* $100k\Omega \pm 1\%$*, 8s, package 0603*, [Online]. Available: http://docs-europe.electrocomponents.com/webdocs/0d9a/0900766b80d9a0b4.pdf.

[35] Yageo, *RES SMD 240 OHM 5% 1/10W 0603*, [Online]. Available: http://www.yageo.com/documents/recent/PYu-RC_Group_51_RoHS_L_7.pdf.

[36] Altium Designer, *Manual*, [Online]. Available: http://www.altium.com/documentation/17.0/display/ADES/Altium+Designer+Documentation.

[37] SolidWorks, *Manual*, [Online]. Available: http://www.solidworkstutorials.com/.

[38] Visual Paradigm, *Manual*, [Online]. Available: https://www.visual-paradigm.com/support/documents/vpuserguide.jsp.