POLITECNICO DI TORINO

Facoltà di Ingegneria dell'Informazione
Corso di laurea in Ingegneria delle Elettronica

Monografia

Progetto e realizzazione
Kill-switch sistemi

Relatori:
prof. Claudio Sansoè
prof. Leonardo Reyneri

Candidato:

Nome: Yunali Sun
Matricola: S147522

Luglio 2010

Monografia

Project:Kill-Switch

Abstract

This work aims at developing a Kill-Switch compatible with the ARAMIS architecture for modular satellites. The Kill-Switch is responsible to keep the satellite in stand-by during storage and launch and to activate the satellite as soon as it is deployed in orbit. The system shall consume least possible power and handle testing, integration, pre-launch and launch phases. The system will be partially described in UML. Activity will terminate with the design (including PCB and the Software), positive testing and documentation ready.

1.Introduction:

1) Describe how does the kill-switch system work
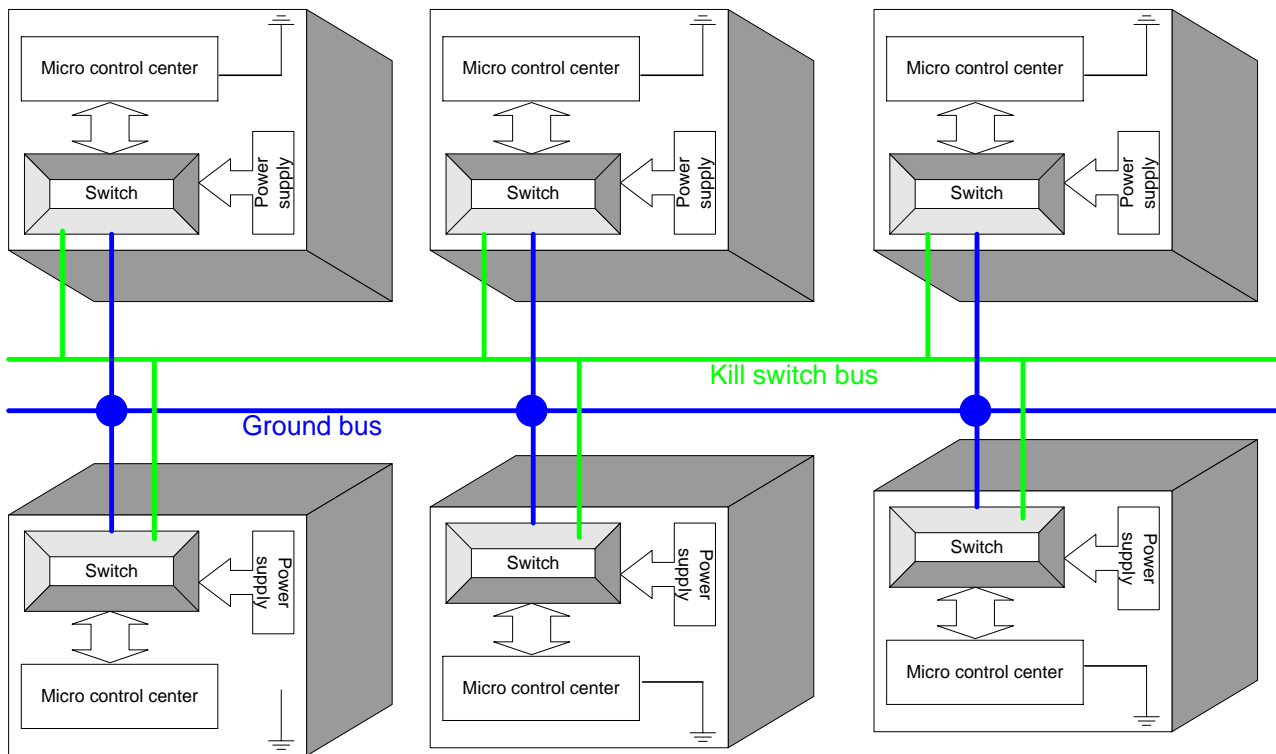
We assume that there are six surfaces on the satellite structure, each of them is installed a switch module. These six kill-switch modules are identical, but only one surface is effective to determine whether the satellite is docked in the expected location or not, the correct docking state of the satellite could be transferred into the kill-switch bus ,and all modules can be simultaneously read the state sent by the kill-switch bus, thus to start the micro-controller.MSP , carrying out control of the satellite. ARAMIS architecture developing system is applying MSP as a microcontroller for kill-switch module ,which could read the signal from kill-switch bus and make decision that whether the satellite should work on docked state.

2) The basic requirements for the kill-switch block design

For designing the kill- switch block, it requests the lowest power consuming, two separate ground and identical kill- switch block for industrial needs. The circuit could send the docking signal and also be able to read the signal coming from the kill-switch bus.

3) How to solve the general problem

a) For low power consuming, first, we could apply pulse trigger , the idea is to make the circuit work only during the pulse period, hanging when there is no pulse, so it will not use the power continually and could save a lot energy. With the ARAMIS architecture for modular satellites, we could use MSP(microcontroller) from the ARAMIS component library component to generate the TX signal,which also can accept the RX signal. It can reduce the use of components, reducing circuit complexity, and the ability to use ultra-low power consumption characteristics of MSP to meet the design requirements.

b) As for the ground problem, we could choose pulse transformer, which could have separated ground according to the designer. We have a Ground bus for physical ground, and each kill switch block has a digital ground.

c) For industrial needs we have to design identical kill-switch system blocks, which should be able to not only transfer the docking state signal to the kill-switch bus, but also receive the signal from the kill-switch bus.

2.Designing

2.1. Specification

According to the general system requirements and design ideas, we give the following Specification

Signal for TX: square wave PER: 50uS, PW: 5uS, offset: 0v, AMP: 3v;
Signal for RX: square wave PW>2uS, AMP: 3.3v

DC voltage supply: 3.3v (according to the driven port level
requirments from the datesheet of MSP)

2. 2. Design process Category Overview

The course of our work is divided into four steps, namely
1) First stage: laboratory simulation stage;
2) Second stage: experimental test board;
3) Third stage: pcb board is to produce a performance version of the test circuit;
4) The last stage: the application of MSP and PCB in combination, to verify the model is able to meet all the requirements.

2. 3. Concrete analysis of each process

2.3.1 First stage: laboratory simulation stage;
We define a square wave function for TX and apply the 3.3v DC as the power supply, kill-swtich bus signal,TX and RX are needed to be measured in the simulation.
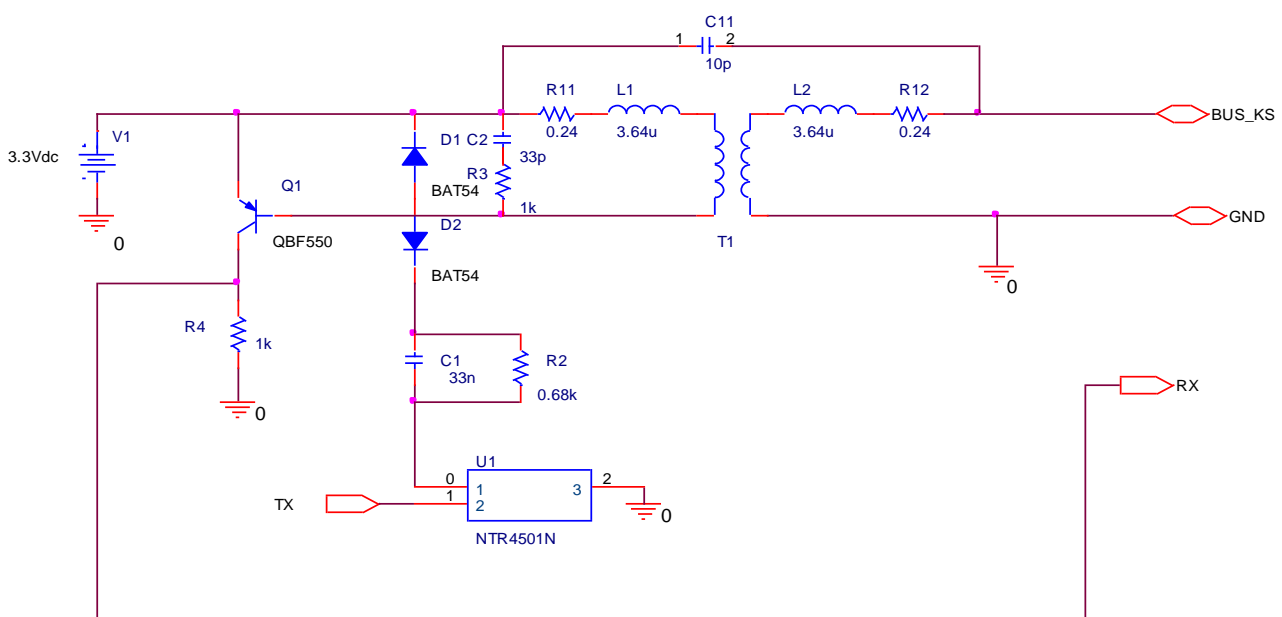
a) Schema of kill-switch block1


Figure1: kill-switch block1

As shown from the figure1, we suppose that the input square wave driven by the mechanical switch as TX (pulse trigger), RX is the receiver, which could receive the signal from the BUS_KS (kill-switch bus), the global ground is called GND, and U1 is a MOSFET, Played the role of an electronic switch, souce of Mosfet connect to the groud.

T1 is a pulse transformer that is optimised for transmitting rectangular electrical pulses (that is, pulses with fast rise and fall times and a relatively constant amplitude). To minimise distortion of the pulse shape, a pulse transformer needs to have low values of leakage inductance and distributed capacitance, and a high open-circuit inductance. In power-type pulse transformers, a low coupling capacitance (between the primary and secondary) is important to protect the circuitry on the primary side from high-powered transients created by the load. For the same reason, high insulation resistance and high breakdown voltage are required. Pulse transformers by definition have a duty cycle of less than 0.5, whatever energy stored in the coil during the pulse must be "damped" out before the pulse is fired again.we choose **Tr_786153MC** as our pulse transformer and the leakage inductance and distributed capacitance have already been included in that component.

NTR4501 is a MOS played the role of the electronic switch,and also could protect the circuit. When there is a TX signal , MOS will work and transmit the signal to the transformer.

In RC TIME CONSTANT: The time required to charge a capacitor to 63 percent (actually 63.2 percent) of full charge or to discharge it to 37 percent (actually 36.8 percent) of its initial voltage is known as the TIME CONSTANT (TC) of the circuit. The charge and discharge curves of a capacitor are shown in figure.

RC time constant figure
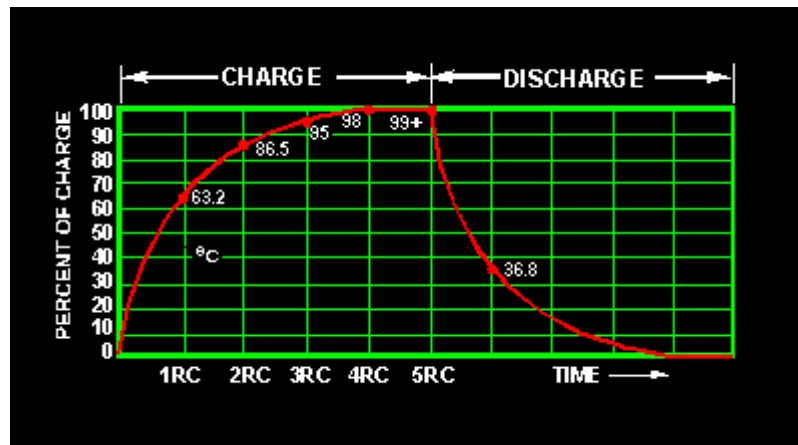
The value of the time constant in seconds is equal to the product of the circuit resistance in ohms and the circuit capacitance in farads. The value of one time constant is expressed mathematically as $t = RC$. We will discuss the design of RC time in the second stage.

b) Simulation with pspice

We use software simulation model to test the kill-switch circuit, as shown in the figure2, we test kill-switch bus signals, TX signals and RX signals of any two modules,at this moment , we could temporarily igore the seprated ground problem among these blocks.

Figure 2: Test simulation model

** Profile: "TOP_LEVEL-WORK1" [r:\tesi\tesi sun kill switch\simulations\test_transformer-TOP_LEVEL-WORK1.sim]
Date/Time run: 05/31/10 11:52:40   Temperature: 27.0
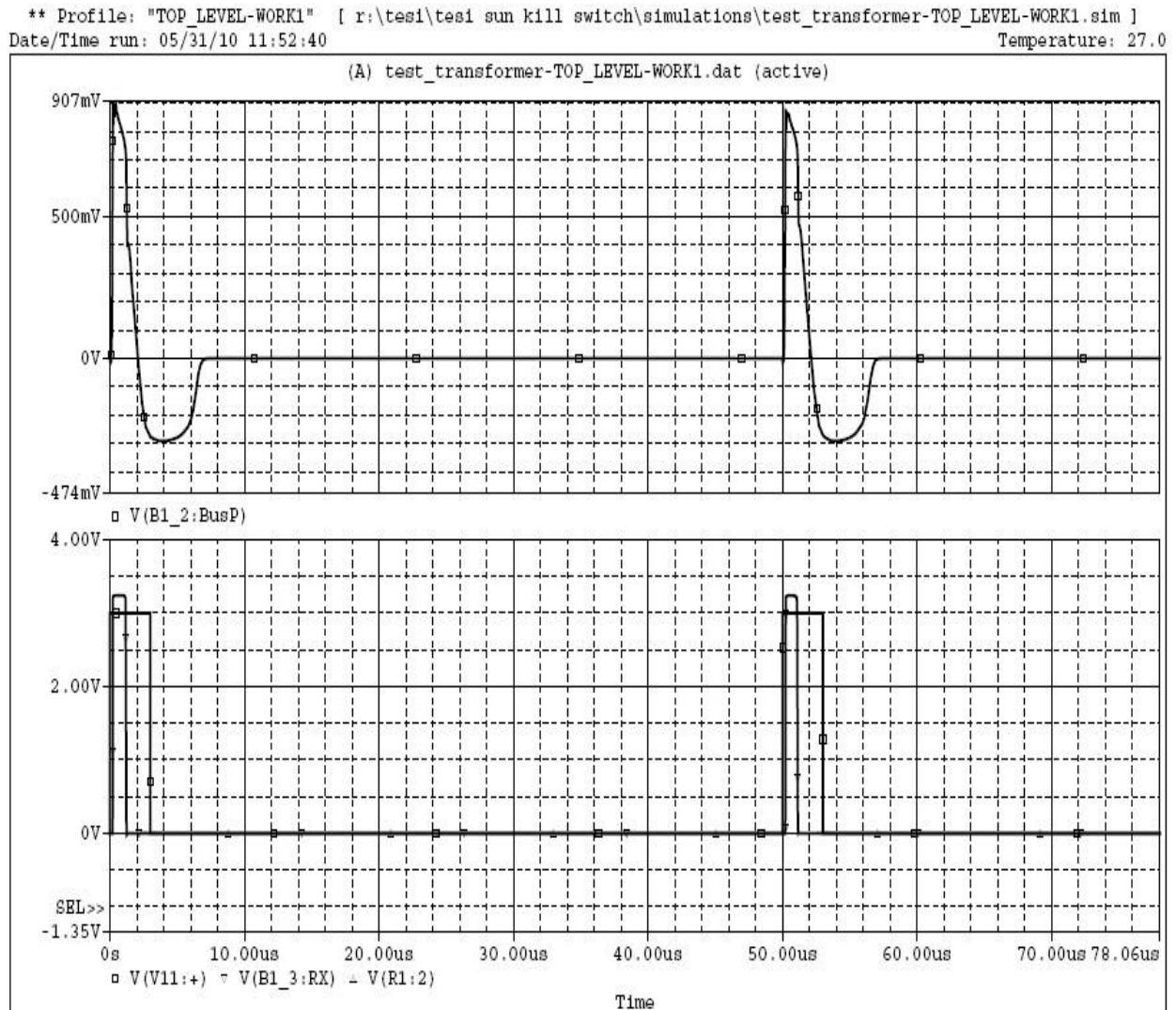
(A) test_transformer-TOP_LEVEL-WORK1.dat (active)

Figure3: simulation result of test modulo

The first row shows the kill-switch bus signal, the second row shows input signal TX(3v),and the signal RX(3.3v)

Signal for TX: square wave PER: 50uS , PW: 5uS, offset: 0v, AMP: 3v;
Signal for RX: square wave PW=2uS, AMP: 3.3v, offset: 0v, AMP: 3.3v;

2.3.2 Second stage: experimental test board

IN this stage, we could apply a funcion generator to generate a square wave function for TX and apply the 3.3v DC as the power supply, kill-swtich bus signal,TX and RX are needed to be measured in the simulation test board.

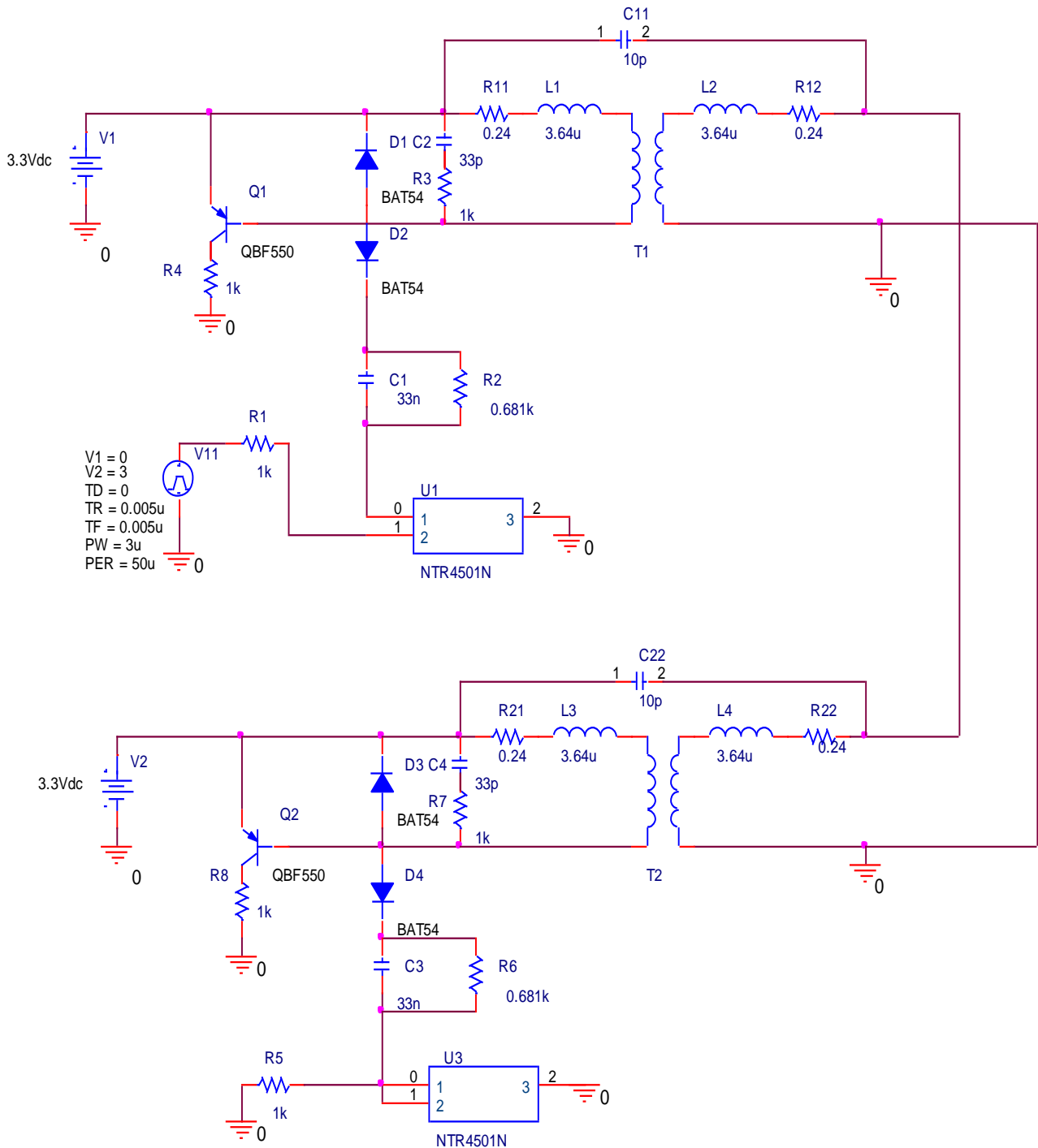## a) Schema of kill-switch circuit for test board

Figure4: Schema of kill-switch circuit for test board

In this test board , we apply only two kill-switch block , the first one will give a driving signal TX, and the second one will read the RX signal coming from the kill-switch bus signal.

b) The components we use

| PARTITION	PART NUM.	PART NAME	PACKAGE	VALUE	NUM
Passives	RS_504_8221	R680R		680R	2
Passives	RS_504_8928	R1K		1K	6
Passives	RS_545_4115	C33p		33p	2
Passives	RS_652_0134	C33n		33n	2
Diodes	RS_670-8785	BAT54A	D_Schottky_200mA_30V		2
MOS	DK_NTR4501NT1GOSCT-ND	NTR4501	Q_NTR4501_SOT23_3A2_20		2
BJT	RS_484-2381	Q_BF550	Q_BF550_SOT23-3_BJT_PNP		2
TRANSFORMER	ME_580-786153MC	Tr_786153MC	TRANSFORMER		2

c) Physical board of kill-switch circuit
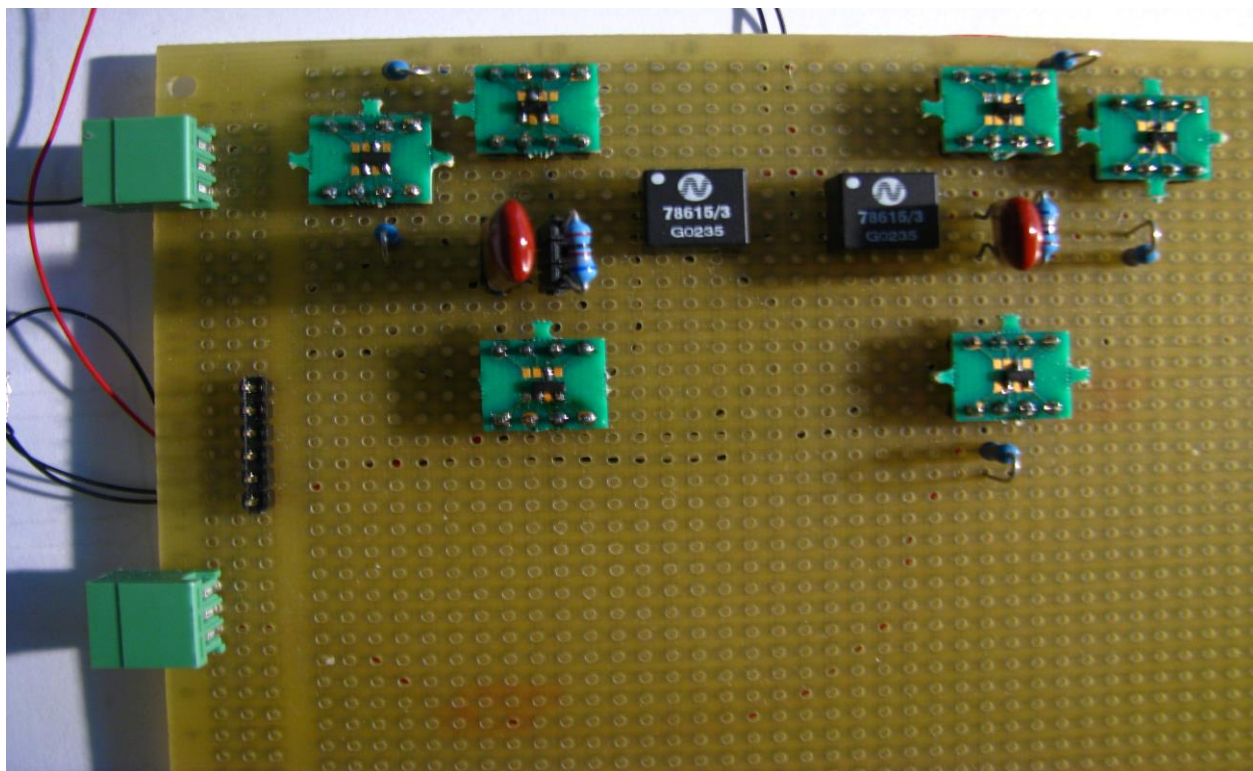
Figure5: kill-switch circuit for test board

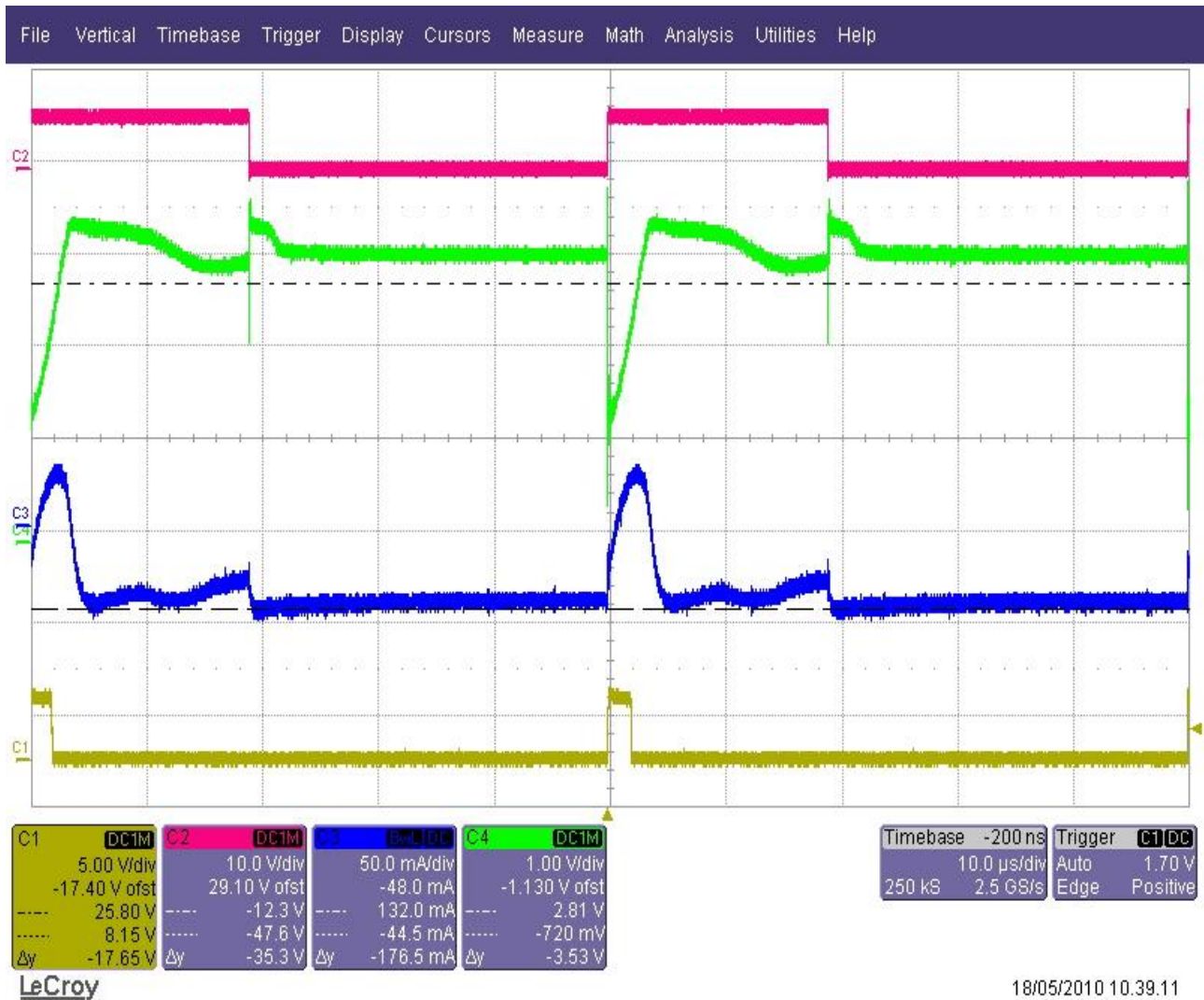c) Measurement of kill-switch circuit for test board with oscilloscope

Figure6: Oscilloscope demo image

This image shows the signal of C1, C2, C3, C4

C2: TX signal : square wave PER: 50uS , PW: 5uS, offset: 0v, AMP: 3v;
C4: Kill-switch signal: PER: 52uS
C3: Test point at the gate of BJT: PER: 51.3uS , gate current is less than 4omA
C1: RX signal (test point at the second block): square wave PER: 50uS, PW: 2uS, AMP: 3.3v;

At this test board, the grounds of the two blocks are in common, the Ground-bus at the secondary part of transformer are separated from the primary ground, from the Oscilloscope demo image we could see that this circuit basically meet the design requirements, disturbance is very small, and can reduce the msp working time to lower power consumption .

In an RC circuit, the value of the time constant (in seconds) is equal to the product of the circuit resistance (in ohms) and the circuit capacitance (in farads), i.e. $\tau = R \times C$. It is the time required to charge the capacitor, through the resistor, to 63.2 ($\approx$ 63) percent of full charge; or to discharge it to 36.8 ($\approx$ 37) percent of its initial voltage. These values are derived from the mathematical constant e, in the test board, we apply different value of the capacitance(33n ,47n , 68n,100n), the circuit could only work with the value less than 68n, so we could choose the capacitance with 33n or 47n.
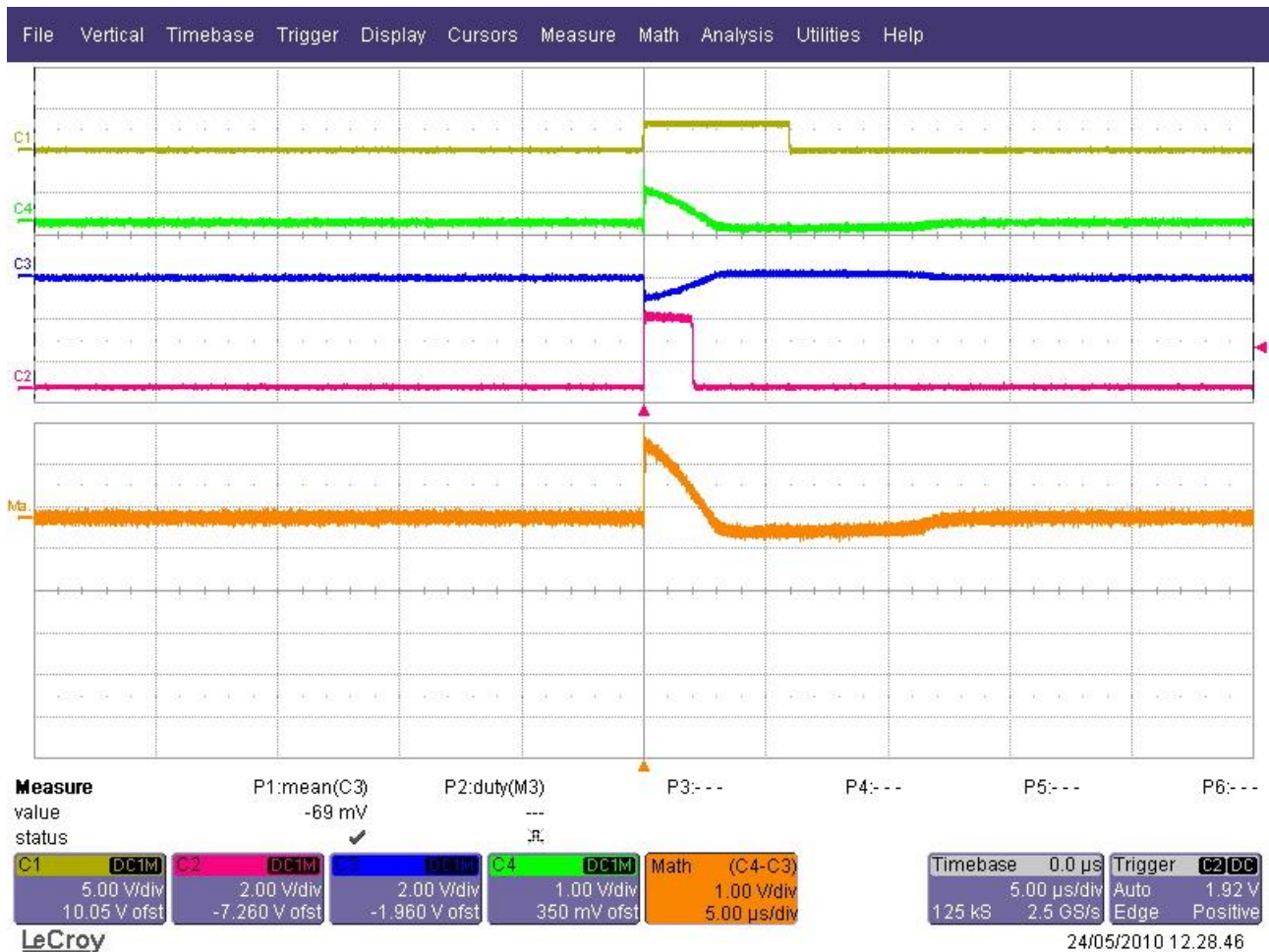
Figure7: Oscilloscope demo image with separate ground

This image shows the signal of C1, C2, C3, C4

> C1: TX signal : square wave PER: 50uS , PW: 5uS, offset: 0v, AMP: 3v;
> C2: RX signal (test point at the second block): square wave PER: 50uS, PW: 2uS, AMP: 3.3v;
> C4: Test point 1 at the kill-switch bus
> C3: Test point 2 at the ground bus
> MATH: C4-C3 we could get the signal on the kill-switch bus with separated ground

At figure7, the grounds of the two blocks are separated, the Ground-bus at the secondary part of transformer are also separated from the primary ground, and two DC power supply are used for two blocks. From the Oscilloscope demo image we could see that this circuit also successfully solves the problem of different ground.

2.3.3 Third stage: PCB board is to produce a performance version of the test circuit

Stage before is based on two modules, in order to further verify the correctness of the circuit design , we need to study the status of the six modules working simultaneously, detection circuit stability and to ensure that is not interference and influence among them.

In the pcb design, we introduced also Bypass capacitor .Because the voltage level for a device is fixed, changing power demands are manifested as changing current demand. The power-supply must accommodate these variations in current draw with as little change as possible in the power-supply voltage. In practice, most digital circuits such as micro controller circuits are designed as direct current (DC) circuits. It turns out that variations in the voltages of these circuits can cause problems. If the voltages swing too much, the circuit may operate incorrectly .By installing bypass capacitors, the frequency of the ripple can have a role in choosing the capacitor value. Rule of thumb is the higher the frequency, the smaller the bypass capacitor you need. A good default value for a ceramic bypass cap is 100nF.
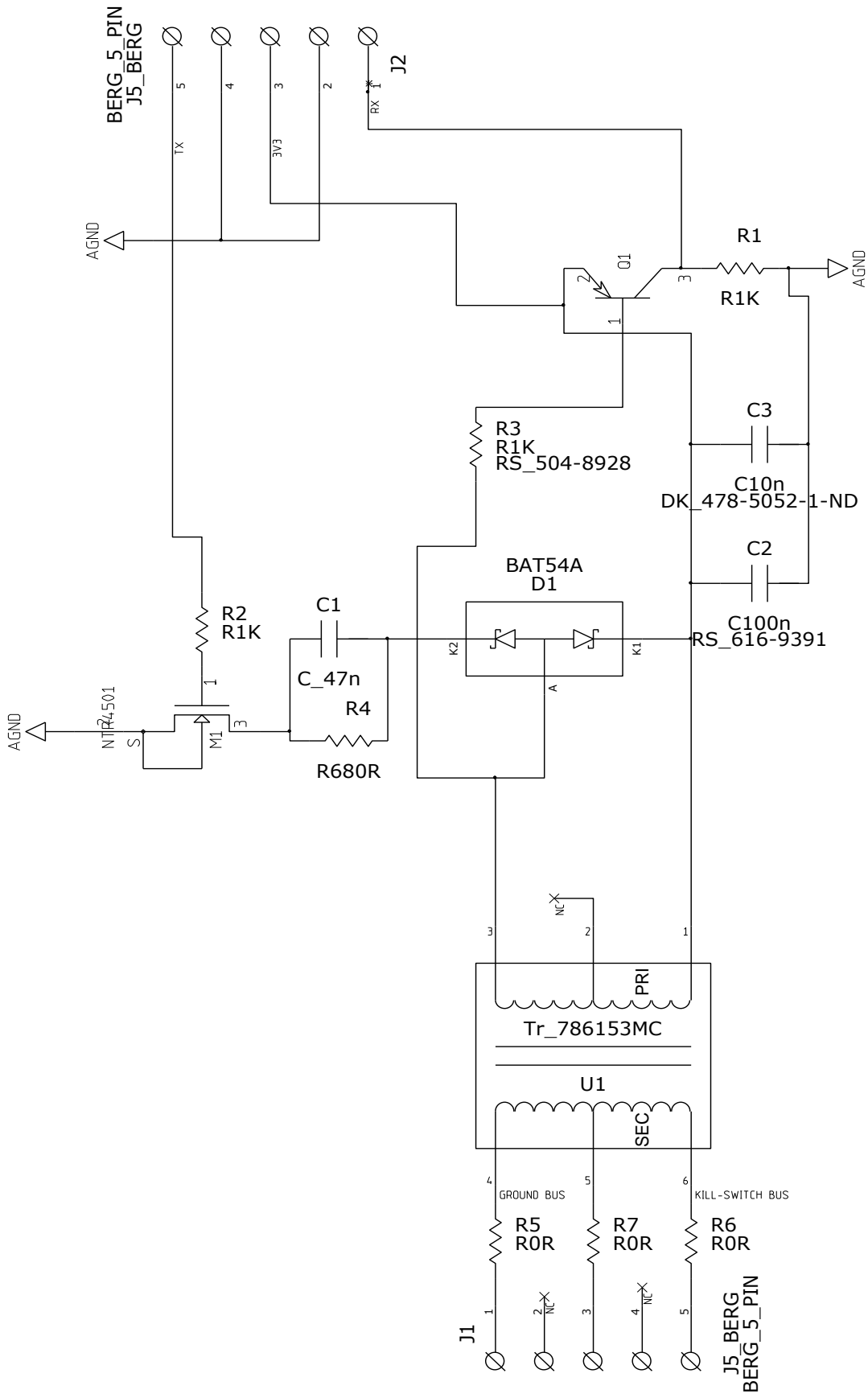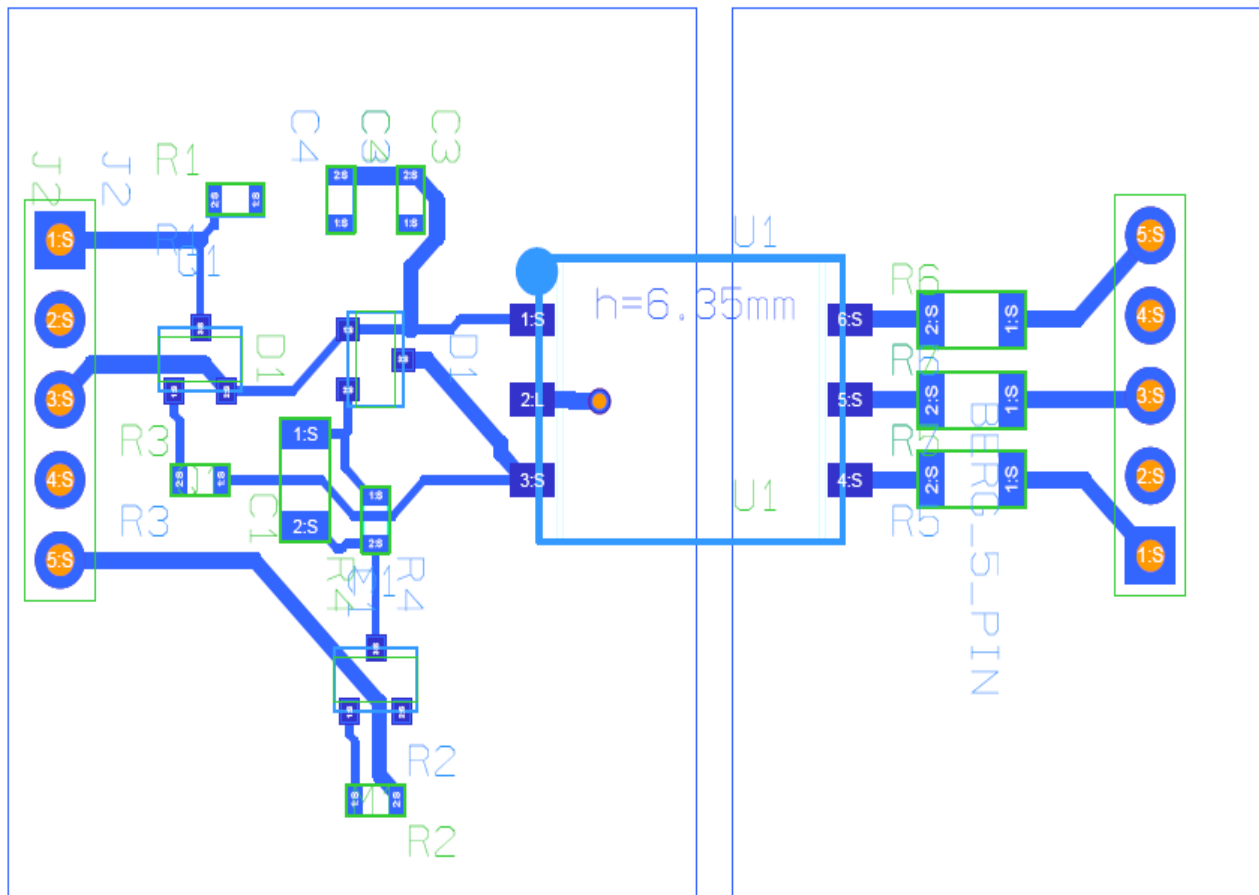
a) Schema of kill-switch PCB board

Figure8: Schema of kill-switch PCB board

b) The components we use

| PARTITION	PART NUM.	PART NAME	PACKAGE	VALUE	NUM
Passives	RS_504_8827	R0R	R_0R_0603_100_1	0R	12
Passives	RS_504_8221	R680R	R_680R_0603_100_1	680R	6
Passives	RS_504_8928	R1K	R_1K_0603_100_1	1K	18
Passives	RS_504_9202	R1K2	R_1K2_0603_100_1	1K2	6
Passives	RS_545_4115	C33p	C_33p_0603_COG_50V_5	33p	6
Passives	RS_652_0134	C47n	C_47n_1026_X7R_100_10	47n	6
Passives	DK_461-2708-1-ND	C1u	C_1u_0603_10V_10	1u	6
Passives	DK_478-5052-1-ND	C10n	C_10n_0603_X7R_50V	10n	6
Diodes	RS_670-8785	BAT54A	D_Schottky_200mA_30V		6
MOS	DK_NTR4501NT1GOSCT-ND	NTR4501	Q_NTR4501_SOT23_3A2_20		6
BJT	RS_484-2381	Q_BF550	Q_BF550_SOT23-3_BJT_PNP		6
TRANSFORMER	ME_580-786153MC	Tr_786153MC	TRANSFORMER		6
CONNECTOR	BERG_5_PIN	J5_BERG	J_5_TH_2.54mm_1_BERG		12

c) Kill-switch PCB layer design (one block design)

MENTOR PCB design software is used for designing, and only one layer is applied in this PCB board, common ground layer. In the middle of the board, the ground is separated according to the requirement.

C:\Documents and Settings\ylsun\kswblock\PCB\kswblock.pcb - Page 1 of 1 pages.

d) Physical board of kill-switch PCB board
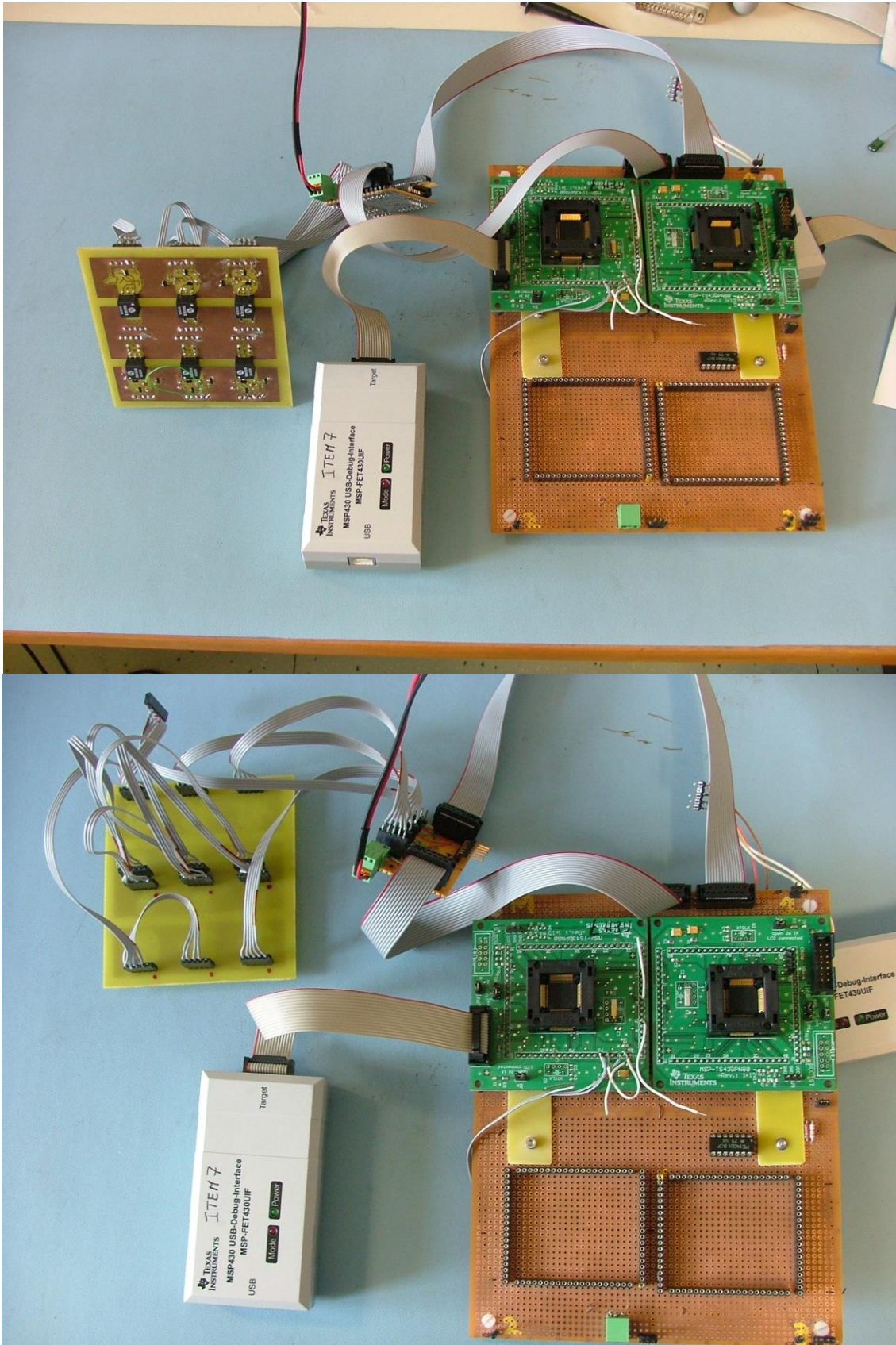
Kill-switch PCB board is on the left and raises a series of cables, which are

connected to a Signal Interconnect board, In order to facilitate measurement.

on the right of the photo, there is msp experimental board, connected with the

Signal Interconnect board.which could not only generate signal TX and can

also receive the signal RX.

e) Measurement of kill-switch circuit for PCB board with oscilloscope

Figure9: Oscilloscope demo image of kill-switch pcb board

This image shows the signal of C1, C2, C3, C4

   C1: TX signal : square wave PER: 50uS , PW: 5uS, offset: 0v, AMP: 3v;
   C2: Kill-switch signal: PER: 52uS
   C3: Test point at the primary part of transformer: 51.3uS,
   C4: RX signal (test point): square wave PER: 50uS, PW: 2uS, AMP: 3.3v;

Figure10: Oscilloscope demo image of RX signal on PCB board

This image shows the signal of C1, C2, C3, C4

All of these test point are RX in different kill-switch block.

2.3.4 The application of MSP and PCB in combination, to verify the
model is able to meet all the requirements.

a) MSP should generate a square wave as the TX signal, at the
same time , it could also detect the signal RX, the program is as
follows,

```
*************************************************************
//  MSP-FET430P430 Demo - Software Toggle TEST
//
//  Description: Toggle P2.0 inside of a software loop to design the square
wave
//  ACLK = n/a, MCLK = SMCLK = default DCO
//
//            MSP430FG439
//          -----------------
//      /|\|          P1.0|-->RX
//       | |              |
//       --|RST        P2.1|<--RX
//         |              |
//         |          P2.0|-->TX
//
//  Texas Instruments Inc.
//  June 2010
//  Built with CCE Version: 3.2.0 and IAR Embedded Workbench Version:
3.21A
//*************************************************************
*******************
```

```c
#include  <msp430xG43x.h>

void main(void)
{ int rx=0;
  WDTCTL = WDTPW + WDTHOLD;              // Stop watchdog timer
  P2DIR |= 0x01;                  // Set P2.0 to output direction as TX
  P2DIR &= ~0x02;                  // Set P2.1 to input direction as RX
  P1DIR |= 0x01;                  // Set P1.0 to output direction as test-RX
  for (;;)
  {
    volatile unsigned int i;

    P2OUT &= ~0x01;                  // Toggle P2.0 using NAND
    P1OUT &= ~0x01;
    i = 5000;              // Delay
    do (i--);
    while (i != 0);

    P2OUT |= 0x01;                  // Toggle P2.0 using OR
    rx = P2OUT & 0x01;
    if (rx != 0)
  { P1OUT |= 0x01;

    }
  i = 10;                // Delay 100uS
    do (i--);
    while (i != 0);

  }
}
```

b) Verify the model.

We apply the MSP430 USB-Debug-Interface to download the program to MSP430, and connect the MSP test board with Signal Interconnect board, from the Oscilloscope; we could get the same demo image as the 4th stage. So we could now get the conclusion of this circuit is suitable for the kill-switch system and could work well in the lab.

3.Conclusion

The project is aims at designing a Kill-Switch compatible with the ARAMIS architecture for modular satellites. Through four stages of the design and testing in laboratory ,we could prove that the design of circuit is compliance with design requirements, software design needs further refinement, such as clever use of MSP430 interrupt program, which could reduce MSP working time, thereby reducing overall system power consumption. By improving the design of software can further meet the design requirements, and optimize overall system performance.