Contents

Chapter 1
Nanosatellite (AraMiS)

1.1 Introduction:

In recent years, many industries and research institutes are trying to access the space. For this, rockets are always used to bring the satellite in the orbit of earth. This makes a lot of effort and tedious that leads to make a small satellite with same pitcher that easily launches in the space along with large number of other small satellites simultaneously. Their launching cost becomes economical when shared by different manufacturer and also affordable for universities and small companies. Secondly, the small satellites are going to decrease in weight, dimension and cost day by day but it increase the complexity of the system progressively. A continuing miniaturization of electronic components has played a major role to decrease the complexity of the system and create an innovation project that no one could ever think about it.

The innovative project known as 'AraMiS' satellite is followed after many experiments and hard working done by many researchers. It is basically a nanosatellite whose weight is between 1 to 10kg. This design gives a low cost and high performance approach to the new world. The reason for high performance is that it has power management subsystem that attains the maximum solar power generated by solar cells. Different numbers of solar cells are used according to its application that should also meet the requirement of budget.

Every satellite system must ensure the critical functions. In particular:

- Power Management System
- Position Control System
- Housekeeping Sensor
- Management and Analysis of Data Control in the satellite
- Telecommunication System

In addition, the components of the satellite are affected by different noise frequency that is generated by internal and external sources. For the external noise, the structure is completely metallic body and it has a good shielding against electromagnetic emissions (EMI). For the internal noise, it creates interference between the various boards or within a same board. It is controllable when placing the appropriate positioning of ground planes of both Analog and Digital units.

Before the end of the project, all the components of small satellite must be described in Visual Paradigm software. It makes for easily understanding and rapidity to define projects in a clear and efficient way. UML is used for the design and documentation of the AraMiS project. The functionality of each and every module of the project must be mentioned in UML.

1.2 History of Small Satellites:

The first developed project of Nano-Satellite made by the researchers of two popular universities named as California State Polytechnic University and the University of Stanford with the

collaboration of the Space Systems Development Laboratory in 1999. It became the standard for all upcoming small satellites. The size of this cubical shape is 10cm x 10cm x 10cm and its total mass is less than 1.33Kg. The diagram of first nanosatellite is shown in below Figure 1.1.

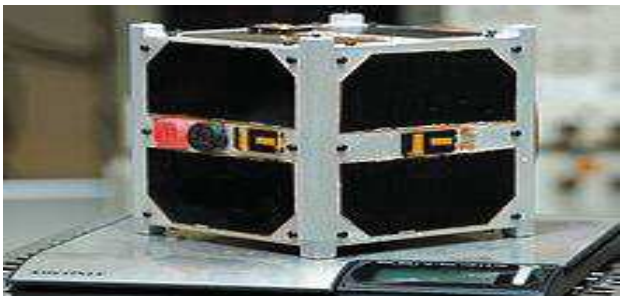


Figure 1.1: CUBESAT Satellite

Another small satellite was created after the first one is known as 'PolyPicoSatellite Orbital Deployer'. In P-POD satellite, Commercial-Off-The-Shelf (COTS) are used to design this nano satellite. It means that the components are purchased from the market in order to meet the requirement of the budget. It also provides a good level of reliability. The diagram of P-POD satellite is shown in below Figure 1.2.

Figure 1.2: Poly-Pico Satellite Orbital Deployer (P-POD).

After this, a special satellite was designed by department of Electronics Engineering (DET) of Politecnico di Torino in 2004. Its name is 'PicPot' cubical satellite and the comparable size is 13cm x 13cm x 13cm. Its mass is less than 5kg and the maximum power consumption is 1.5W. The life of this PicPod in the orbit is 90days. The diagram of PicPot cubical satellite is shown in below Figure 1.3.

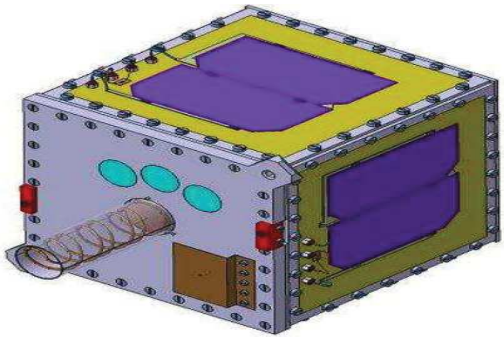


Figure 1.3: PicPod Satellite.

The goal was to measure the temperature and illumination with resulting in data transmission to the ground station from the height of almost 800km but unfortunately, in July 2006 the team of Politecnico di Torino launches the PicPot from the base of Soviet Baykonous but launcher blew up before reaching to the orbit. After this unsuccessful project, university's team continued their research and developed a new nanosatellite known as 'AraMiS'.

1.3 Architecture of AraMiS Project:

AraMiS is modular in electrically, mechanically, protocol and software level. It reduces the cost on designing, testing and fabrication in the field of nanosatellite. The comparable size of AraMiS is 16.5cm x 16.5cm x 16.5cm. Its mass is less than 5kg and the maximum power generated by the solar panel is 6W. The life of AraMiS in the orbit is five years and is modular in electrically, mechanically, protocol and software level. The mechanical modularity means to fabricate the tile and its sub system in our desired shape. Electrical modularity means to obtain same electrical strength of the signal for its entire module. In the same way, Software modularity of the tile allow fast changeable according to the specific subsystem and protocol level modularity able to provide traceability for onboard communications.

The architecture of AraMiS is divided into three main subsystems which are explained below.

- Mechanical
- Power Management
- Attitude Determination and Control
- Telecommunication
- Payload

1.3.1 Mechanical Subsystem:

Mechanical subsystem of AraMiS provides a frame work to place all the tiles close to each other in the sense that all the components are placed in exact and compact position. The skeleton of this mechanical subsystem are cubical form which is made from aluminum. Aluminum is selected for this mechanical structure because of its lighter weight and less corrosion effect from the environment. The Power Management tile having Solar Panels at the outer layer and Telecommunication tiles having Transceiver system are mounted by screws to these rods. As we increase the number of tiles, it will increase the size of nanosatellite along with power. So it can be adaptable for different mission just by increasing or decreasing the number of tiles. Different solar panels of AraMiS satellites are shown in below figure 1.4.

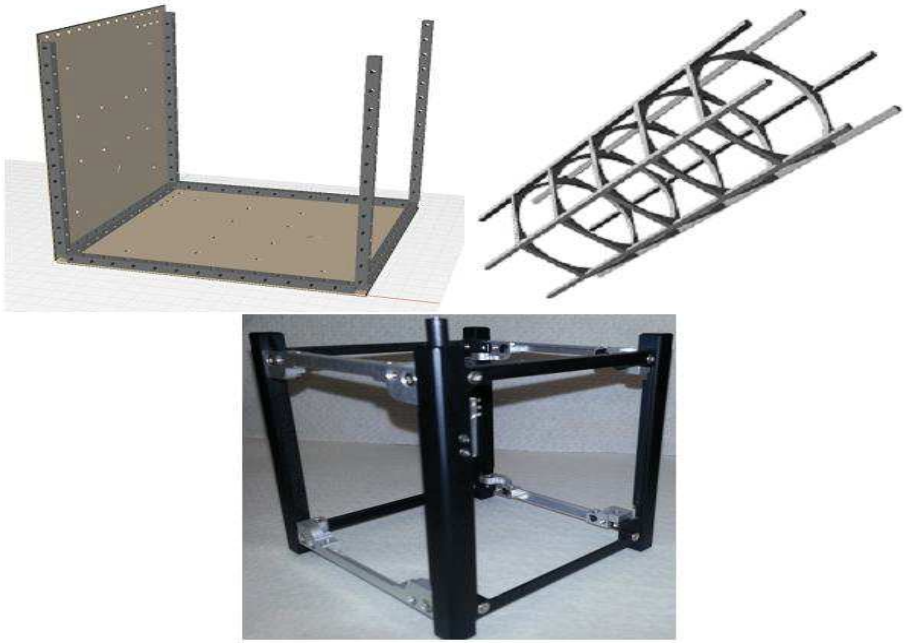
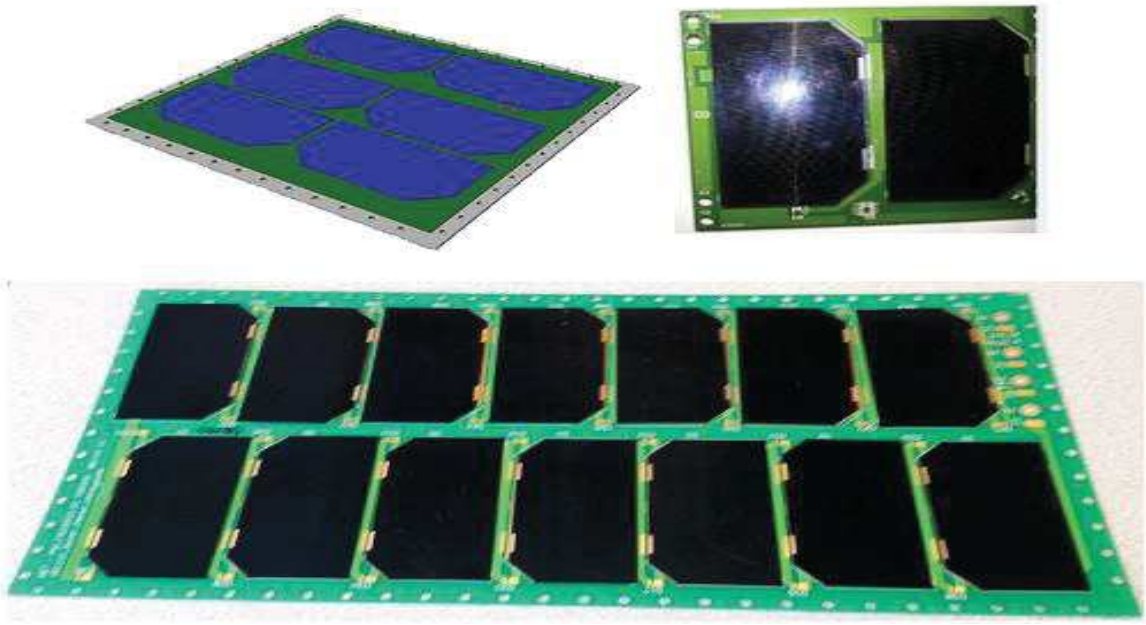


Figure 1.4: Three different AraMiS mechanical structures

1.3.2 Power Management Subsystem:

This subsystem generates, distribute and convert power to different voltage levels according to the requirement of different subsystem. It is the major subsystem because if it fails then it will destroy the whole satellite system. For this a special caring need to fulfill the requirement of this power management. Secondly, managing a power of satellite in any mission consume both time and money. It means that the more we add modules the more it requires power. For this more solar cells are required to meet the requirement of the power. AraMiS use the modular approach that can be suitable for any mission. With the help of this, it decreases the timing of managing power along with reducing the cost. Solar panels of AraMiS satellites are shown in below figure 1.5.



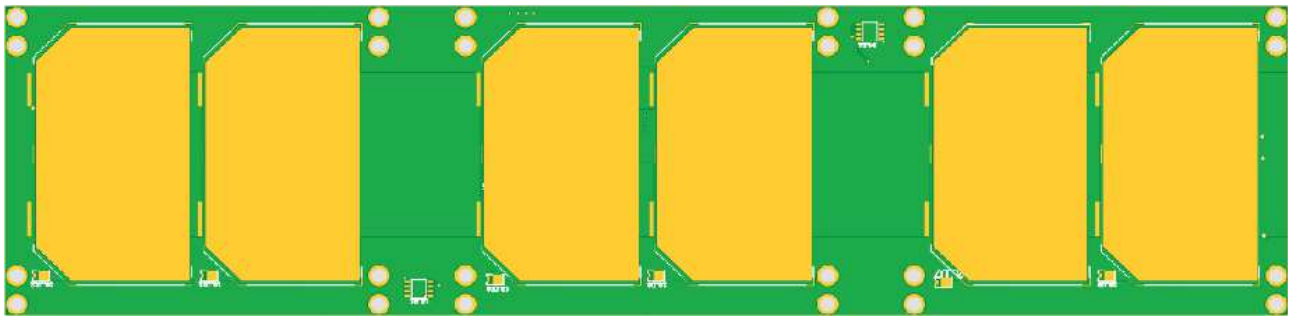


Figure1.5: Four different AraMiS solar panels

1.3.3 Attitude Determination and Control Subsystem:

Attitude Determination and Control System (ADCS) provide an extra feature in the field of nanosatellite. It helps for sense a data and changes the orientation according to desired position in the space. It is divided into two types with reference to its performance.

- Active
- Passive

Passive ADCS has a permanent magnet in the satellite that is simple to adopt and need no power to activate it. It acts as a compass for finding the earth position. The problem in passive ADCS is that when earth magnetic field change then it will leave its spin control and we will get a poor result. On the other hand, Active ADCS is very useful as it has a very good control on its actuator that can change the satellite position after taking the command from the On board Computer. ADCS of the AraMiS are shown in below figure 1.6.

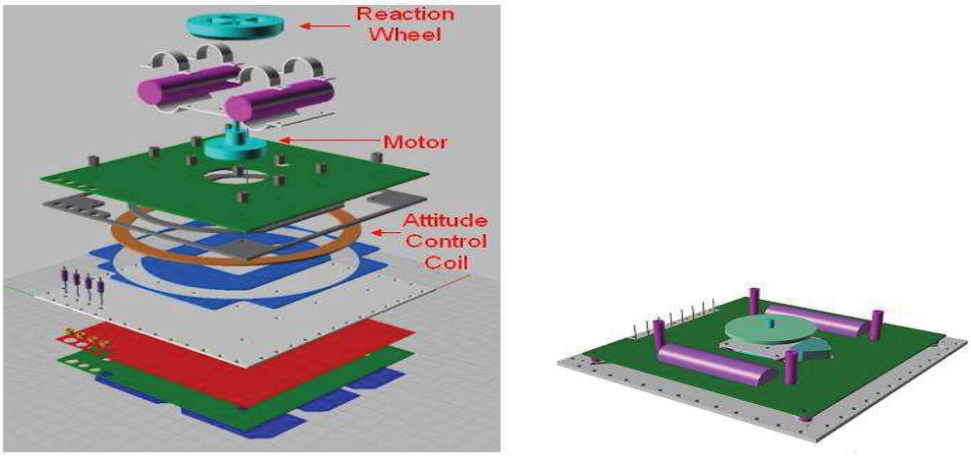


Figure 1.6: AraMiS ADCS modules

1.3.4 Telecommunication Subsystem:

The AraMiS telecommunications subsystem follows the modularity concept. There is a basic telecommunication tile that is provided in a standard AraMiS satellite. In case of special applications, dedicated tiles can be added to meet mission criteria. This module is used to receive command and control packets from the ground station and to send back telemetry and status information. The bandwidth needed to exchange this kind of information is usually low, so the RF link was designed for low speed and low power. The module has been designed using COTS

components which were selected to achieve good fault tolerance level. There are two different frequency bands used for satellite and ground communication: the UHF 437MHz and the S-band 2.4 GHz. To reduce occupied bandwidth, both channels are implemented using half-duplex protocol, sharing the same frequency for downlink and uplink. Telecommunication subsystem of AraMiS satellites are shown in below figure 1.7.

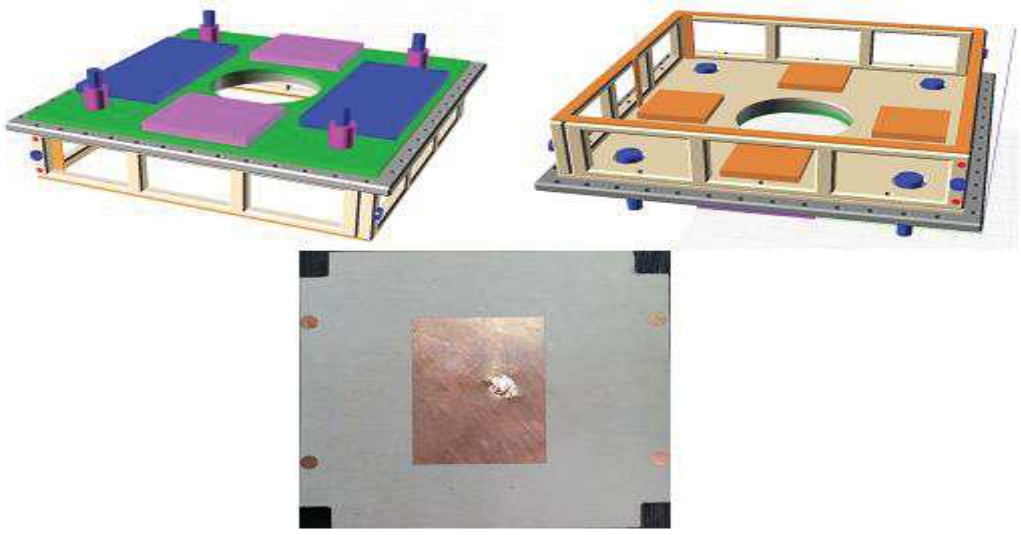


Figure 1.7: AraMiS ADCS modules

1.3.5 Payload Subsystem:

The payload is heavily mission dependent and the architecture was developed to allow high flexibility on it: the main requirements that the AraMiS architecture poses on the payload is its compatibility with the tile power distribution and data bus. Different payloads can be fitted in the various configurations but mechanical fixtures should be developed to connect them to the mechanical structure. Payload subsystem of AraMiS satellite is shown in below figure 1.8.

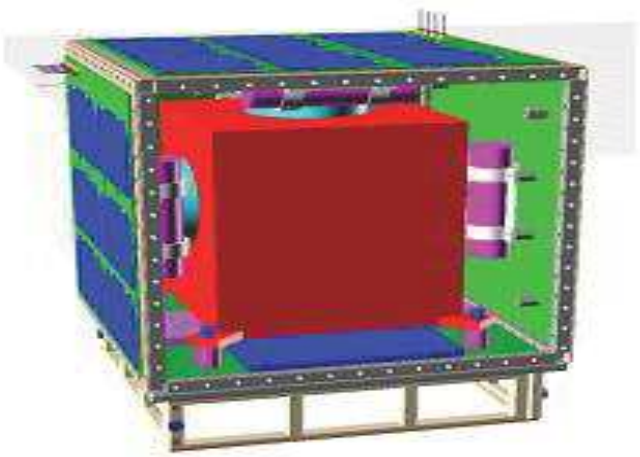


Figure 1.8: Payload inside AraMiS

1.4 AraMiS-C1:

After many struggle and efforts done by the researchers of Politecnico di Torino, AraMiS-C1 is developed in 2007 that is one unit cubical standard satellite based on the modular approach of AraMiS. The body of AraMiS-C1 is created by six external blocks known as 'Tiles' which give power and data standardized interface. There are two types of external tiles. One is known as 1B8 power management tile that combine with three other cubical tiles that is used for large scale integration and compact stack of different resins and material. It include solar panel, external battery, attitude determination and control system and housekeeping sensors. Secondly, the other two tiles known as 1B9 telecommunication tiles that contain micro-controller based programmable transceiver, 437MHz and 2.4GHz modem, Low noise amplifier for reception and power amplifier for transmission. It also has deployable UHF antenna in one side and SHF on the other side of tile. This tile controls the data and command exchange to or from the earth. Inside of these tiles, there is a space that is used to place the payload. 1U AraMiS-C1 with its two types of tiles is shown in below Figure 1.9.

Figure 1.9: Image of AraMiS-C1

AraMiS-C1 has the following subsystems:

- ISIS-1 Unit Cube Sat Structure
- 1B8_CubePMT Modules
- 1B9_CubeTCT Modules
- Payload
- Battery Pack
- UHF Antenna
- Harness
- Onboard Data Handling
- On-Board Computer (OBC)

1.5 Temperature effects on AraMiS:

The satellite revolving in the orbit throughout the mission ,has it's faces subjected to different temperatures depending on its position relative to the Sun .The faces of the satellite towards the sun is illuminated by the sun rays and the other faces are in the dark. The strong temperature gradient is not only because of the lack of the atmosphere at this altitude and the irradiation reaches values of 1300 Wm which is much higher than its present on earth. The high temperature rise is also

due to the overheating of the electronic components on board, by conduction and radiation. Theoretically, the working temperature of the satellite is of the range, (-30 to 40) ° C, having the maximum power dissipation Pj by the internal circuit is about 200W.

Chapter 2
Software Tools and its Applications

2.1 Introduction:

In this chapter, we will describe the usage of different software tools for the AraMiS project. These software's will help in finding the design and simulation of electronic circuits, selection of the components, its library management and proper documentation of the testing of the circuits.

The most important tool we use in this project is Mentor Graphics that helps us in designing of electrical schematics. To work on it we have to add the Aramis_Mentor_Lib project library and then remove the errors in already made schematics of electronic circuits. The confirmation of the removing all the errors is easily seen once we create the Net list for the designed circuits. After making the simulation of all sub components, we have to make the printed circuit board with the help of its tool of Expedition PCB in Dx-Designer. We preferred LT Spice-IV for the simulation of circuits because of its easy to use, good to manage even for switching circuits and good quality product.

Another important tool we use in this chapter is unified description languages UML. For this, we have to work on Visual Paradigm software 13.2 that can allow different user to work on it in the sense to maintain the record of different sub component of AraMiS project independently.

2.2 Mentor Graphics 7.9.4:

Mentor Graphics as we explained above is one of the most important tools for different complex electronics circuit design. It is followed by Dx-Designer software that can provide an environment to complete circuit design for its definition and reusable components. The silent features of this software tools are given below:

- Design Capture tool is used for making the real schematic diagram.
- Aramis_Mentor_Lib Library contains all the devices and components that are used in AraMiS project, their packages and different simulation models. If the error comes because of the missing spice model of any electronic component then there are two ways to solve it. Firstly, search the spice model on the internet if it is not available then make the spice model by its own after reading the data sheet.
- The simulation of electronic circuit can be possible on the Dx-Designer by using simulator Hyper Lynx but we preferred LT-Spice for the simulation because of some reason which we will discuss it later on.
- Printed Circuit Board is designed and manufactured with the help of its tool Expedition PCB.

2.2.1 Aramis_Mentor_Lib:

The main central library known as 'Aramis_Mentor_Lib' provides a real time interface where all users can use it at the same time and share their design circuits. In this library, there is special block

known as ‘Reusable Block’. It contains logical, physical and both logical and physical block that is used in our project. Logical block mean it contains only the circuit diagram, Physical block mean it is composed of only the layout of the circuit diagram. It is helpful for the production of printed circuit board and both Physical and Logical block contain the components of the circuit from the layout to its application level. Additionally, these reusable blocks are helpful in order to improve the electronic components by removing all the errors inside of it. This improvement is possible by editing the affected block directly on the schematic. This way can save the time and energy.

In Library manager tool, it shows all the parts of the component by search it with any command of Part Number, Part Label or Part Name. Part number contains the information of Supplier code, Part name contains the information of the package and Part Label contains the information of Electrical characteristic.

After finding any part in the search icon, it contains the further representation of the component represented by Symbol and Cell. The symbol has the logical shape of the component in electrical diagram while the Cell has the mechanical shape of electronic Pad that is useful for the PCB design.

In Part Editor Window, additional information is available which also considerable for any electronic circuits. Its main parameters are Value, Model and Pin Order etc. It is representing in below Figure 2.1.

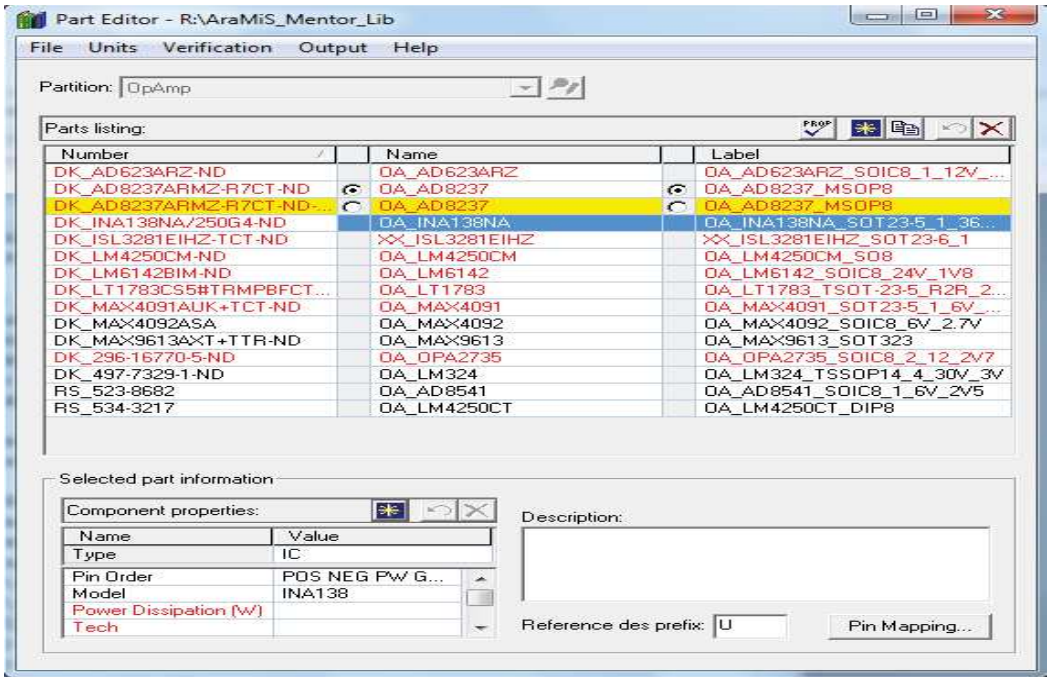


Figure 2.1: Part Editor window for Aramis_Mentor_Lib

Its important properties are explained below.

- Value means the value of physical quantity of the part. For example: suffix K equal to10^3.
- Temperature Coefficient (TC) means the effect of temperature on the passive components.
- Tolerance means the range of the variation of Resistor, Capacitor and Inductor values in percentage form.
- Model means the name of the spice model associated with a given device model.

- Pin Order means the pins of the symbol that corresponds to the simulation model. It is helpful to judge the behavior of the device in better way.
- Reference des Prefix means to show the template of part. For example, for resistor R, for capacitor C, for inductor I etc.

2.2.2 Design Capture and Expedition PCB:

For actualization of the schematic of electronic component and making their Net list, design capture is one of the most remarkable tools. Net list produce an output command of the relative circuit in .expt format. This format is useful for the simulation of relevant circuit in LT-Spice. Another term is 'Packager' that is helpful to distinguish one component from another component. It analyzes the entire component to map them in the form of cell that will proceed in making the PCB by using the command of Expedition PCB.

Another interesting factor is the ICES (interactive Constraint Editor System (CES) that helps to define the parameters corresponding to the trace routing. It includes classes, sizes and distances etc. for the actualization of PCB. It is a design capture which allows a faster way to define main characteristic of various Net representative of the physical connection between different devices on the printed circuit board. It is representing in below Figure 2.2.

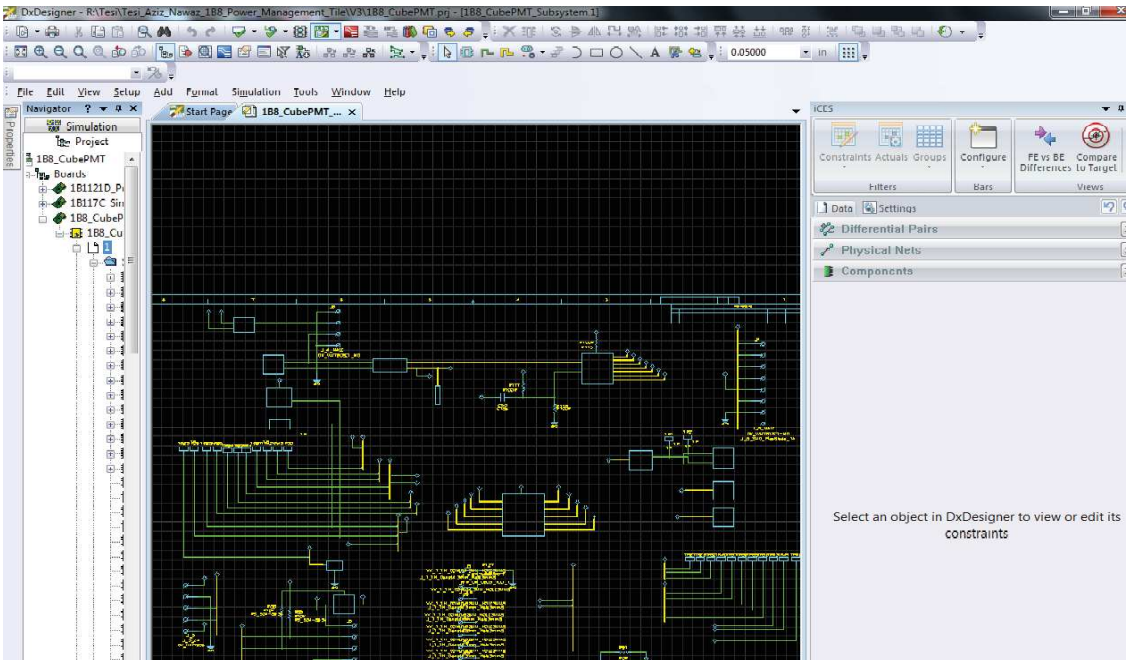


Figure 2.2: Using iCES inside the Design Capture

In expedition PCB software for making the design of PCB, it should be define initially for the actualization of Tabs (4 or 8 layers). We have to follow the below steps in order to avoid any difficulty in making PCB.

- Run the Forward Annotation that makes the connection of schematic with the printed circuit.
- Make the Tile shape and choose the area for making possible route of border.
- Put all the components inside the printed circuit.

- Define the constraint that includes distance between lines, its thickness, Vias formation and distance between components etc.
- Initially, run auto routing but in the middle, it can be possible to still connect unconnected components with the help of manual routing.
- Generate the output file for physical PCB design: Gerber File and NC Drill.
- Display Control helps to facilitate all operations including enabling and disabling the components in different layers, some information can be seen that is related to specified cells, mirroring forward vision tab for a better view of the top and bottom layer.
- Update the cells later on after making some changes in the cell by using Update command Cell & Pad stack.

2.3 Changing Environment for Simulation from Mentor Graphics to LTSpice:

For the simulation of electronic schematics on Dx-Designer, It was preferred to simulate it on the LTSPICE IV .The reason not to simulate it on Mentor Graphics was that the simulator Hyper Lynx is based on HSPICE syntax and for this we need to make the model in this format. On the internet, mostly manufacturer use PSPICE language in order to model the electronic component. For this reason, LTSPICE was one of the convenient ways to simulate the circuit efficiently.

On the other hand, this software is open source and free to use. It is suitable for the switching regulators and power circuits. Below are some steps that need to follow in order to perform the correct simulation.

- Firstly, use the tools Design Capture for making schematic in Mentor Graphics.
- Generate the Netlist by clicking the option > Netlist. There are two possibilities whether the Netlist will be successful or not. If it is successful then continued it by selecting the expt file in sym folder and two .spi file in genhdl folder. These two spi files are generated after setting the parameters of simulation in Dx-Designer. If it's not successful then remove all the relevant error mostly the error come because of spice model missed in some components and then start the same process as we explained above.
- For Monte Carlo Simulation it is necessary to define the Random Simulation including .dc or .tran or sometime both are used at the same time.
- Remove the following lines in .expt formatted file before run the command icon:
  - .include "resultDisplayFile.Aqr
  - .OPtion dcmode = all
  - .OPtion trmode = Fast
  - .OPtion Tnom = 27 (optional)
- Add the command related to desire task and then save the expt file. Different types of simulation are given below.
- Monte Carlo: .step param < Initial Step > < Final Step > < Step Entities >.
  For example .step param 1 100 1, starts from step 1 up to hundred with increase of one so in total a number of cases equal to 100.
- Temperature: .step TEMP < Temp Start > < Temp End > < Step Increase >. For example .step TEMP -35 135 1, starts from step -35 up to 135 with increase of one step, so in total a number of steps equal to 101.

- Transient Analysis: .tran < Print Time Interval > < End Time > < Start Time > < Max Time >. For example .tran 100U 10 1 50M, starts from 1 second to 10 second with relevant print time interval and maximum time.
- DC Analysis: .dc < Parameter Name > < Initial Value > < End Value > < Step Increment >.For example .dc IOUT 0 0.152 0.001, IOUT starts from step 0 up to 0.152 with increase of 0.001.
- If the error is like ‘error on the spice netlist generated’ then remove the '+’ in the last line that includes the source files.
- Lastly, when the simulation finish then save the output just like in the figure appears below.

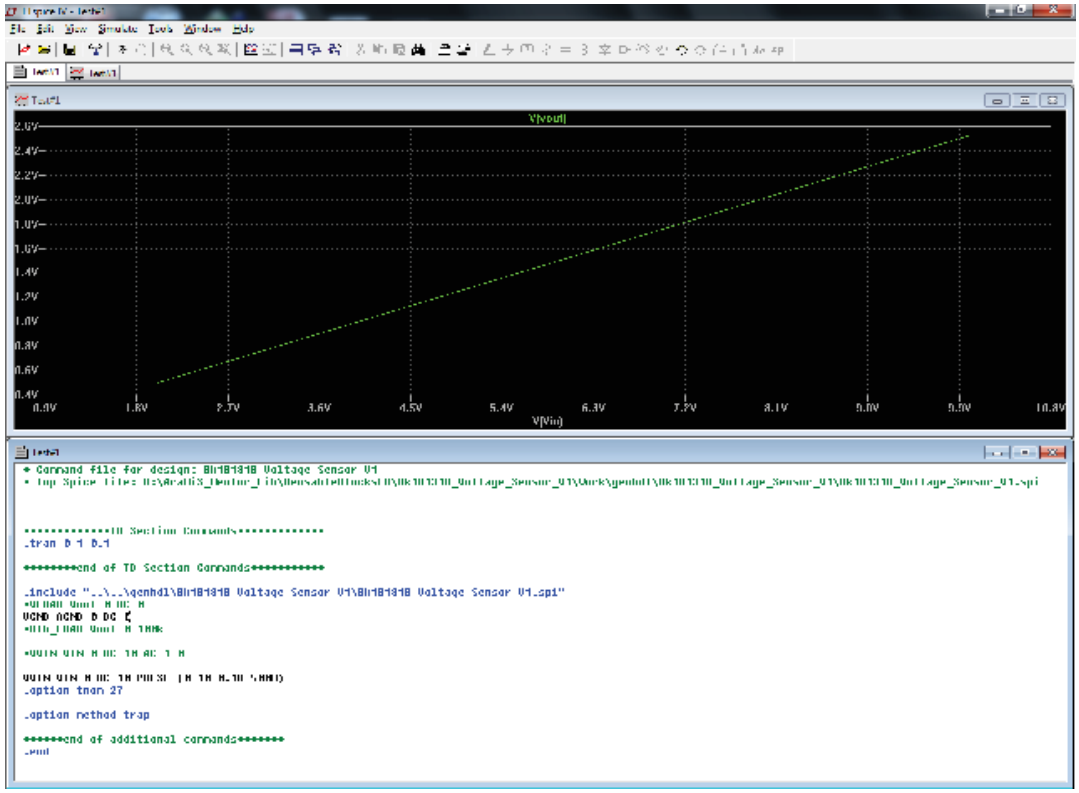


Figure 2.3: Simulation on LTSPICE

2.4 Visual Paradigm 13.2:

The UML (Unified Modeling Language) as we described above is a unique language that represent Visualization, Modeling, Communication and proper documentation for any type of project. It handles both software and hardware of the project. We can say it as a high level object oriented language that use in visual paradigm which shows the project in different diagrams. Every subsystem of the project is usually composed of hardware and corresponding software. Their Subsystems names are used according to the terminology for their classes in UML.

AraMiS project is successfully executed with the help of visual paradigm 13.2. It is because of the fact that it provides the environment to convert high level codes representing different diagram into low level codes that is executable with the help of microprocessor MSP430. UML language can be managed by a large number of people in a group. It is followed with the help of server in which one

can load the work that is quickly accessible by another user. It includes the diagrams for Performance Specification, Functional Specification, Documenting software or hardware of the project and Analysis of the system and its subsystem. UML provides a lot of diagrams, including class diagram, use case diagram, sequence diagram, requirement diagram and state diagram etc. All the diagrams in visual paradigm show the properties in different point of view. Selecting different diagram depend on the behavior of the system. The most useful diagrams include use case and class diagrams that we are going to describe.

2.4.1 Use Case Diagram:

Use Case Diagram is a diagram that describes the functions of the system and its Actors. These actors are represented by 'a little man'. The whole diagram shows the relationship between actors and their use cases with the help of arrow line known as association. The shape of the arrow tells the type of association. It is represented in below Figure 2.4.

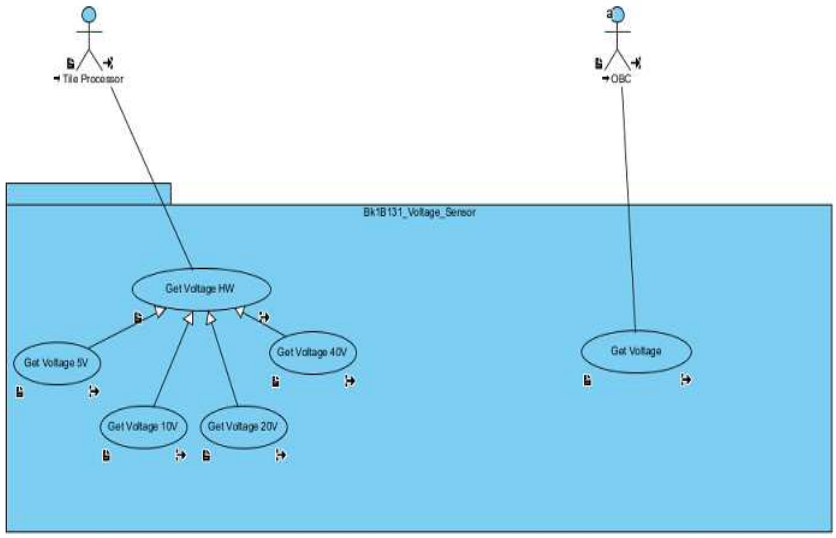


Figure 2.4: Example of Case Diagram in Visual Paradigm

2.4.2 Class Diagram:

Class diagram is one of the interesting graphical representations of class and its inheritance. These inheritances include the logical and physical linkage between two classes that are distinguished with the help of arrow direction and its type. In other words, it is basically a good idea in which graphical object helps to describe the structure of a system, its components and their relationship between them. It is further represented by its class name, attributes (characteristic of object) and object's operations. It is representing in below Figure 2.5.

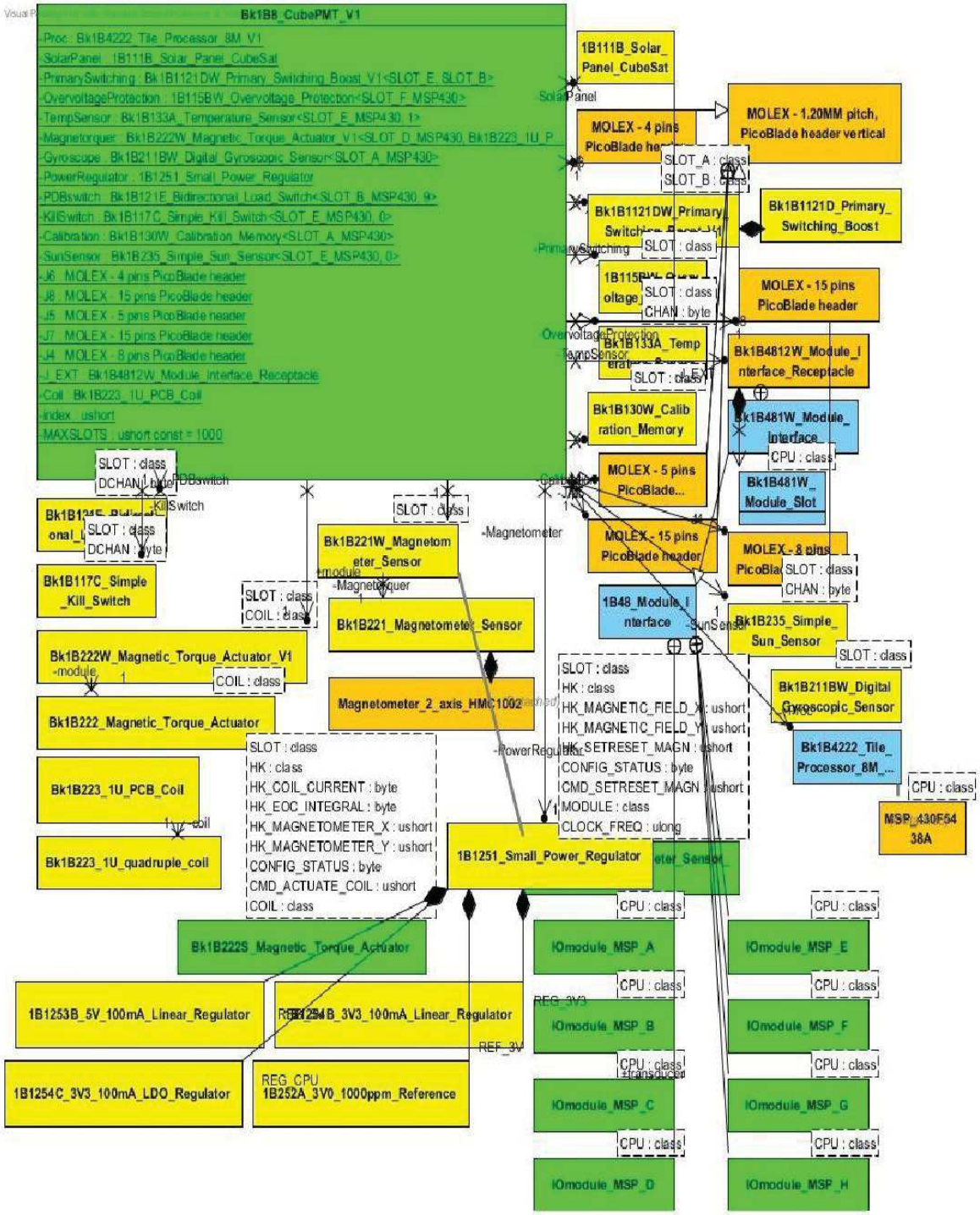


Figure 2.5: Example of Class Diagram in Visual Paradigm

In visual paradigm, it has the information for each class in section of class specification for better understanding the characteristic of class. In this way, all the difficulties can be removable to perform the simulation of electronic circuit in real world. The class diagram is very efficient for the complex system where many subclasses of main class are available. It is shown in below Figure 2.6.

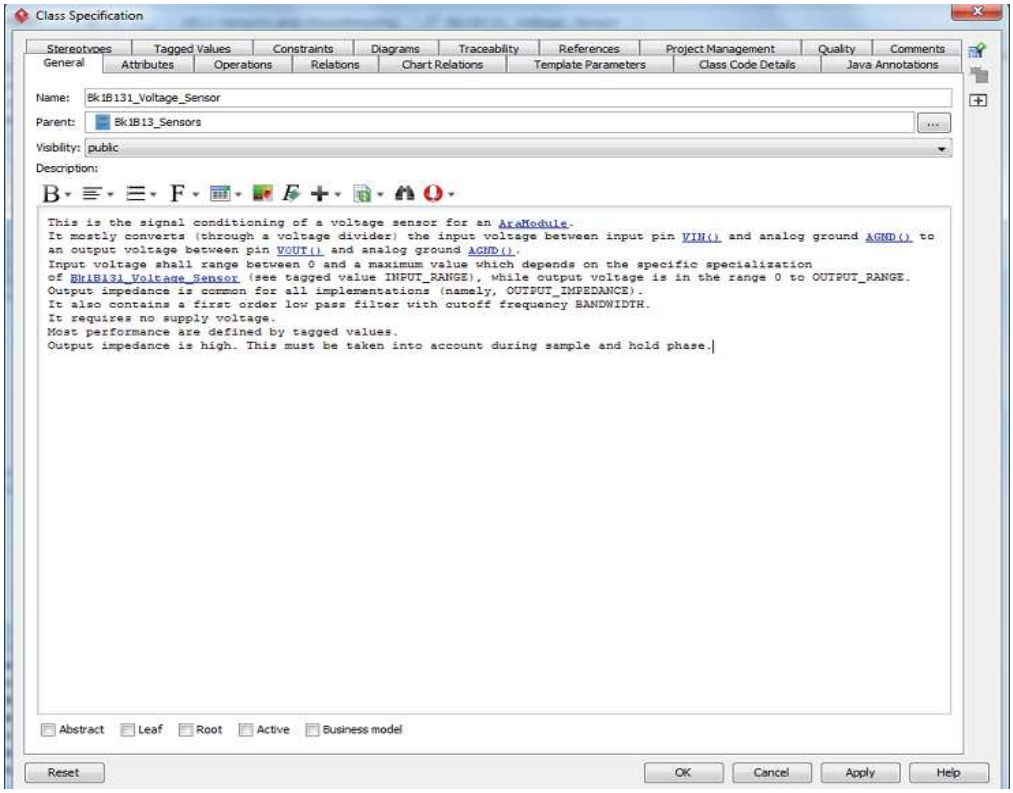


Figure 2.6: Block Description in Visual Paradigm

In the same bar of class specification, there is another important tab known as ‘Tagged value’, in which the class specifications corresponding to its datasheet are available. It is represented in below Figure 2.7.

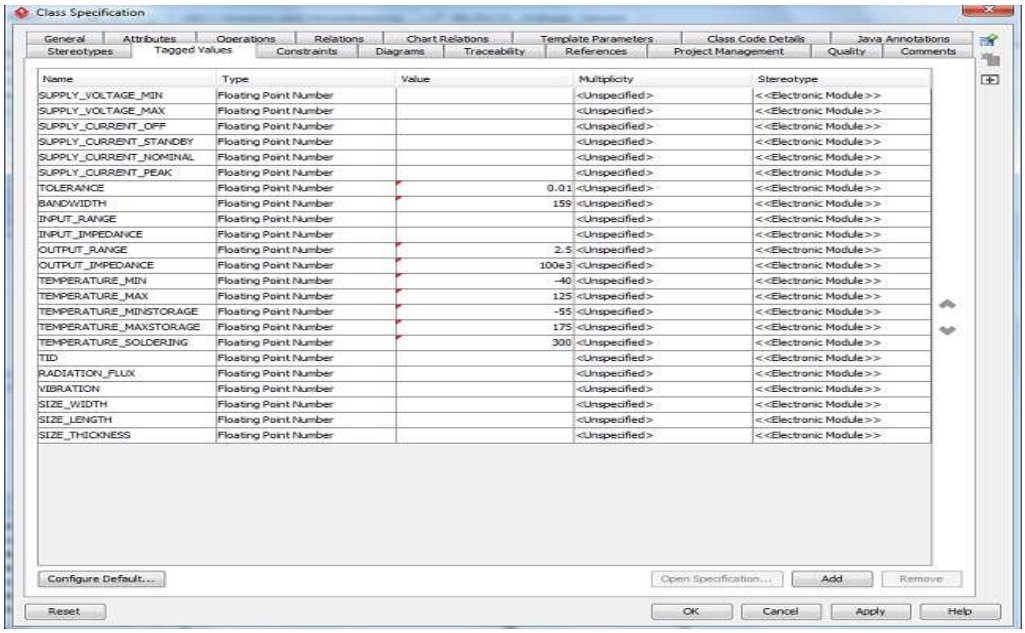


Figure 2.7: Specification of reference block in Visual Paradigm

Within the same bar of class specification, there is also an important tab ‘References’. Here the path of the reference folder is added that contains the simulation results of subsystem of the project. It provides an immediate check of functional specification of the associated class. It is representing in below Figure 2.5.

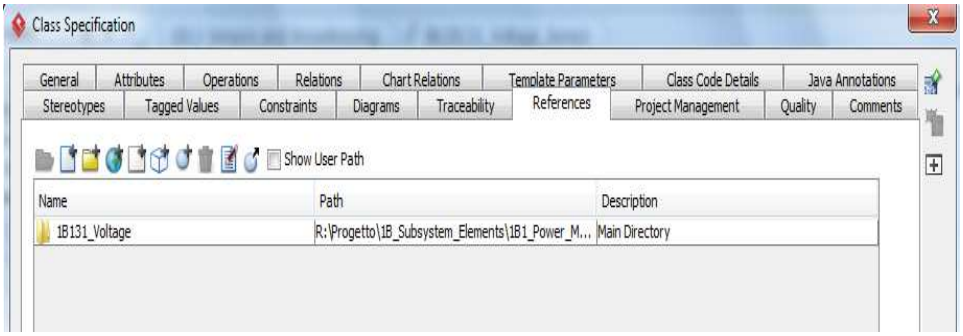


Figure 2.8: Adding specified Path directory in Visual Paradigm

Chapter 3
General Project

3.1 Introduction:

1B8_CubePMT is a tile of AraMiS that contains Electric Power Supply, Attitude Determination and Control system. It is mounted on the four external sides of the AraMiS-C1 while the other two sides have the telecommunication tiles called 1B9_CubeTCT. Electric Power Supply system helps to control the power generation while the Attitude and determination control system controls the position of spinning of satellite across the earth.

EPS system contain solar panel, boost converter, housekeeping sensors, load switches, linear and switching regulators and ADCS contain sun sensor, magnetometer, gyroscope, magnetic torque actuator and magnetorquer coil. It also has microcontroller MSP430F5438 that helps to manage the power and data processing and maintain its operation.

Modular power management tiles (PMTs) are already available in the market but they are less efficient, heavier in weight, consume more power and contain less number of subsystems. The goal of this work is to implement EPS and ADCS subsystems in a single module focusing on the main issues and adding some additional features. 1B8_CubePMT is developed on the design approach of AraMiS architecture using the satellite on demand design flow configuration.

This chapter is devoted for understanding both the tile of 1U and 3U AraMiS. Their subsystems descriptions, implementations and testing details will be discussed in following chapters. The outer and inner image of 1U AraMiS-C1with its tiles are shown in below Figure 3.1.

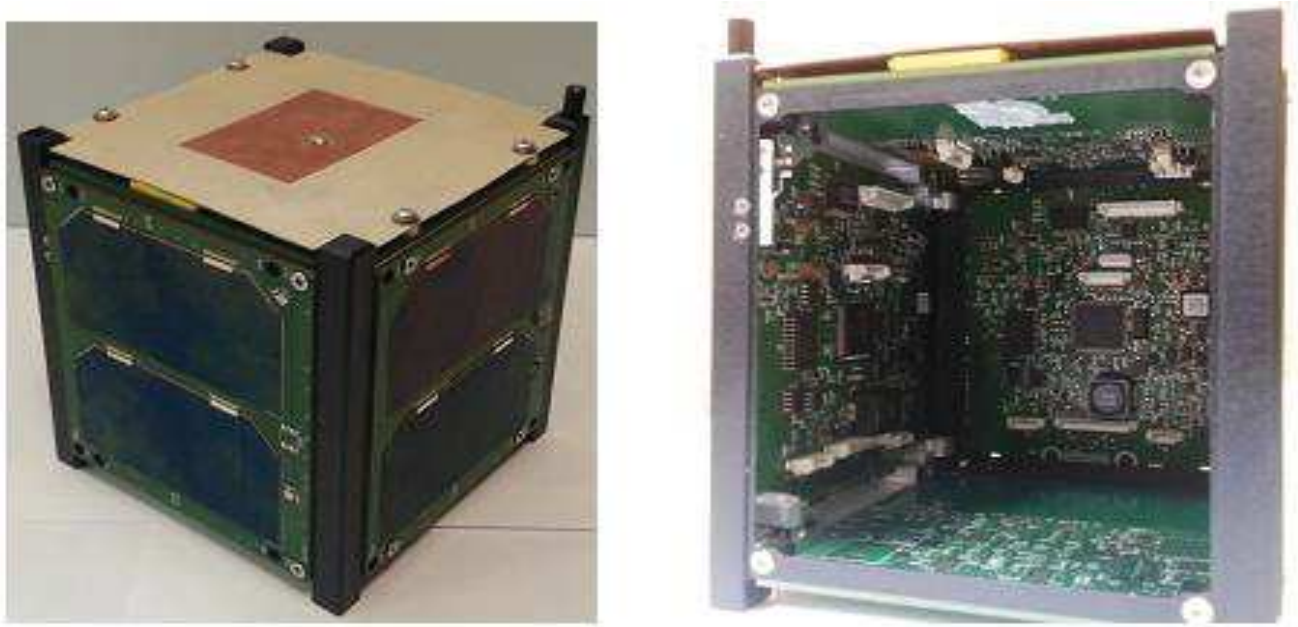


Figure 3.1: Image of 1U Aramis-C1

3.21B8_CubePMT_1U:

In Cube Sat, EPS and ADCS are the most essential elements of any aerospace mission. Efficient EPS and precise ADCS are the core of any spacecraft mission. So keeping in mind their importance, they have been integrated and developed on a single tile called 1B8_CubePMT_1U module. It acts as mechanical structure for AraMiS-C1 satellite.

Two solar cells and Sun Sensor are attached at the external body but the electric power supply and ADS systems are attached inside of 1B8_CubePMT_1U tile. The efficiency of solar cells is 26% that convert solar energy to 4.4V. Sun sensor is used to tell the direction of satellite across the sun. Boost Converter are mounted inner side of tile processor that step up the solar panel voltage (4.4V) to 14V.This is because of the fact that it has the efficiency of 93%. Magnetometer and Gyroscope also be connected inside the tile that is connected with MSP430 micro controller with the help of SPI bus. MSP430 microcontroller is the heart of 1B8_CubePMT tile that manage all the process of whole system. Its block diagram is shown in below figures 3.1.

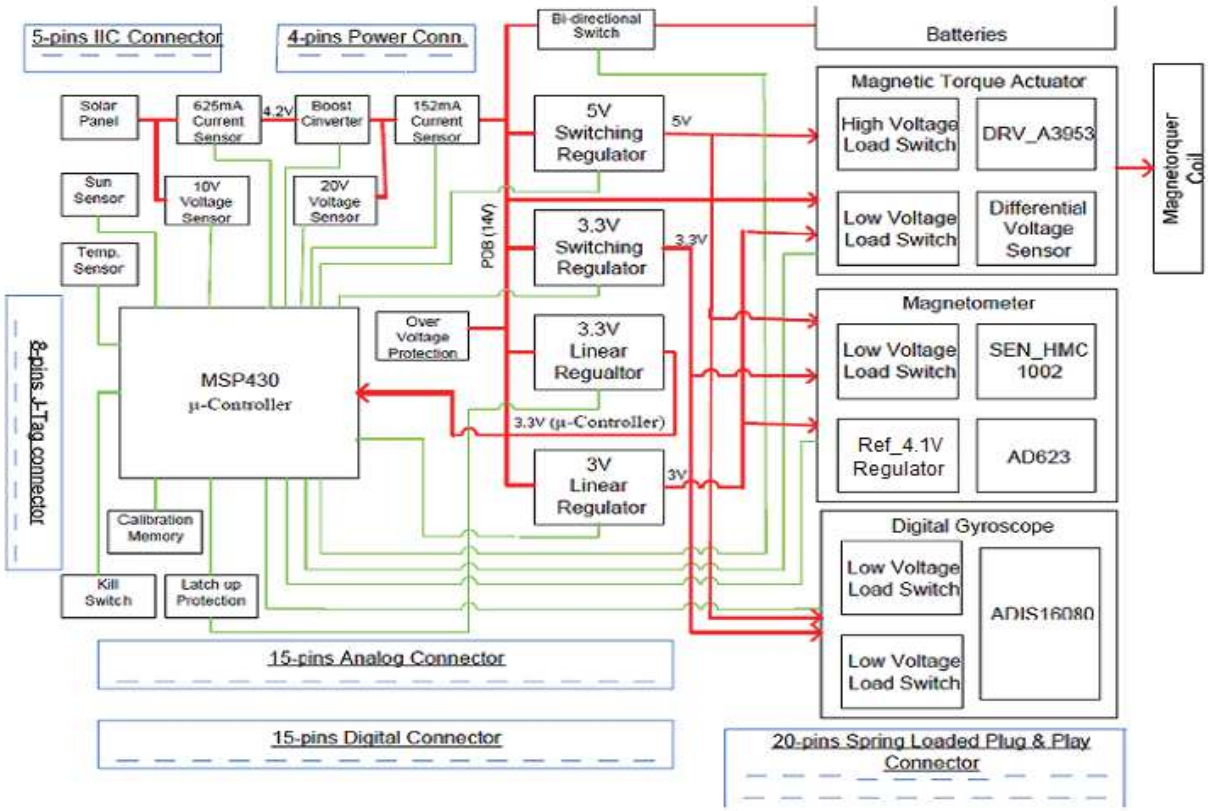


Figure 3.2: Block diagram of 1B8_CubePMT_1U.

3.2.1 Subsystems of 1B8_CubePMT_1U:

The 1B8_CubePMT_1U system can be further divided into seven subsystems which are explained below.

- **1B1 Power Generation and Storage:** It is used to generate energy, store it and manage it. It covers the subsystems including two cells Solar Panel (1B111B), PWM DC Converter (1B1122) and Over Voltage Protection (1B115B) and Boost Converter (1B1121D).

- **1B12 Power Distribution:** It is used to distribute the power for AraMiS. It covers the subsystems including two Linear Regulators (1B1252A and 1B1254C), two Switching Regulators (1B1253B and 1B1254B) and three Load Switches (1B121C, 1B121D and 1B121E).
- **1B13 Housekeeping Sensors:** It is used to control the power management subsystem. It covers the subsystems including two Current Sensors (1B132A and 1B132D), two Voltage Sensors (1B131B and 1B131C), Temperature Sensor (1B133A) and Calibration Memory (1B130W).
- **1B21 Inertial Attitude Control:** It is used to control all the measurements related to Angular Velocity for AraMiS. It covers the subsystem including Gyroscope (1211B).
- **1B22 Magnetic Attitude Determination:** It is used to control all the measurements related to satellite orientation in the orbit and gives this information to on board processor. It covers the subsystems including Magnetometer Sensor (1B221), Magnetic Torque Actuator (1B222) and Magnetorquer Coil (1B223).
- **1B23 Other Attitude Control:** It is used to determine attitude parameter for AraMiS. It covers the subsystem including Sun Sensor (1B235).
- **1B4 Process and Module Interface:** It is used to manage and process for AraMiS and connect its subsystems with external interfaces. It covers the subsystems including MSP430 Microcontroller (1B4222), I2C Interface (1B4851), RS232 Interface (1B4852), JTAG interface (1B4854) and PDB interface (1B4861).

The images of both sides of 1B8_CubePMT_1U tile are given below in Figure 3.3 and 3.4.

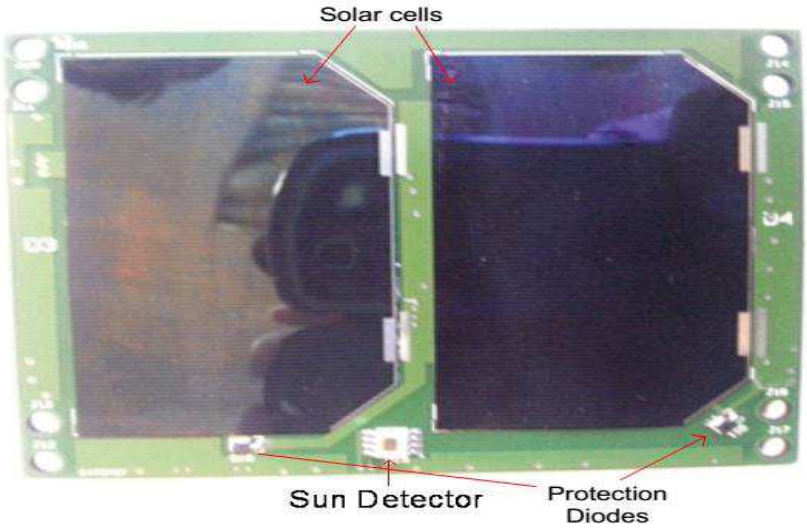


Figure 3.3: Diagram of the external background of 1B8_CubePMT_1U module.

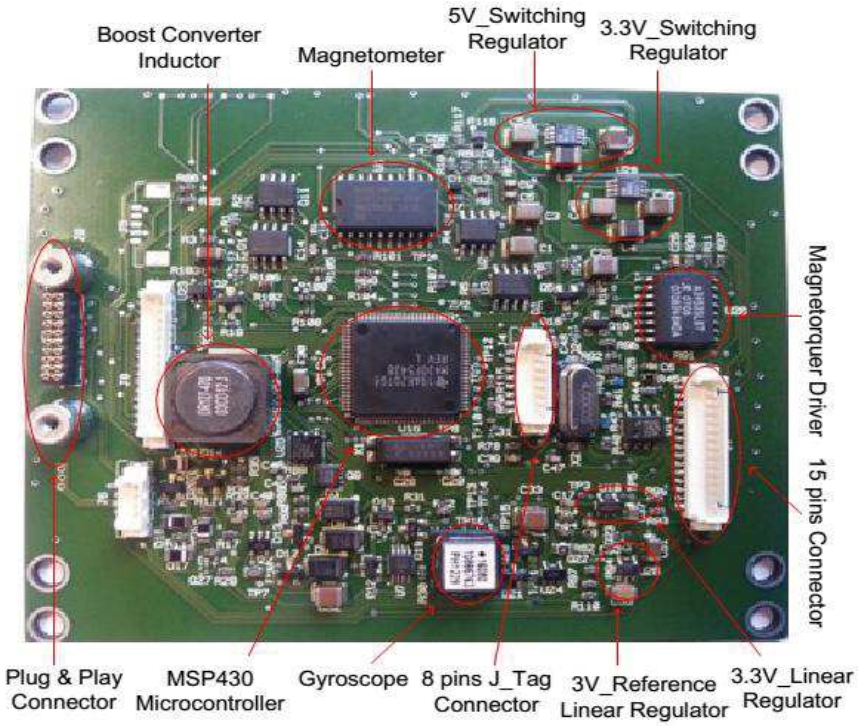


Figure 3.4: Diagram of internal background of 1B8_CubePMT_1U module.

3.2.2 Cross-Sectional view for PCB of 1B8_CubPMT_1U:

PCB of 1B8_CubePMT_1U is divided into eight layers with dimensions equal to 98.0×82.5×1.6 mm3. One sun sensor is directly attached to the first layer of PCB and two solar cells are attached to first layer of PCB with the help of resin. From layer two to layer five contains 200 turns of magnetorquer coil. Sixth layer has the ground plane while the seventh layer has partially covered with ground plane. The last layer (eighth layer) contains PCB traces to connect the components.

Above the PCB, there are two 15 pins connector that is use to contact the digital and analog signals of the systems. A 20 pins plug and play connector is used to connect further subsystem to communicate with tile processor. There is 4 pins connector on the PCB that is reserved for the solar panel and PDB. Lastly, an 8 pin J-tag interface is used to debug and program the tile processor and a 5 pins I2C interface is used for connecting a tile with other tiles. Cross sectional view of 1B8_CubePMT_1U and its dimension are shown in below Figure1.11and Figure1.12:

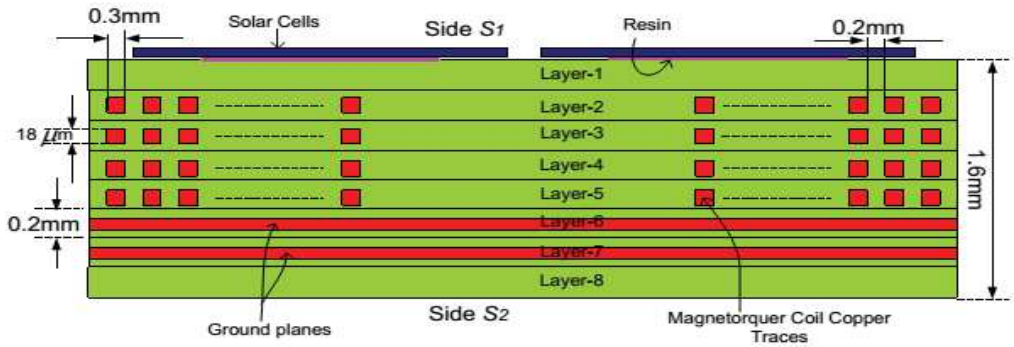


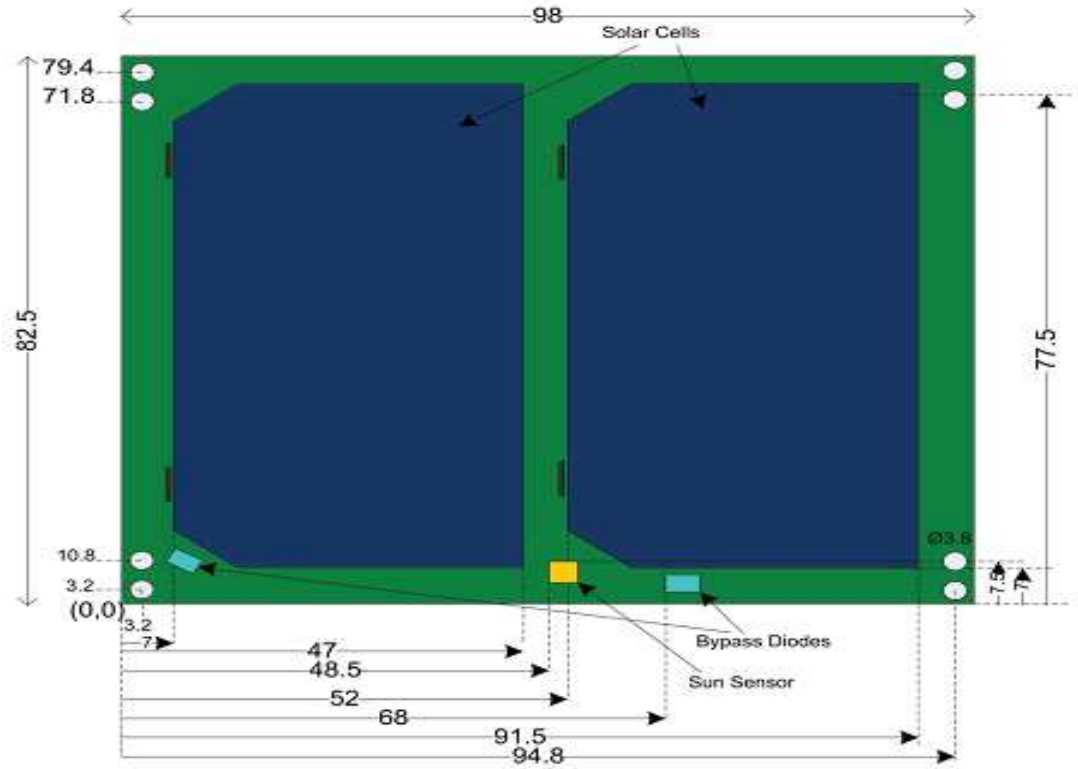
Figure 3.5: Cross sectional view of eight layers PCB of 1B8_CubePMT_1U

Parameter	Dimension	Unit
PCB dimension of 1B8_CubePMT_1U	$98.0 \times 82.5 \times 1.6$	mm^3
Total thickness of 1B8_CubePMT with components	9.15	mm
Mass of 1B8_CubePMT module	40	mm^3
Dimension of a single solar cell	$70 \times 40 \times 0.15$	mm
Height of Pico Blade Molex connector	4.7	mm
Height of Boost Converter inductor	7.5	mm
Height of Gyroscope	5.2	mm

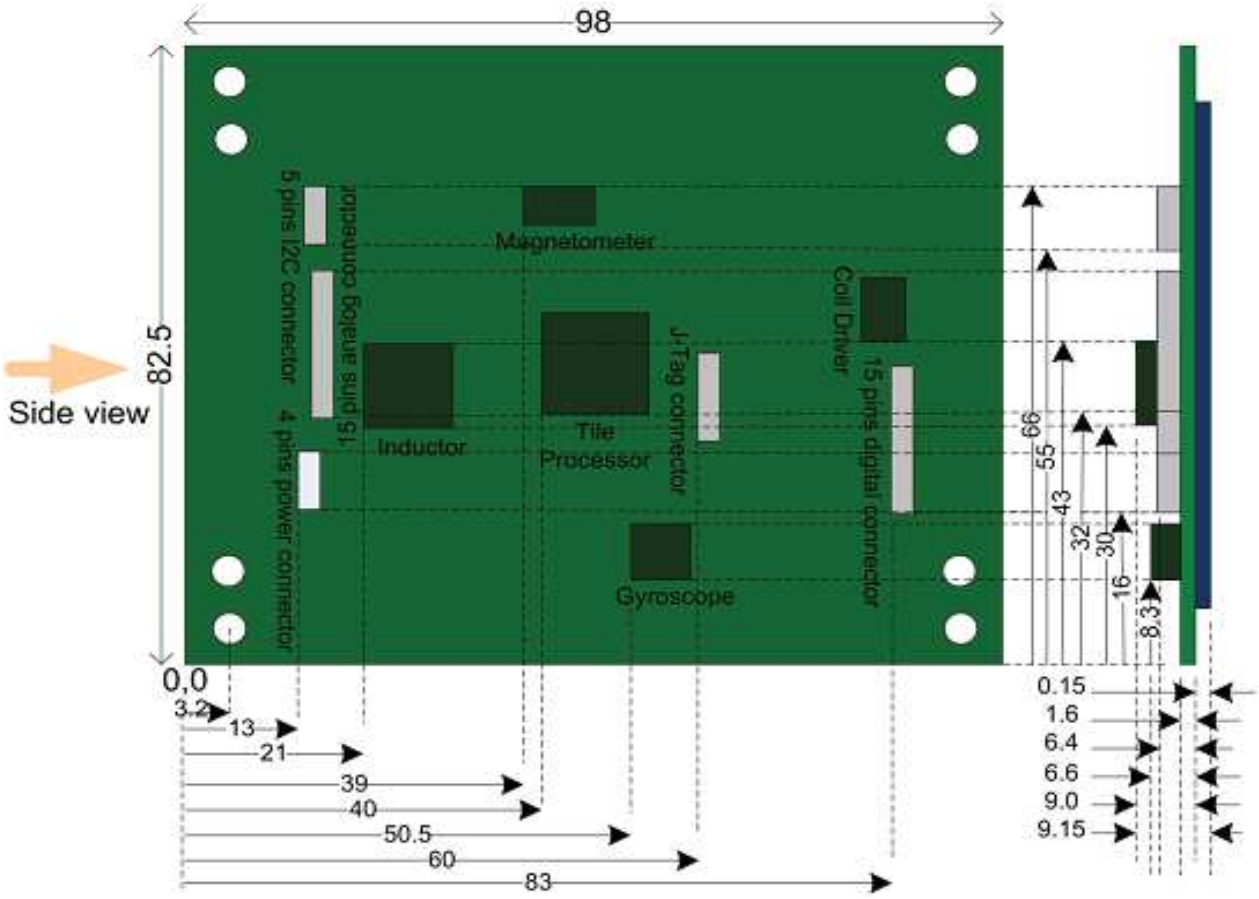
Table 3.1: 1B8_CubePMT_1U dimension.

3.2.3 Images of 1B8_CubePMT_1U with its dimensions:

The images of both sides of 1B8_CubePMT_1U tile are given below.



(a)



(b)

Figure 3.6: 1B8_CubePMT_1U dimensions (mm) (a) Solar panel side (b) component side.

3.3 1B8_CubePMT_3U:

1B8_CubePMT_3U is the development kit of 1B8_CubePMT_1U. The length of 3U is almost three times than 1B8_CubePMT_1U. It gives a large amount of space to put the extra component on the printed circuit board. In 1B8_CubePMT_3U, all the components are more or less the same as 1B8_CubePMT_1U except some additional components which need to be use according to the mission requirements and improvement of the system. Its distinguished features are given below.

- Instead of using two solar cells, it requires 6 solar cells. The reason is that 6 solar cells will generate 5.82W (13.2V and 0.4A) which has higher maximum power point than two cell that only has 1.76W (4.4V and 0.4A). Instead of using one temperature sensor, it requires two temperature sensors. The reason is that both of them have different range to sense the temperature.
- Instead of using one sun sensor, it requires two sun sensors. The reason is that if one sun sensor is damaged during the flight then there is back up for correct readings from the other sun sensor.
- Instead of using one processor, it requires two processors. One is use to process the 1B8_CubePMT subsystems while other is used to handle the other system of different board.

- Instead of using four connectors, it requires 4 additional 20 pin FRC module interface in order to co-operate with subsystem of another card.
- Instead of using 8 Donuts (5.5 mm) for connecting the tile across the rods by screw, it requires 24 Donuts (4.3 mm) for proper connection on the racks. The reason is that 3U tile is much longer than 1U and it supports better during the mission.

Its block diagram is shown in below figures 3.7.

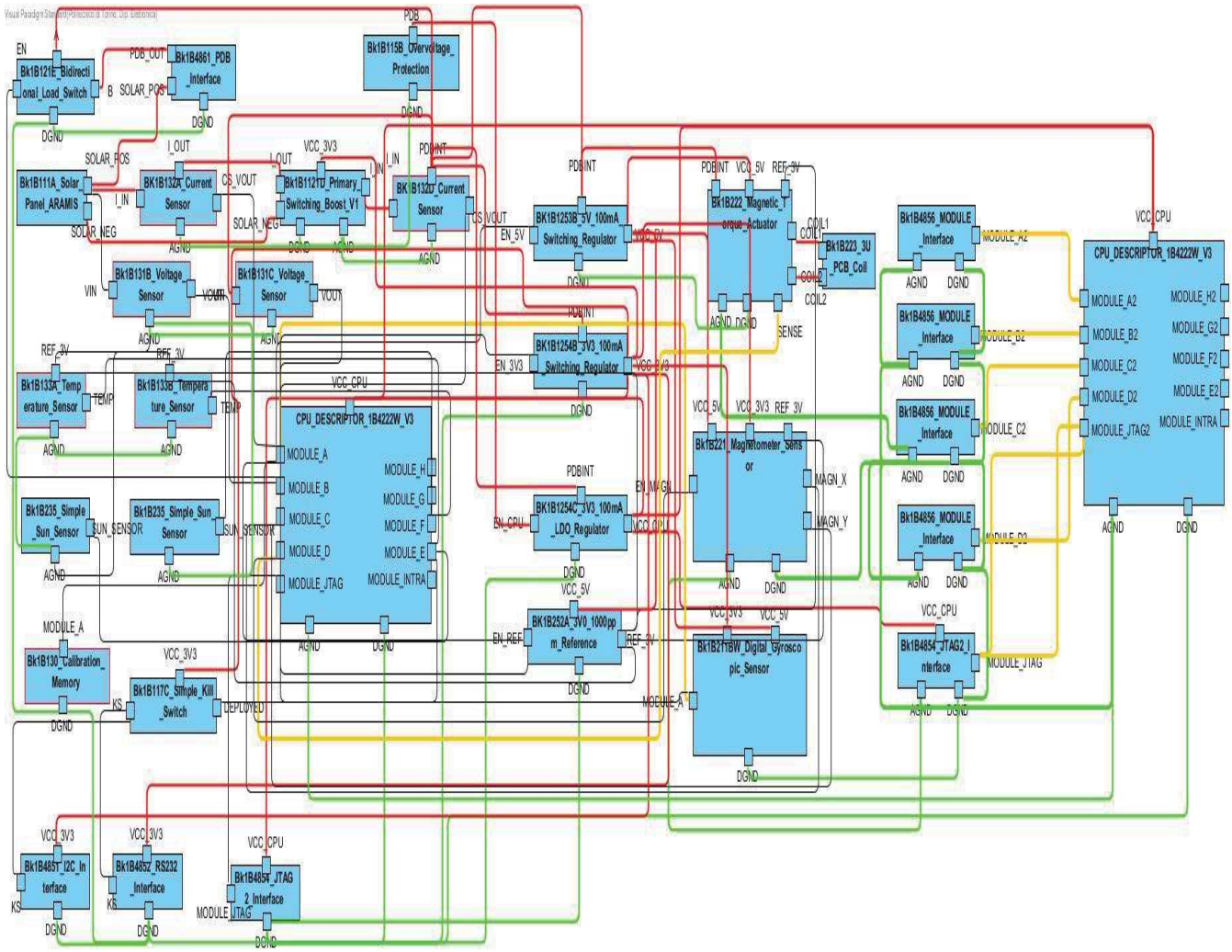


Figure 3.7: Block diagram of 1B8_CubePMT_3U.

3.3.1 Subsystems of 1B8_CubePMT_3U:

In 1B8_CubePMT_3U, almost all the components are same as 1B8_CubePMT_1U except some additional components which are newly added /replaced according to the mission requirement of the satellite. The 1B8_CubePMT_3U system can be further divided into seven subsystems which are explained below.

- **1B1 Power Generation and Storage:** It is used to generate energy, store it and manage it. It covers the subsystems including six cells Solar Panel (1B111A), PWM DC Converter (1B1122) and Over Voltage Protection (1B115B) and Boost Converter (1B1121D).

- **1B12 Power Distribution:** It is used to distribute the power for AraMiS. It covers the subsystems including two Linear Regulators (1B1252A and 1B1254C), two Switching Regulators (1B1253B and 1B1254B) and three Load Switches (1B121C, 1B121D and 1B121E).
- **1B13 Housekeeping Sensors:** It is used to control the power management subsystem. It covers the subsystems including two Current Sensors (1B132A and 1B132D), two Voltage Sensors (1B131B and 1B131C), two Temperature Sensors (1B133A) and Calibration Memory (1B130W).
- **1B21 Inertial Attitude Control:** It is used to control all the measurements related to Angular Velocity for AraMiS. It covers the subsystem including Gyroscope (1211B).
- **1B22 Magnetic Attitude Determination:** It is used to control all the measurements related to satellite orientation in the orbit and gives this information to on board processor. It covers the subsystems including Magnetometer Sensor (1B221), Magnetic Torque Actuator (1B222) and Magnetorquer Coil (1B223).
- **1B23 Other Attitude Control:** It is used to determine attitude parameter for AraMiS. It covers the subsystem including Sun Sensor (1B235).
- **1B4 Process and Module Interface:** It is used to manage and process for AraMiS and connect its subsystems with external interfaces. It covers the subsystems including two MSP430 Microcontrollers (1B4222), I2C Interface (1B4851), RS232 Interface (1B4852), JTAG interface (1B4854), PDB interface (1B4861) and Module Interface (1B4856).

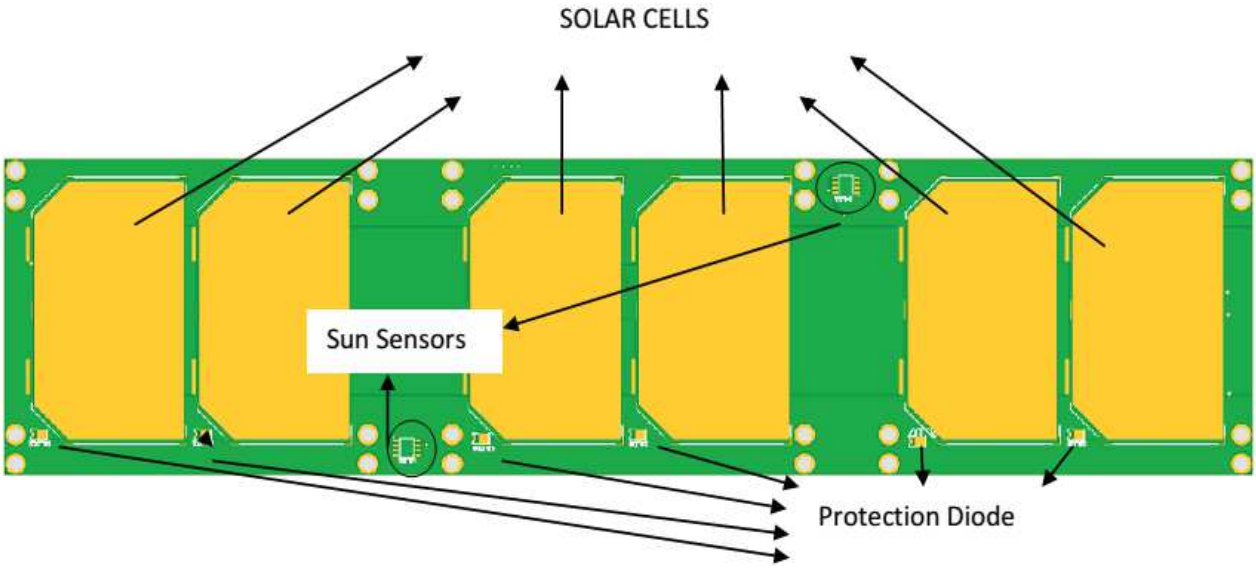


Figure 3.8: Diagram of the external background of 1B8_CubePMT_3U module.

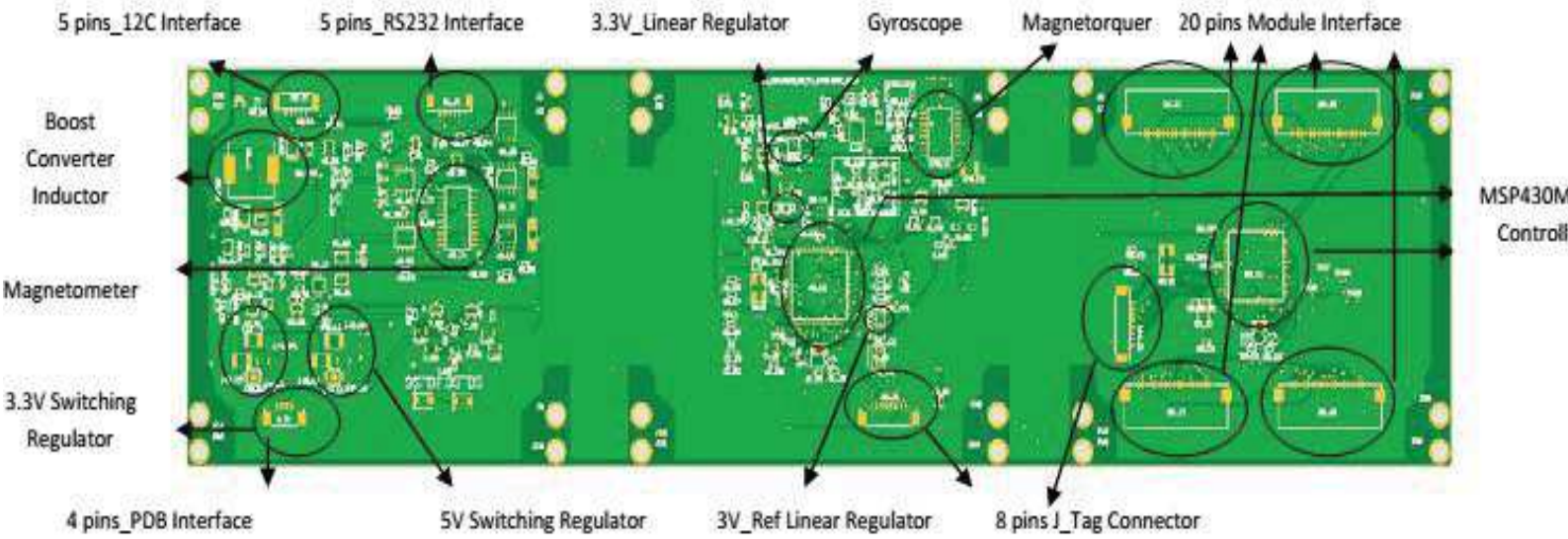


Figure 3.9: Diagram of internal background of 1B8_CubePMT_3U module.

3.3.2 Cross-Sectional view for PCB of 1B8_CubPMT_3U:

PCB of 1B8_CubePMT_3U is also divided into eight layers with dimensions equal to $324.9 \times 82.5 \times 1.6$ mm3. Two sun sensors are directly attached along with six solar cells that are attached to eighth layer of PCB with the help of resin. From layer four to layer seven contains 120 turns of magnetorquer coil. Second layer has the ground plane while the third layer has 3.3V plane because of more useful power. The first layer contains the PCB traces to connect all the components.

Above the PCB, there are two 15 pins connector that is use to contact the digital and analog signals of the systems. 20 pins Module Interface is used to connect external module (subsystem) to the tile processor for handling high power further subsystem to communicate with tile processor. There is 4 pins connector on the PCB that is reserved for the solar panel and PDB. Secondly an 8 pin J-tag interface is used to debug and program the tile processor. Lastly, 5 pins I2C and RS232 interface is used for connecting a tile with other tiles. Cross sectional view of 1B8_CubePMT_3U and its dimension are shown in below Figure3.10 and Figure3.11.

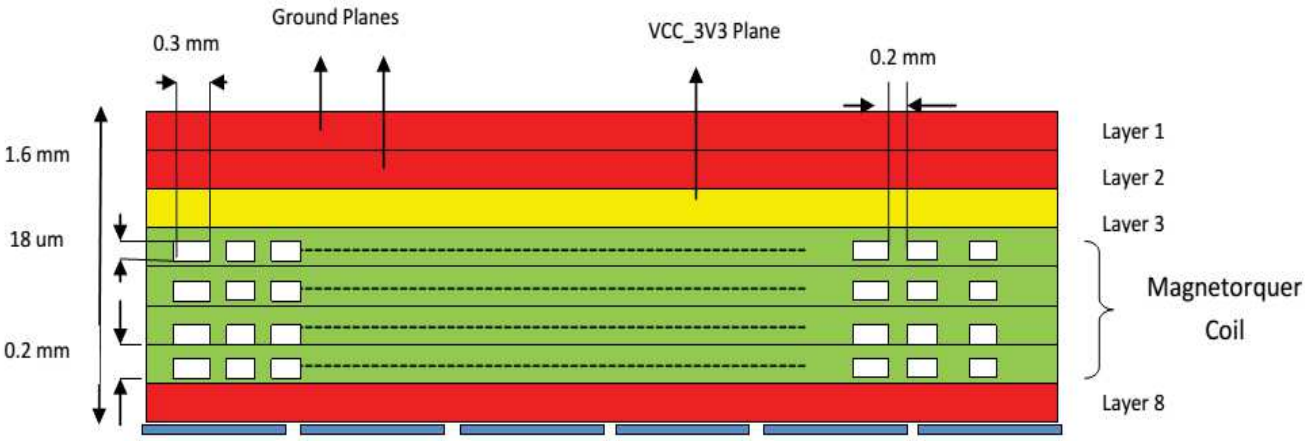


Figure 3.10: Cross sectional view of PCB

Parameter	Dimension	Unit
PCB dimension of 1B8_CubePMT MODULE	$324.9 \times 82.5 \times 1.6$	mm^3
Total thickness of 1B8_CubePMT_3U with components	10.2	mm
Mass of 1B8_CubePMT_3U	40	g
Dimension of a single solar cell	$70 \times 40 \times 0.15$	mm^3
Height of Pico Blade Molex connector	4.7	mm
Height of Boost Converter inductor	8	mm
Height of Gyroscope	0.85	mm

Table 3.2: 1B8_CubePMT_3U dimension.

3.4 1B4222 Tile Processor:

MSP430F5438 is a low power RISC microcontroller. It is usually placed at center of each tile of Aramis-C1 that support 25MHz system clock. It has seven modes that contain 1 active mode and the remaining 6 modes are used for low power. Each port is connected with sub components known as modules. The diagrams for the connection of modules with the subsystem are shown in below Figure 3.12:

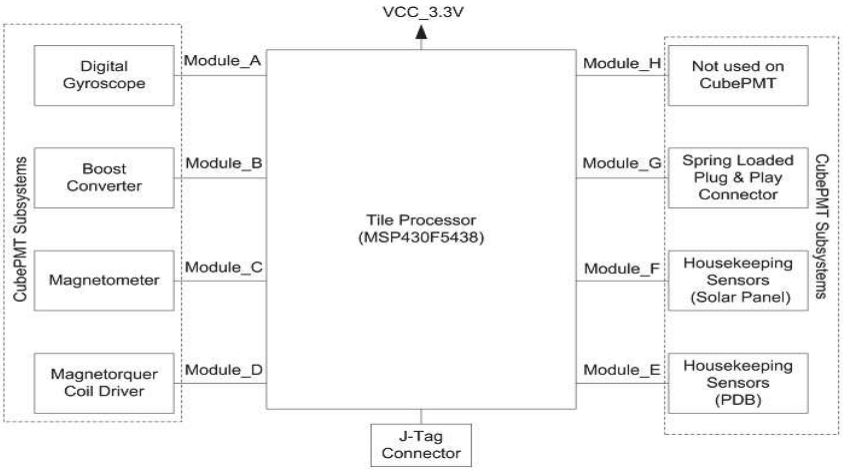


Figure 3.12: 1B8_CubePMT architecture with respect to Tile processor.

Its silent features are given below:

- Managing and processing the subsystem of both 1U and 3U for 1B8_CubePMT.
- Control the power consumption of the whole system.
- Taking the data from different sensors and give the command accordingly.
- Compile and Run the command for different subsystems.
- Communicating between tiles and recording the payload services with the help of I2C bus.

3.5 Data Interface

The data and power interface of 1B8_CuibePMT is very simple. It has nine different interfaces which are explained below:

- PDB Interface: It is a MOLEX-4 pins Pico Blade connector. On this connector solar panel output and PDB of the 1B8_CubePMT module are available. It is present on both 1U and 3U 1B8_CubePMT.
- I2C Interface: It is a MOLEX-5 pins Pico Blade connector. This connector has on-board data bus (I2C) and kills switch connection. A 3.3V supply is also available on this connector. It is present on both 1U and 3U 1B8_CubePMT.
- RS232 Interface: It is a MOLEX-5 pins Pico Blade connector. This connector has on-board data bus (RS232) and kills switch connection. A 3.3V supply is also available on this connector. It is present on both 1U and 3U 1B8_CubePMT.
- J-Tag Interface: It is a MOLEX-8 pins Pico Blade JTAG connector. This connector is used for programming and debugging purposes of the tile processor. It is present on both 1U and 3U 1B8_CubePMT.
- Analog Interface: It is a MOLEX-15 pins Pico Blade analog connector. All the analog signals of different sensors are available on this connector. A 5V supply and 3V reference supply are also available on this connector. It is present only on 1U 1B8_CubePMT.
- Digital Interface: It is a MOLEX-15 pins Pico Blade digital connector. This connector has all the critical digital signals for testing purposes. It is present only on 1U 1B8_CubePMT.
- Plug and Play Spring Loaded Interface: It is a 20 pins optional connector and an external module (subsystem) can be connected to the tile processor through this connector. It is present only on 1U 1B8_CubePMT.
- Module Interface: It is a Molex-20 pins FRC connector. This connector connect external module (subsystem) to the tile processor for handling high power. It is present only on 3U 1B8_CubePMT.

3.6 Providing Power for the subsystems of 1B8_CubePMT:

1B8_CubePMT generate power and distribute into four types of voltages which are used for its different subsystems. These 4 types of voltages are explained below.

- **14V PDB:**

In 1B8_CubePMT_1U, Boost Converter steps up the voltage from 4.4 V to 14 V PDB. The 14 Volt then go the bidirectional load switch as an input and this load switch give it to PDB interface. Batteries are charged from PDB and provide power to the1B8_CubePMT subsystems in the absence of solar power.

Similarly, it is necessary for the linear regulator (1B1254C), switching regulator (1B1253B, 1B1254B), high voltage load switch (1B121D) and operational amplifiers used in the current sensor.

- **5V Switching:**

One switching regulator (1B1253B) provides 5V to all the subsystems components. It is necessary for the driver, low voltage load switch, differential voltage sensor used in magnetic torque actuator,

for operational amplifiers, low voltage load switch used in magnetometer and for linear regulator (1B1252A).

- **3.3V Switching and Linear:**

One switching regulator (1B1254B) provides 3.3V to all the subsystem components except the tile processor (separate 3.3V regulator is used for tile processor). Secondly, One linear regulator (1B1254C) converts PDB voltage to 3.3V. This regulator gives supply to tile processor.

- **3V Reference:**

One linear regulator (1B1252A) converts 5V to 3V reference. It is necessary for temperature sensor, load switch in gyroscope, driver in magnetorquer actuator, operational amplifier in magnetometer.

Other than these voltages shown above, Power management tile provides the feed signals necessary for the entire BK1B4231 Onboard Computer and Image Processor. These four Voltage signals are necessary for the components of on board computer.

Chapter 4
Library for AraMiS

4.1 Introduction:

In this chapter we will discuss in detail the description, circuit diagram and Spice Netlist of all the subsystems of 1B8_CubePMT.

4.3 1B132 Current Sensor:

A current sensor is a device that detects electric current (AC or DC) in a wire, and generates a signal proportional to it. The generated signal could be analog voltage or current or even digital output. It can be then utilized to display the measured current in an ammeter or can be stored for further analysis in a data acquisition system or can be utilized for control purpose. The class diagram of 1B132 Current Sensor taken from visual paradigm is shown below in figure 4.1.

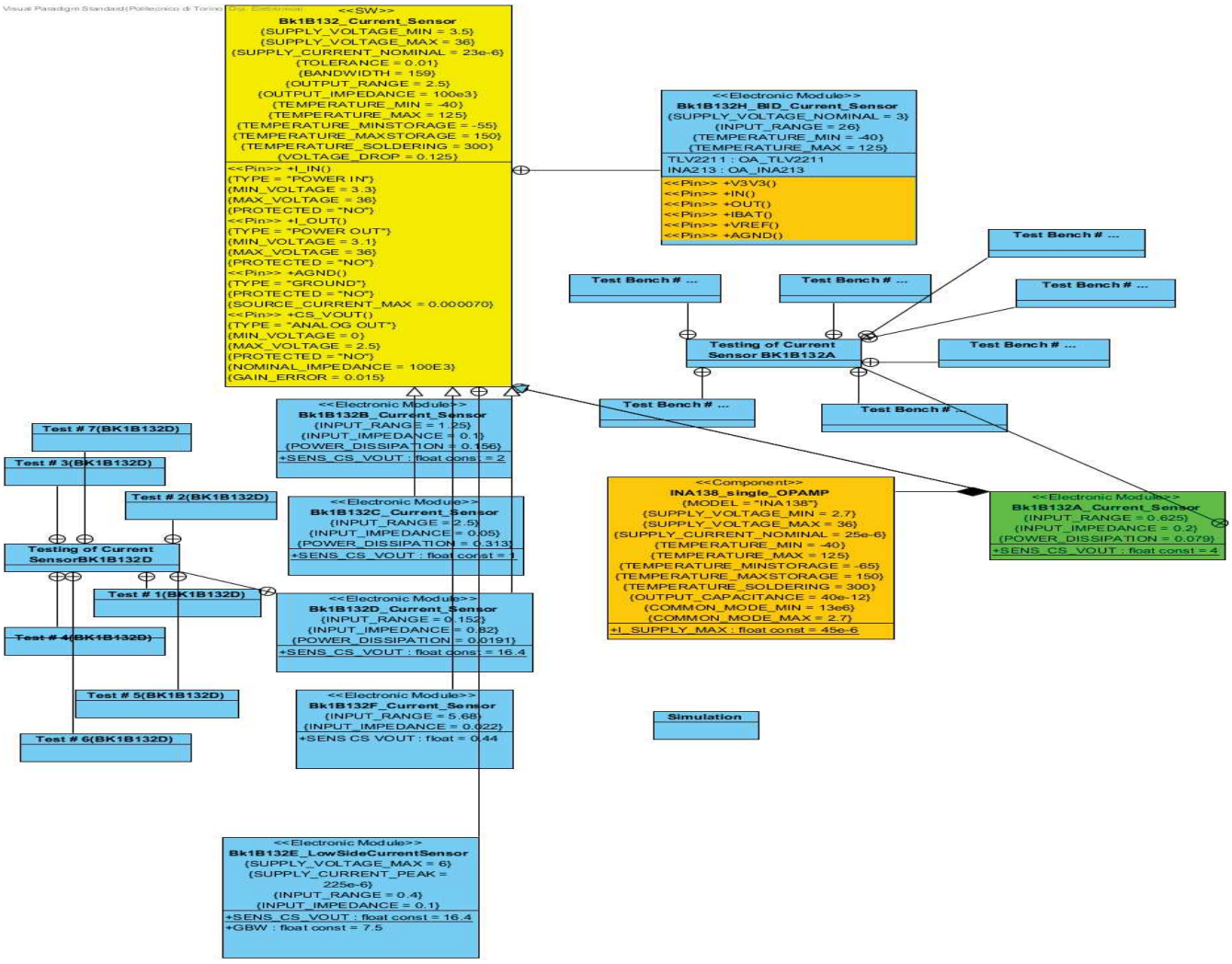


Figure 4.1: Class diagram of 1B132 Current Sensor

4.3.1 Description:

In both 1U and 3U 1B8_CubePMT, two high-side current sensors are used for an Aramis project. These current sensors convert positive current flowing from pin I_IN () to pin I_OUT () into an output voltage between pin CS_VOUT () and analog ground AGND (). Input current shall be in a range which depends on the specific specialization of Bk1B132_Current_Sensor (see tagged value INPUT_RANGE), while output voltage is in the range 0 to OUTPUT_RANGE.

The choice of INA138 device is dictated by the fact that it can limit the high current by making potential drop across a low valued series resistance. Differential input impedance between pins I_IN () and I_OUT () depends on the specialization and is given by tagged value INPUT_IMPEDANCE. Output impedance is common for all implementations (namely, OUTPUT_IMPEDANCE). It internally takes supply voltage from pin I_IN (), therefore input voltage on this pin shall be in range SUPPLY_VOLTAGE_MIN to SUPPLY_VOLTAGE_MAX. Supply current drawn from pin I_IN () to AGND () is given by SUPPLY_CURRENT_NOMINAL. It also contains a first order low-pass filter with cutoff frequency given by BANDWIDTH. Most performance is defined by tagged values. Output voltage is calculated as given by

$$V\ (\text{CS\_VOUT}\ ()) = I\ (\text{I\_IN}\ ()) * \text{SENS\_CS\_VOUT}$$

Where I (I_IN ()) is the current entering from pin I_IN () and exiting I_OUT (), while SENS_CS_VOUT depends on the specialization of Bk1B132_Current_Sensor.

The schematic diagram of BK1B132A current sensors is given blow in figure 4.2.

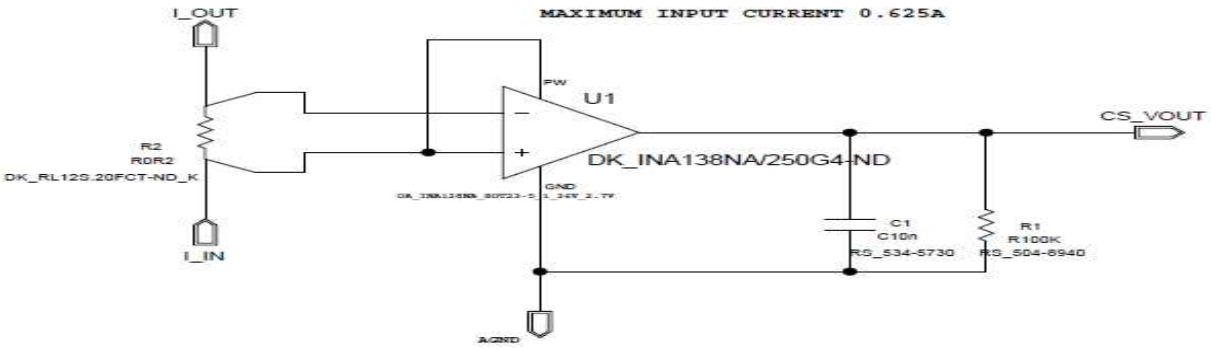


Figure 4.2: Schematic diagram of Bk1B132A_Current_Sensor

4.3.2 Testing of BK1B132A_Current Sensor

Testing Results of Bk1B132A_Current _Sensor are shown below.

Serail #	Parameters	Expected Value	Current Result	Verification	Pass/Fail	Test bench
1	Temperature (Centigrade)	-40 to 125	-35 to 125	-35:CS_VOUT=2.48V 125:CS_VOUT=2.55V	Fail	Test#7
2	Output Voltage (V)	2.5	With no load:2.5 With load(R=100K):1.25	Vo=I_sense*R_sense*R_out/5k=2.5	Pass	TEST#1
3	Tolerance (%)	1	1.3	Output Range:1.410-1.449 T=0.0195/1.4295=0.013=1.3%	Fail	Test#2
4	Input Voltage (V)	Min=3.3 Max=36	Min=3.3 Max=36	CS_VOUT=2.5V	Pass	Test#4
5	Input Impedance(Zin)	200mohm	200mohm	V(i_in)-V(i_out)/I*(1i195:2)=200mohm	Pass	Test#5
6	Output Impedance(Zo)	Same as current result	(RL=100K) -------->Zo=50K	VL/VNL=RL/(RL+Zo)=0.5	Pass	Test#6
7	Input Current(A)	Same as current result	Min:0 Max:0.625	CS_VOUT:2.5	Pass	TEST#8

Pin I_IN ():

Serial #	Parameter	Expected Value	Current Result	Verification	Pass/Fail	Test bench
1	Minimum input Voltage	3.3	3.3	CS_VOUT=2.5V	Pass	Test#4
2	Maximum input Voltage	36	36	CS_VOUT=2.5V	Pass	Test#4

Pin I_OUT ():

Serial #	Parameter	Expected Value	Current Result	Verification	Pass/Fail	Test bench
1	Minimum input Voltage	3.1	3.1	CS_VOUT=2.5V	Pass	Test#4
2	Maximum input Voltage	36	36	CS_VOUT=2.5V	Pass	Test#4

Pin AGND ():

Serial #	Parameter	Expected Value	Current Result	Verification	Pass/Fail	Test bench
1	Maximum Supply Current(uA)	70 uA	72.8uA	1)Ix(1i195:4)+Ix(1i183:OUT)=0.000072A 2)25uA+45uA=70A as expected	Fail	Test#3

Pin CS_VOUT ():

Serial #	Parameter	Expected Value	Current Result	Verification	Pass/Fail	Test bench
1	Min Output Voltage	0	0	CS_VOUT=0	Pass	Test#1
2	Maximum Output Voltage	2.5	2.5	CS_VOUT=2.5	Pass	Test#1
3	Nominal	100K	100K	RL=100K	Pass	Test#6

	Impendence					

- ## Test Bench # 1(BK1B132A)

This test is used to measure the output of current sensor with respect to input. Here the dc current is given as an input and we calculated the voltage across the sink. The current is measured across the resistor placed in series between the input and the output pin of the INA138 by making its voltage difference. This voltage difference is subsequently sent to ADC of the microcontroller that must be compatible with the converter. After sensing the potential difference across the resistor, the output voltage goes to the rest of the blocks. Below, I have attached the sim_adms file that represents how to test the output/input relationship of current sensor in LT-Spice.

```
.dc IOUT 0 0.625 0.1
.include "..\..\genhdl\Bk1B132A_Current_Sensor_V1\Bk1B132A_Current_Sensor_V1.spi"
VGround AGND 0 DC 0
VIN I_IN 0 DC 36
IOUT I_OUT 0 DC 1

******end of additional commands*******
.end
```

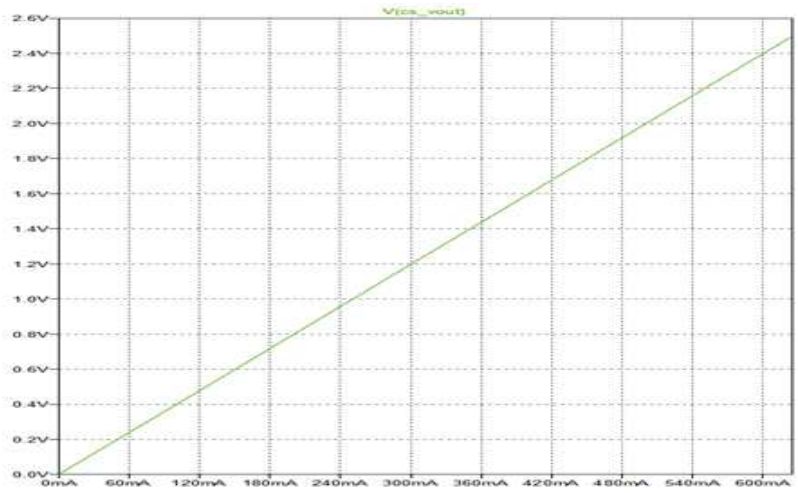


Figure 4.3: Output Vs Input of Bk1B132A_Current_Sensor

Above is the plot of current sensor whose maximum current limits 625mA. Here, the output voltage obtained is compatible to the previous theoretical results.

- ## Test Bench # 2(BK1B132A)

This test is used to apply a Montecarlo approach in order to evaluate the error introduced by the manufacturing tolerances of the resistors in the main circuit. For this, zoom in the output voltage (CS_VOUT) plot and observed the range of output value in which select only those lines which are nearer to each other and then apply the standard deviation formula in order to approximate the tolerance. We will find their tolerances respectively. Below, I have attached the sim_adms file that represents how to test the tolerance of this current sensor in LT-Spice.

```
.dc IIOUT 0 0.625 0.1
.step param run 1 100 1
.include "..\..\genhdl\Bk1B132A_Current_Sensor_V1\Bk1B132A_Current_Sensor_V1.spi"
VIN I_IN 0 DC 36
IIOUT I_OUT 0 DC 0.625
VGround AGND 0 DC 0
*******end of additional commands********
.end
```

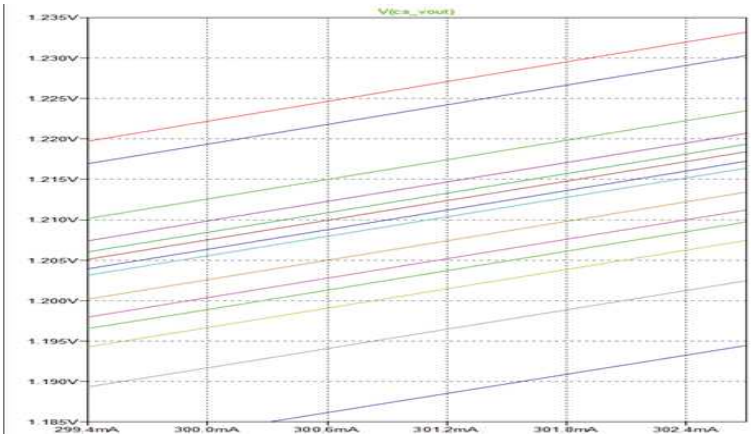


Figure 4.3: Tolerance of Bk1B132A_Current_Sensor

Output voltage range for this current sensor is from 1.410V to 1.449V.So, its tolerance become

Tolerance =0.013=1.3%

The obtained uncertainty is about 0.3% that is considered to be negligible.

- ## Test Bench # 3(BK1B132A)

This test is used to measure the maximum supply current across the circuit. For this, sink current flow across the load resistance and the ground. In simulation of both current sensors, we will get more or less the same value of sink current that is 50uA. Below, I have attached the sim_adms file that represents how to test the maximum supply current of this current sensor in LT-Spice.

```
.tran 0.001 100m 0
.include "..\..\genhdl\Bk1B132A_Current_Sensor_V1\Bk1B132A_Current_Sensor_V1.spi"
VIN I_IN 0 DC 36
IIOUT I_OUT 0 DC 0.625
VGround AGND 0 DC 0
RLoad CS_VOUT 0 100K
*******end of additional commands********
.end
```

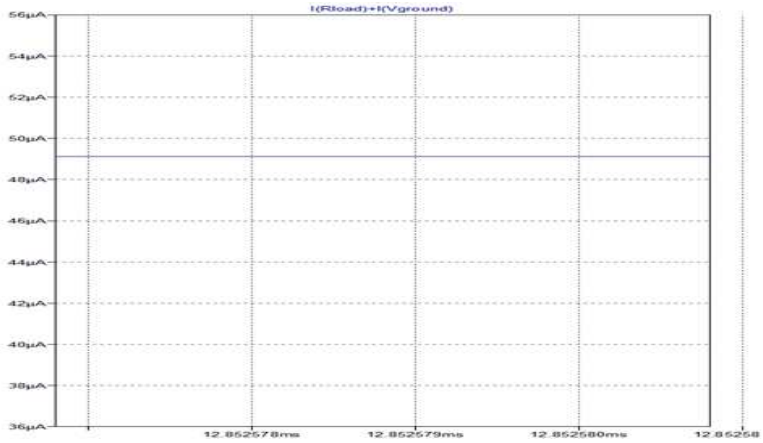


Figure 4.4: Maximum Supply Current of Bk1B132A_Current_Sensor

The expected value of maximum supply current is calculated as.

25uA (flow across LOAD) +45uA (flow across GND) =70uA

There is 20uA difference between expected value and simulated value.

- ## Test Bench # 4(BK1B132A)

This test is measured between input and output voltage. For both current sensors we got exactly 2.5V as we increase the input voltage. Below, I have attached the sim_adms file that represents how to test the input and output voltage of this current sensor in LT-Spice.

```
.dc VIN 0 36 0.1
.include "..\..\genhdl\Bk1B132A_Current_Sensor_V1\Bk1B132A_Current_Sensor_V1.spi"
VIN I_IN 0 PULSE (1 40 0.1U 500M )
VGround AGND 0 DC 0
IIOUT I_OUT 0 DC 0.625
*******end of additional commands********
.end
```

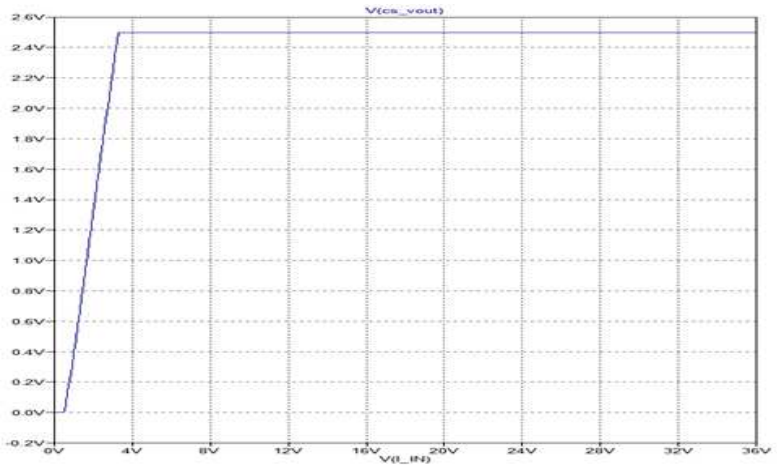


Figure 4.5: Output voltage Vs Input voltage of Bk1B132A_Current_Sensor

- ## Test Bench # 5(BK1B132A)

This test is used to measure the input impedance of current sensor across four wire resistor. The reason to measure across this four wire resistor is that the equivalent resistance between two parallel resistors is usually a low valued resistor where current easily pass through it. Below, I have attached the sim_adms file that represents how to test the input impedance of this current sensor in LT-Spice.

```
.dc IIOUT 0 0.625 0.1
.include "..\..\genhdl\Bk1B132A_Current_Sensor_V1\Bk1B132A_Current_Sensor_V1.spi"
VGround AGND 0 DC 0
VIN I_IN 0 DC 36
IIOUT I_OUT 0 DC 0.625
*******end of additional commands********
.end
```

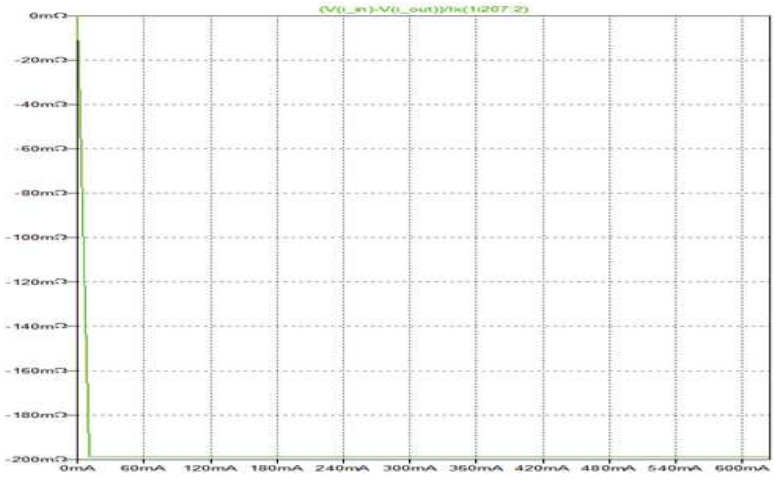


Figure 4.6: Input Impedance of Bk1B132A_Current_Sensor

- **Test Bench # 6(BK1B132A)**

This test is used to measure the output impedance of current sensor in the presence of load resistance (100 KΩ) where current easily pass through it. Below, I have attached the sim_adms file that represents how to test the output impedance of this current sensor in LT-Spice.

```
.tran 0.001 100m 0
.include "..\..\genhdl\Bk1B132A_Current_Sensor_V1\Bk1B132A_Current_Sensor_V1.spi"
VIN I_IN 0 DC 36
IIOUT I_OUT 0 DC 0.625
VGround AGND 0 DC 0
RLoad CS_VOUT 0 100K
*******end of additional commands********
.end
```

Figure 4.7: Output Impedance of Bk1B132A_Current_Sensor

Here is the way to verify the output impedance shortly.

$$VL/VNL = RL/ (RL+Zo) = 0.5$$

- **Test Bench # 7(BK1B132A)**

This test is used to measure the change of output voltage by changing the temperature. Below, I have attached the sim_adms file that represents how to test the output voltage by changing the temperature in LT-Spice.

```
.DC TEMP -35 125 5
.include "..\..\genhdl\Bk1B132A_Current_Sensor_V1\Bk1B132A_Current_Sensor_V1.spi"
V_IN I_IN 0 DC 36
VGND AGND 0 DC 0
I_OUT I_OUT 0 DC 0.625
*******end of additional commands********
.end
```

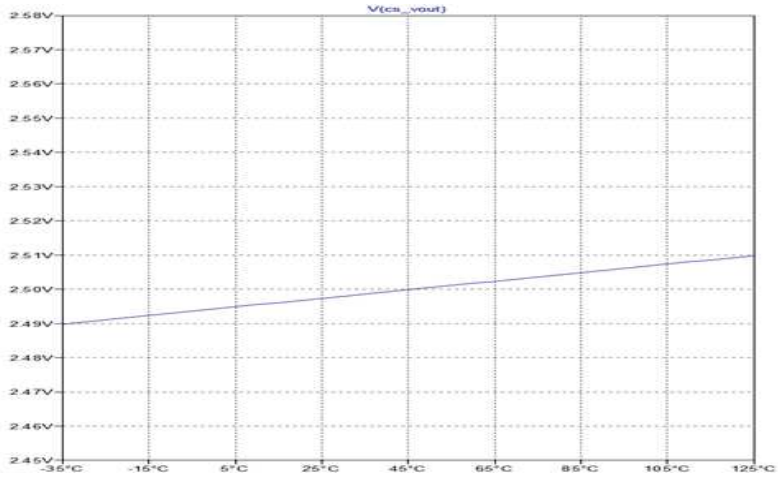


Figure 4.8: Temperature VS output voltage Bk1B132A_Current_Sensor

Here is mentioned the maximum and minimum temperature effect on the output voltage.

-35°C: CS_VOUT=2.48V

125°C: CS_VOUT=2.55V

4.3.3 Spice Netlist of BK1B132A_Current_Sensor:

Once the schematic is created, it is netlisted in the Design Capture of the Mentor Graphics (Simulation→Netlist). It generates a spice netlist which can be used for simulating in the LTSpice. Here I have attached the genhdl file that shows all the components of this voltage sensor and how they are connected in the schematic.

```
* Project Bk1B132A_Current_Sensor_V1
* Mentor Graphics Wirelist Created with Version 6.4.002
* File created Wed Nov 30 13:32:58 2016
* Inifile   :
* ConfigFile:  C:\MentorGraphics\7.9.4EE\SDD_HOME\standard\wspice.cfg
* Options   :  -__ -.spi -h -$ -7 -kC:\MentorGraphics\7.9.4EE\SDD_HOME\standard\wspice.cfg bk1b132a_current_sensor_v1
* Levels    :
*
C11229 CS_VOUT AGND {MC( 0.01uF , 10.000000 /100)} TC=10.000000U
X11251 XSIG010025 XSIG010024 XSIG010025 AGND CS_VOUT INA138
R11219 CS_VOUT AGND {MC( 100Kohms , 1000.000000M /100)} TC=100.000000U
X11263 I_IN I_OUT XSIG010025 XSIG010024 RES_4WIRE R={MC(200Mohms,1000.000000M/100)} TC=200.000000U
* Dictionary 0
*Warning : No ground node (Label a net GND)

.include "..\..\genhdl\Bk1B132A_Current_Sensor_V1\Bk1B132A_Current_Sensor_V1_sources.spi"
.include "..\..\sym\INA138.mod"
.include "..\..\sym\RES_4WIRE.mod"
```

4.4 Voltage Sensor:

A voltage divider (also known as a potential divider) is a passive linear circuit that produces an output voltage (V_{out}) that is a fraction of its input voltage (V_{in}). Voltage division is the result of distributing the input voltage among the components of the divider. A simple example of a voltage divider is two resistors connected in series, with the input voltage applied across the resistor pair and the output voltage emerging from the connection between them.

The class diagram of 1B132 Current Sensor taken from visual paradigm is shown below in figure 4.9.

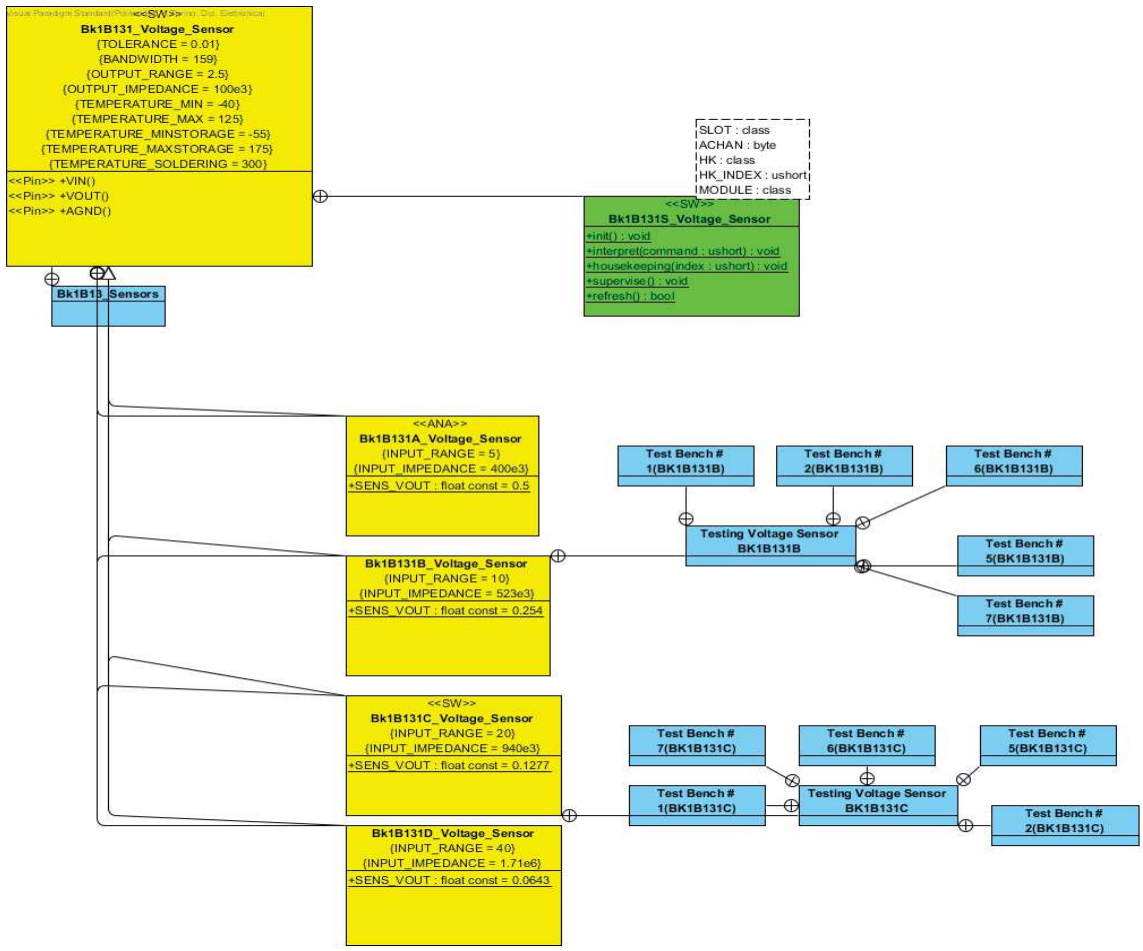


Figure 4.9: Class diagram of 1B131 Voltage Sensor

4.3.1 Description:

In both 1U and 3U 1B8_CubePMT, two voltage sensors are used for an Aramis project. The voltage sensors convert (through a voltage divider) the input voltage between input pin VIN () and analog ground AGND () to an output voltage between pin VOUT () and analog ground AGND (). Input voltage shall range between 0 and a maximum value which depends on the specific specialization of Bk1B131_Voltage_Sensor (see tagged value INPUT_RANGE), while output voltage is in the range 0 to OUTPUT_RANGE. Output impedance is common for all implementations (namely, OUTPUT_IMPEDANCE).

It also contains a first order low pass filter with cutoff frequency BANDWIDTH. It requires no supply voltage. Most performance is defined by tagged values. Output impedance is high. This must be taken into account during sample and hold phase.

Theoretical verification of analog output voltage (Vout) of voltage sensor connected to ADC of tile processor, are given below.

$$V_{out} = V_{in} \times \frac{R_{17}}{R_{17} + R_{29}}$$

Its schematic diagram is shown in figure below 4.10.

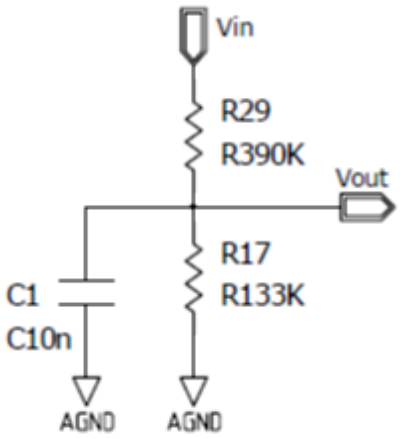


Fig 4.10: Schematics of a Bk1B131B_Voltage_Sensor.

4.3.2 Testing of Voltage Sensor BK1B131B

Testing Results of Bk1B131B_Voltage_Sensor are shown below.

Serial #	Parameter	Expected Value	Current Result	Verification	Pass/Fail	Test bench
1	Temperature (Centigrade)	-40 to 125	-40 to 125	-40:Vout=2.49V **125:**Vout=2.5V	Pass	Test#7
2	Output Voltage (V)	2.5	With no load:2.5 With load(R=100K):1.25	Vout=Vin*R17/(R17+R29)=2.5	Pass	TEST#1
3	Tolerance (%)	1	0.37	Output Range:2.412-2.430 T=0.009/2.421=0.0037=0.37%	Fail	Test#2
4	Input Voltage (V)	Vin=10	Vmin=2------>Vout=0.5 Vmax=10------>Vout=2.5	Vout=2.5V for 10 volt input	Pass	Test#4
5	Input Impedance(kohm)	523	522.7	V(vin)/I(R1i116)=522.7	Pass	Test#5
6	Output Impedance(Zo)	100K	(RL=100K)------>Zo=50K	VL/VNL=RL/(RL+Zo)=0.5	Pass	Test#6

Pin VIN ():

Serial #	Parameter	Expected Value	Current Result	Verification	Pass/Fail	Test bench
1	Minimum input Voltage	2	2	Vout=0.5V	Pass	Test#4
2	Maximum input Voltage	10	10	Vout=2.5V	Pass	Test#4

Pin AGND ():

Serial #	Parameter	Expected Value	Current Result	Verification	Pass/Fail	Test bench
1	Maximum Input Current(uA)	102.5	12.5	I(C1i97)+I(R)=0.0000125 or 10/97.5K=102.5 as expected	Fail	Test#3

Pin VOUT ():

Serial #	Parameter	Expected Value	Current Result	Verification	Pass/Fail	Test bench
1	Min Output Voltage	0.5	0.5	VOUT=0.5 for 2V input	Pass	Test#1
2	Maximum Output Voltage	2.5	2.5	VOUT=2.5 for 10V input	Pass	Test#1
3	Nominal Impendence	100K	100K	RL=100K	Pass	Test#6

- ## Test Bench # 1(BK1B131B)

This test is used to measure the output of voltage sensor with respect to input voltage. Here the dc voltage is given as an input and we calculated the voltage across the output terminal. Below,I have attached the sim_adms file that represent how to test the output of this voltage sensor in LT-Spice.

```
.tran 0 1 0.1
.include "..\..\genhdl\Bk1B131B_Voltage_Sensor_V1\Bk1B131B_Voltage_Sensor_V1.spi"
VGND AGND 0 DC 0
VVIN VIN 0 PULSE (0 10 0.1U 500M)
*******end of additional commands********
.end
```

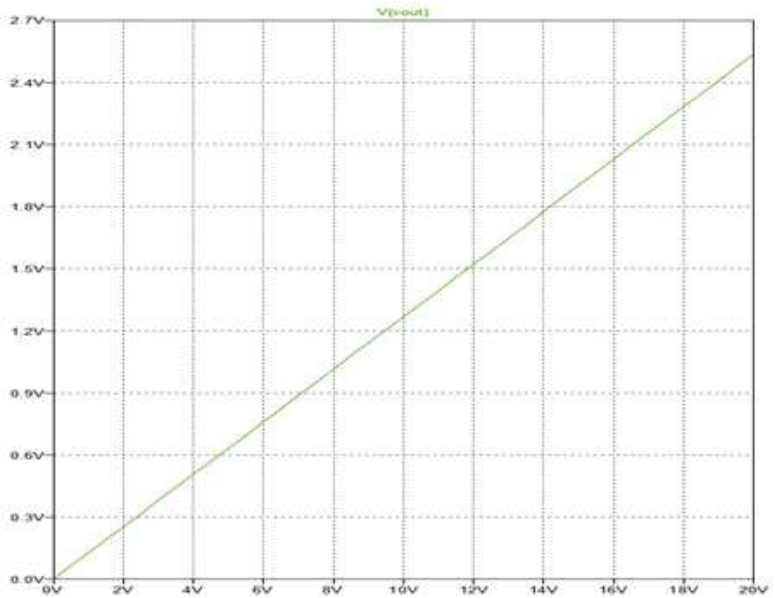


Fig 4.11: Output Vs Input of Bk1B131B_Voltage_Sensor.

Above is the plot of current sensor whose maximum current limits 625mA. Here, the output voltage obtained is compatible to the previous theoretical results.

- **Test Bench # 2(BK1B131B)**

This test is used to apply a Montecarlo approach in order to evaluate the error introduced by the manufacturing tolerances of the resistors in the main circuit. For this, zoom in the output voltage VOUT plot and observed the range of output value in which select only those lines which are nearer to each other and then apply the standard deviation formula in order to approximate the tolerance. We will find their tolerances respectively. Below, I have attached the sim_adms file that represents how to test the tolerance of this voltage sensor in LT-Spice.

```
.tran 0 1 0.1
.include "..\..\genhdl\Bk1B131B_Voltage_Sensor_V1\Bk1B131B_Voltage_Sensor_V1.spi"
VGND AGND 0 DC 0
VVIN VIN 0 PULSE (0 15 0.1U 500M)
*******end of additional commands*******
.end
```

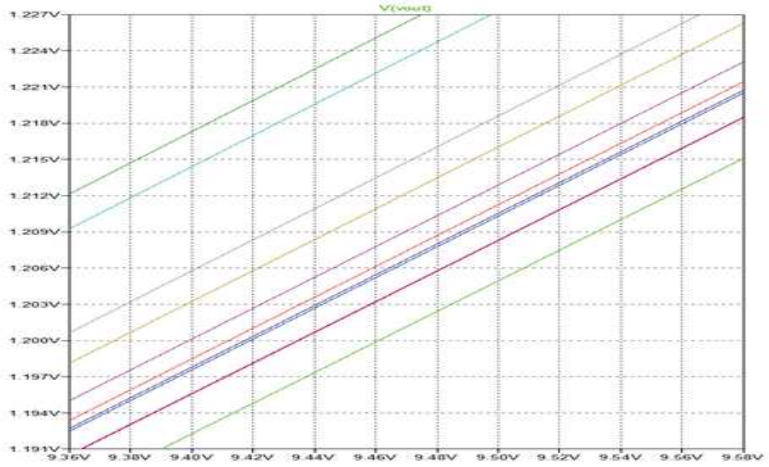


Fig 4.12: Tolerance of Bk1B131B_Voltage_Sensor

Output Voltage Range for this voltage sensor: 2.412V<------->2.430V

$$\text{Tolerance} = \frac{0.009}{2.421} = 0.0037 = 0.37\%$$

The obtained uncertainty is about 0.93%, which we considered it negligible.

- **Test Bench # 5(BK1B131B)**

This test is used to measure the input impedance of voltage sensor. Below, I have attached the sim_adms file that represents how to test the input impedance of this voltage sensor in LT-Spice.

```
.tran 0 1 0.1
.include "..\..\genhdl\Bk1B131B_Voltage_Sensor_V1\Bk1B131B_Voltage_Sensor_V1.spi"
VGND AGND 0 DC 0
R Vout 0 100K
VVIN VIN 0 PULSE (0 10 0.1U 500M)
*******end of additional commands********
.end
```

Fig 4.13: Input Impedance of Bk1B131B_Voltage_Sensor

Here is the way to verify the input impedance during simulation.

$$\frac{V(vin)}{I(R1i116)} = 522.7\Omega \quad \text{(Expected = 523}\Omega\text{)}$$

- ## Test Bench # 6(BK1B131B)

This test is used to measure the output impedance of current sensor in the presence of load resistance (100 KΩ) where current easily pass through it. Below, I have attached the sim_adms file that represents how to test the output impedance of this current sensor in LT-Spice.

```
.tran 0 1 0.1
.include "..\..\genhdl\Bk1B131B_Voltage_Sensor_V1\Bk1B131B_Voltage_Sensor_V1.spi"
VGND AGND 0 DC 0
R Vout 0 100K
VVIN VIN 0 PULSE (0 10 0.1U 500M)
*******end of additional commands********
.end
```

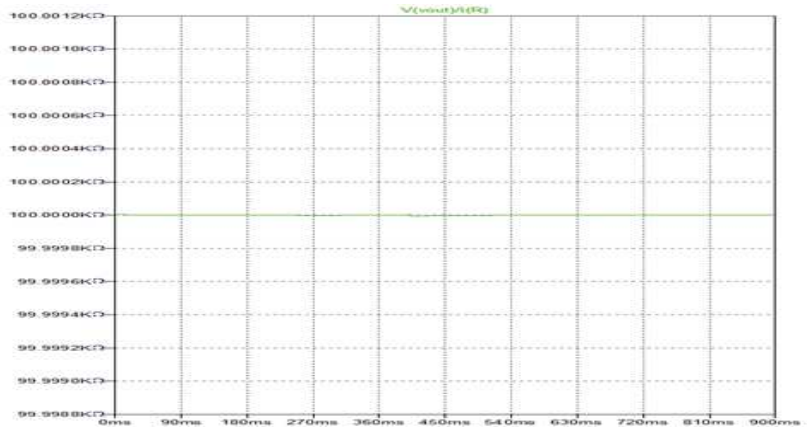


Fig 4.14: Output Impedance of Bk1B131B_Voltage_Sensor

Here is the way to verify the output impedance shortly

VL/VNL=RL/ (RL+Zo) =0.5

- **Test Bench # 7(BK1B131B)**

This test is used to measure the change of output voltage by changing the temperature .Below; I have attached the sim_adms file that represents how to test the output voltage by changing the temperature in LT-Spice.

```
.dc TEMP -140 125 5
.include "..\..\genhdl\Bk1B131B_Voltage_Sensor_V1\Bk1B131B_Voltage_Sensor_V1.spi"
VGND AGND 0 DC 0
VVIN VIN 0 DC 10
*******end of additional commands*******
.end
```

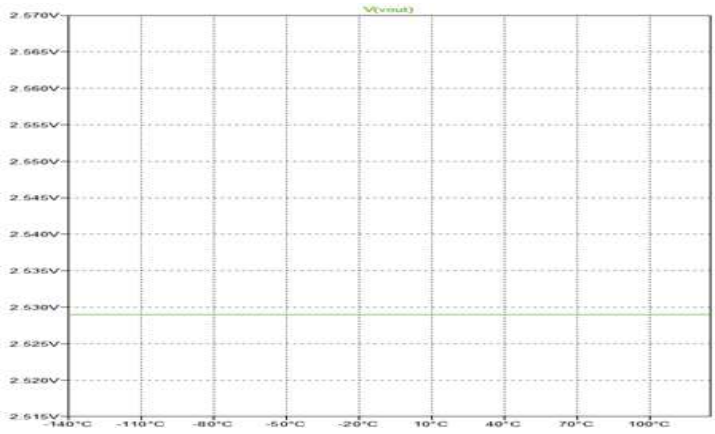


Fig 4.15: Temperature Vs Output Voltage of Bk1B131B_Voltage_Sensor

Here we will mention the maximum and minimum temperature effect on the output voltage.

-40: CS_VOUT=2.528V

125: CS_VOUT=2.528V

4.3.3 Spice Netlist of BK1B131B_Voltage_Sensor:

Once the schematic is created, it is netlisted in the Design Capture of the Mentor Graphics (Simulation→Netlist). It generates a spice netlist which can be used for simulating in the LTSpice as shown below. Here I have attached the genhdl file that shows all the components of this voltage sensor and how they are connected in the schematic.

```
* Project Bk1B131B_Voltage_Sensor_V1
* Mentor Graphics Netlist Created with Version 6.4.002
* File created Wed Nov 30 13:38:28 2016
* Inifile   :
* ConfigFile:  C:\MentorGraphics\7.9.4EE\SDD_HOME\standard\wspice.cfg
* Options   :  -__ -.spi -h -$ -7 -kC:\MentorGraphics\7.9.4EE\SDD_HOME\standard\wspice.cfg bk1b131b_voltage_sensor_v1
* Levels    :
*
C1I126 Vout AGND {MC( 10.000000N , 10.000000 /100)} TC=10.000000U
R1I136 Vin Vout {MC( 390Kohms , 1000.000000H /100)} TC=100.000000U
R1I146 Vout AGND {MC( 133Kohms , 1000.000000H /100)} TC=100.000000U
* Dictionary 0
*Warning : No ground node (Label a net GND)

.include "..\..\genhdl\Bk1B131B_Voltage_Sensor_V1\Bk1B131B_Voltage_Sensor_V1_sources.spi"
```

4.4 1B1122 PWM DC Converter:

PWM DC Converter contains passive components including resistors, capacitors and schottky diodes. This converter usually gives the constant output voltage that plays a major role in our designed Boost Converter. For the inverting input voltage of a comparator U7 (part of Boost Converter), a PWM-DC-converter block is used in order to set a reference voltage at the inverting terminal of U7. In our case, it gives 2.83 V at the output terminal (DC_OUT) for the input voltage is 3.6V. The class diagram of PWM DC converter Bk1B1122_PWM_DC_Converter is shown in below Figure 4.16.

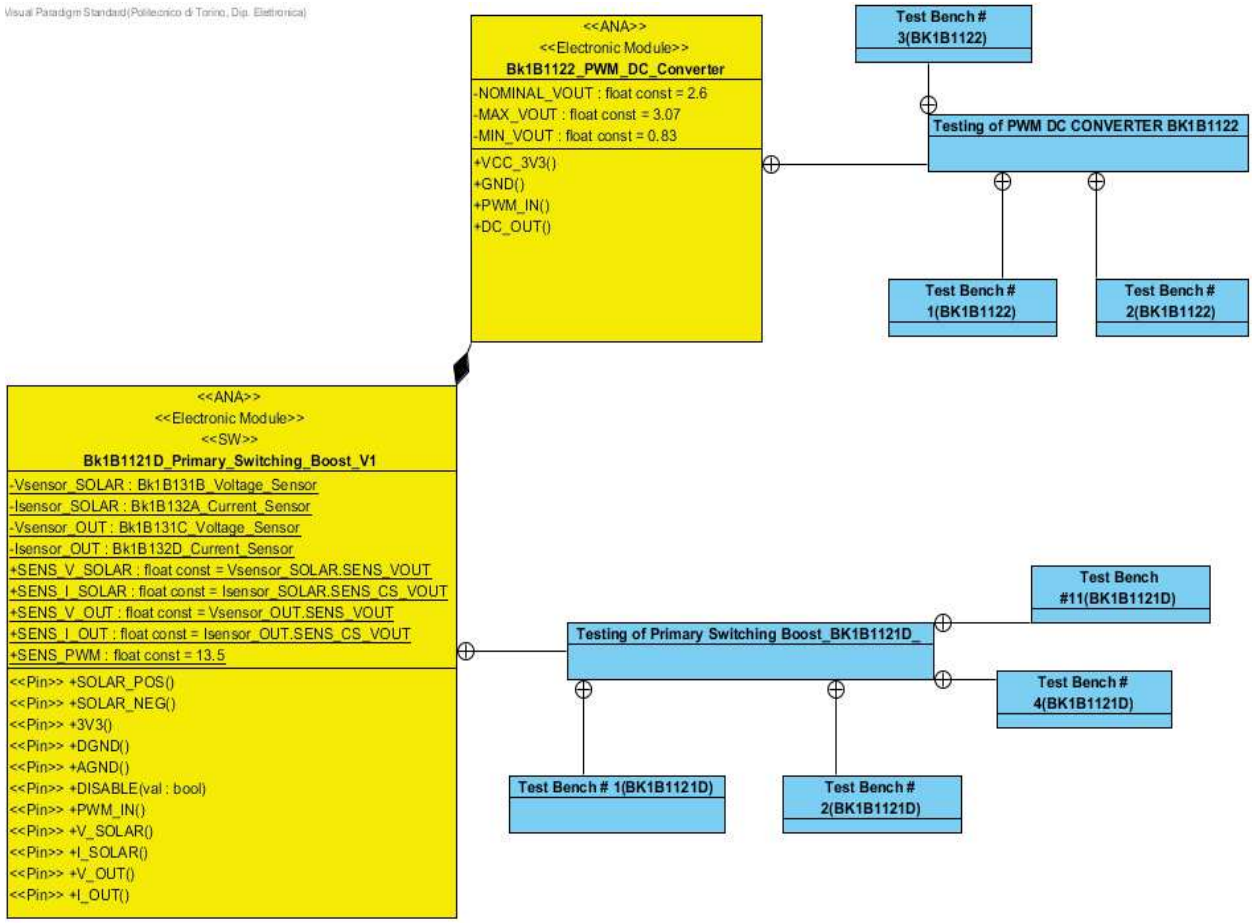


Figure 4.16: Class diagram of 1B1122 PWM DC Converter

4.4.1 Description:

In both 1U and 3U 1B8_CubePMT, PWM DC Converter is used for an AraMiS project. This converter convert the input voltage between input pin PWM_IN () and digital ground DGND () to an output voltage between pin DC_OUT () and digital ground DGND (). Supply voltage shall range between 3 and 3.6 which depends on the specific specialization of 1B1122_PWM_DC_Converter (see tagged value Supply Voltage), while output voltage always a constant voltage. It gives minimal output voltage equal to 0.83, maximum output voltage equal to 3.07V and the nominal output voltage equal to 2.6V. Its schematic diagram is shown in figure below 4.17.

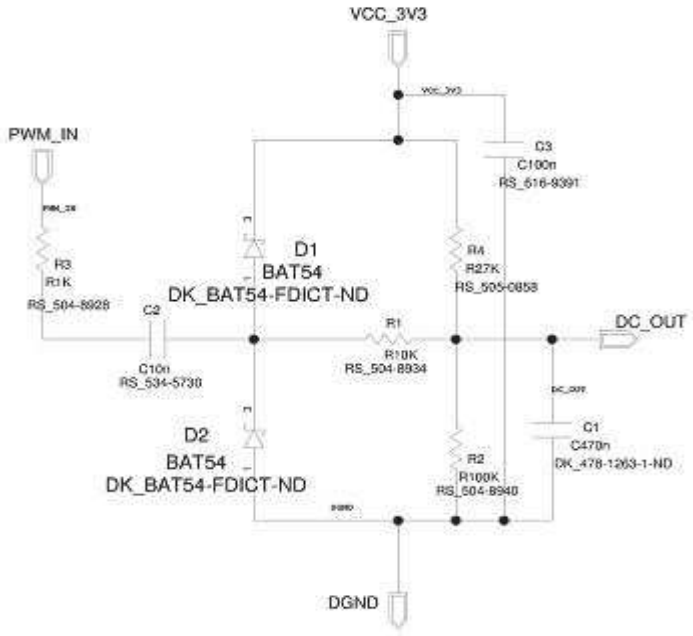


Figure 4.17: Schematic diagram of Bk1B1122_PWM_DC_Converter

4.4.2 Testing of PWM DC CONVERTER BK1B1122

Testing of Bk1B1122_PWM_DC_Converter is given below.

Serial #	Parameter	Expected Value	Current Result	Verification	Pass/Fail	Test Bench
1	Supply Current (uA)	26	24	I(Rload)= Vout/RLOAD 26uA=2.6/ RLOAD Rload=100K	Pass	Test#3
2	SupplyVoltage (VCC_3V3)	Min:3 Max:3.6	Min: 3 Max:3.6	Voltage range is possible as seen in data sheet.	Pass	Test#1
3	Tolerance (%)	0.01	0.01	Output Range:(2.6019-2.5950)/2 T=3.45* 10^-3+2.5950=2.59845----->2.5950/2.59845=0.01%	Pass	Test#2
4	Output Voltage (V)	Min:0.87 Max:3.07	Min:2.36 Max:2.83	I/P's O/P's 3 2.36 3.2 2.51 3.5 2.75 3.6 2.831	Fail	Test#1

Pin PWM_IN ():

Serial #	Parameters	Expected Value	Current Result	Pass/Fail	Test Bench
1	PWM Input Pulse (V)	3.3	3.3	Pass	Test#1

Pin DGND ():

Serial #	Parameter	Expected Value	Current Result	Pass/Fail	Test Bench
1	Supply Current (uA)	26	24	Pass	Test#3

Pin DC_OUT ():

Serial #	Parameters	Expected Value	Current Result	Pass/Fail	Test Bench
1	Min output Voltage	0.87	3-------->2.36	Fail	Test#1

	(V)				
2	Max output Voltage (V)	3.07	3.6----------->2.83	Fail	Test#1

Pin VCC_3V3 ():

Serial #	Parameters	Expected Value	Current Result	Pass/Fail	Test Bench
1	Min Supply Voltage (VCC_3V3)	3	3	Pass	Test#1
2	Max Supply Voltage (VCC_3V3)	3.6	3.6	Pass	Test#1

- ## Test Bench # 1(BK1B1122)

This test is used to measure the output of PWM DC Converter in time domain. Here the dc voltage VCC_3V3 and PWM pulse is given as an input and we calculated the voltage across the output. This PWM DC converter block especially used to give a constant voltage at the inverting terminal of U7 in the Boost converter. Here we got the constant voltage of 2.83V at the output of this converter. Below, I have attached the sim_adms file that represents how to test the output of PWM DC converter in LT-Spice.

```
.tran 100U 1 0 50M
.include "..\..\genhdl\Bk1B1122_PWM_DC_Converter_V1\Bk1B1122_PWM_DC_Converter_V1.spi"
VVAL VCC_3V3 0 DC 3.6
VGND DGND 0 DC 0
VVPWM PWM_IN 0 PULSE(0 3.3 1u 1n)
*******end of additional commands********
.end
```

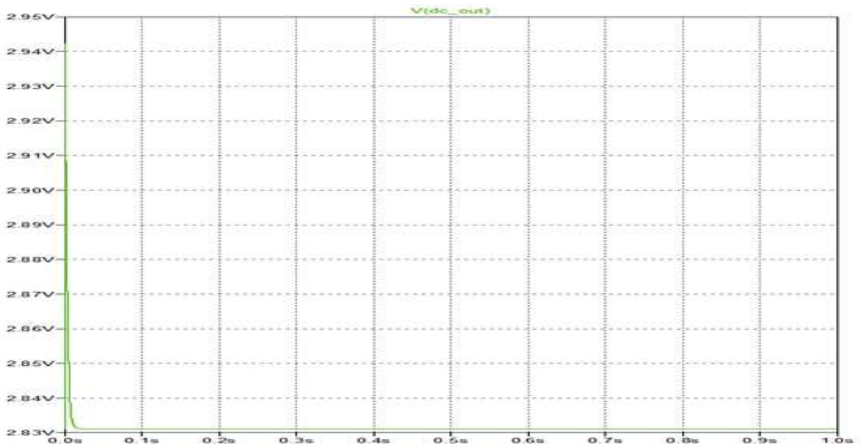


Figure 4.18: Output Vs Input Voltage of Bk1B1122_PWM_DC_Converter

- ## Test Bench # 2(BK1B1122)

This test is used to apply a Montecarlo approach in order to evaluate the error introduced by the manufacturing tolerances of the resistors in the main circuit. For this, zoom in the output voltage VOUT plot and observed the range of output value in which select only those lines which are nearer to each other and then apply the standard deviation formula in order to approximate the tolerance. We will find their tolerances respectively. Below, I have attached the sim_adms file that represents how to test the tolerance of this pwm dc converter in LT-Spice.

```
.tran 100U 1 0 50M
.include "..\..\genhdl\Bk1B1122_PWM_DC_Converter_V1\Bk1B1122_PWM_DC_Converter_V1.spi"
VVAL VCC_3V3 0 DC 3.6
VGND DGND 0 DC 0
RL DC_OUT 0 100k
VVPWM PWM_IN 0 PULSE(0 3.3 1u 1n)
*******end of additional commands*******
.end
```

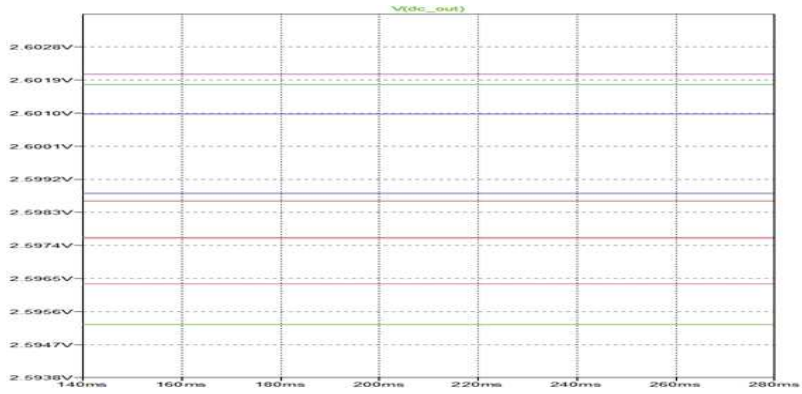


Figure 4.19: Tolerance of Bk1B1122_PWM_DC_Converter

Output Voltage Range for PWM DC Converter is from 2.5950V to 2.6019V.

$$\text{Tolerance} = \frac{(2.6019-2.5950)}{2} = 3.45*10\text{^}-3+2.5950 = \frac{(2.5950)}{2.59845} = 0.01\%$$

The obtained result of tolerance is exactly the same as we expected from this circuit. So, there is no uncertainty in it.

- ## Test Bench # 3(BK1B1122)

This test is used to measure the maximum supply current across the circuit. For this, sink current flow across the load resistance. In simulation of PWM DC Converter, we will get the same value of sink current that is 26uA. Below, I have attached the sim_adms file that represents how to test the maximum supply current of this converter in LT-Spice.

```
.tran 100U 1 0 50M
.step param 0 1 0.001
.include "..\..\genhdl\Bk1B1122_PWM_DC_Converter_V1\Bk1B1122_PWM_DC_Converter_V1.spi"
VVAL VCC_3V3 0 DC 3.3
VGND DGND 0 DC 0
*******end of additional commands*******
.end
```

Figure 4.20: Maximum Supply current of Bk1B1122_PWM_DC_Converter

Below, the load resistor is designed in order to generate expected value of maximum supply current.

$$I\ (Rload) = \frac{Vout}{Rload}$$

$$26uA = 2.6/Rload$$

$$Rload = 100K$$

The same value of both expected and simulated value.

4.4.2 Spice Netlist of BK1122_PWM_DC_Converter:

Once the schematic is created, it is netlisted in the Design Capture of the Mentor Graphics (Simulation→Netlist). It generates a spice netlist which can be used for simulating in the LTSpice. Here I have attached the genhdl file that shows all the components of this voltage sensor and how they are connected in the schematic.

```
* Project Bk1B1122_PWM_DC_Converter_V1
* Mentor Graphics Wirelist Created with Version 6.4.002
* File created Wed Nov 30 13:49:26 2016
* Inifile   :
* ConfigFile:  C:\MentorGraphics\7.9.4EE\SDD_HOME\standard\wspice.cfg
* Options   :  -__ -.spi -h -$ -kC:\MentorGraphics\7.9.4EE\SDD_HOME\standard\wspice.cfg bk1b1122_pwm_dc_converter_v1
* Levels    :
*
C1I523 N_1N18 N_1N14 {MC( 10.000000N , 10.000000 /100)} TC=10.000000U
R1I533 PWM_IN N_1N18 {MC( 1Kohms , 1000.000000M /100)} TC=100.000000U
C1I484 DC_OUT DGND {MC( 470.000000N , 20.000000 /100)} TC=10.000000U
C1I475 VCC_3V3 DGND {MC( 100.000000N , 10.000000 /100)} TC=10.000000U
R1I493 VCC_3V3 DC_OUT {MC( 27Kohms , 1000.000000M /100)} TC=100.000000U
D1I457 N_1N14 VCC_3V3 BAT54
R1I503 DC_OUT DGND {MC( 100Kohms , 1000.000000M /100)} TC=100.000000U
D1I466 DGND N_1N14 BAT54
R1I513 N_1N14 DC_OUT {MC( 10Kohms , 1000.000000M /100)} TC=100.000000U
* Dictionary 2
* _1N14=N_1N14
* _1N18=N_1N18
*Warning : No ground node (Label a net GND)

.include "..\..\sym\BAT54.mod"
```

4.5 BK1B1121D_Primary_Switching_Boost:

A boost converter (step-up converter) is a DC-to-DC power converter that steps up voltage (while stepping down current) from its input (supply) to its output (load). It is a class of switched-mode power supply (SMPS) containing at least two semiconductors (a diode and a transistor) and at least one energy storage element: a capacitor, inductor, or the two in combination. To reduce voltage ripple, filters made of capacitors (sometimes in combination with inductors) are normally added to such a converter's output (load-side filter) and input (supply-side filter). Its working condition is explained below.

When the switch is closed, Mosfet is turned on. During this time diode is off and the path of current then become from the inductor and Mosfet. As we know that the inductor store energy in the form of magnetic field and current flow from the capacitor C2 to the load.

Its duty cycle can be calculated in ON state is given below.

$$T_{ON} = D \times T$$

Where $D = \frac{t_{ON}}{t_{ON}+t_{OFF}}$ and T is the switching cycle. Its schematic diagram is shown in below Figure 4.21.

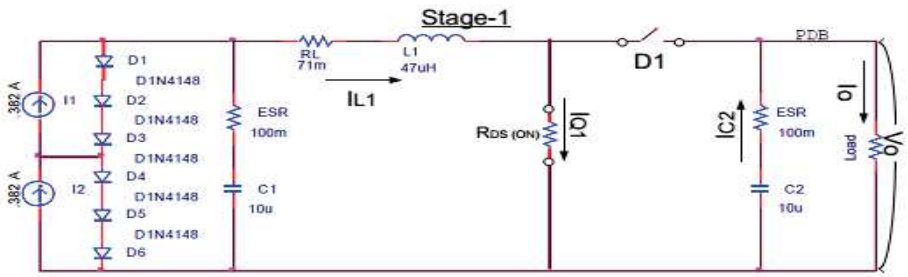


Figure 4.21: Power stage-1 of the boost converter.

When the switch is open, Mosfet is turned off. During this time diode is on and the path of current then become from the inductor and diode towards capacitor and load. Its duty cycle can be calculated in OFF state is given below.

$$T_{OFF} = (1\text{-}D) \times T$$

Where $D = \frac{t_{ON}}{t_{ON}+t_{OFF}}$ and T is the switching cycle. Its schematic diagram is shown in below Figure 4.22.

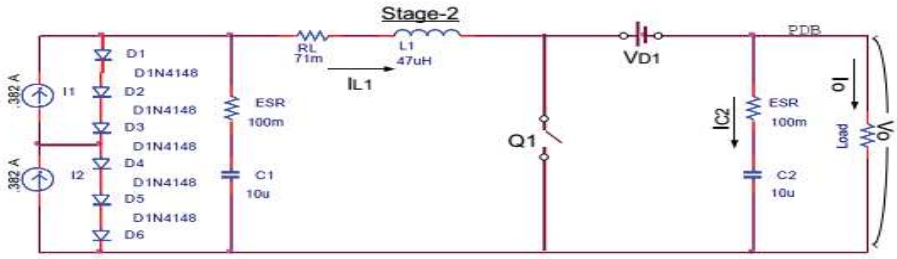


Figure 4.22: MOSFET OFF state of the boost converter.

The class diagram of 1B132 Current Sensor taken from visual paradigm is shown below in figure 4.23.

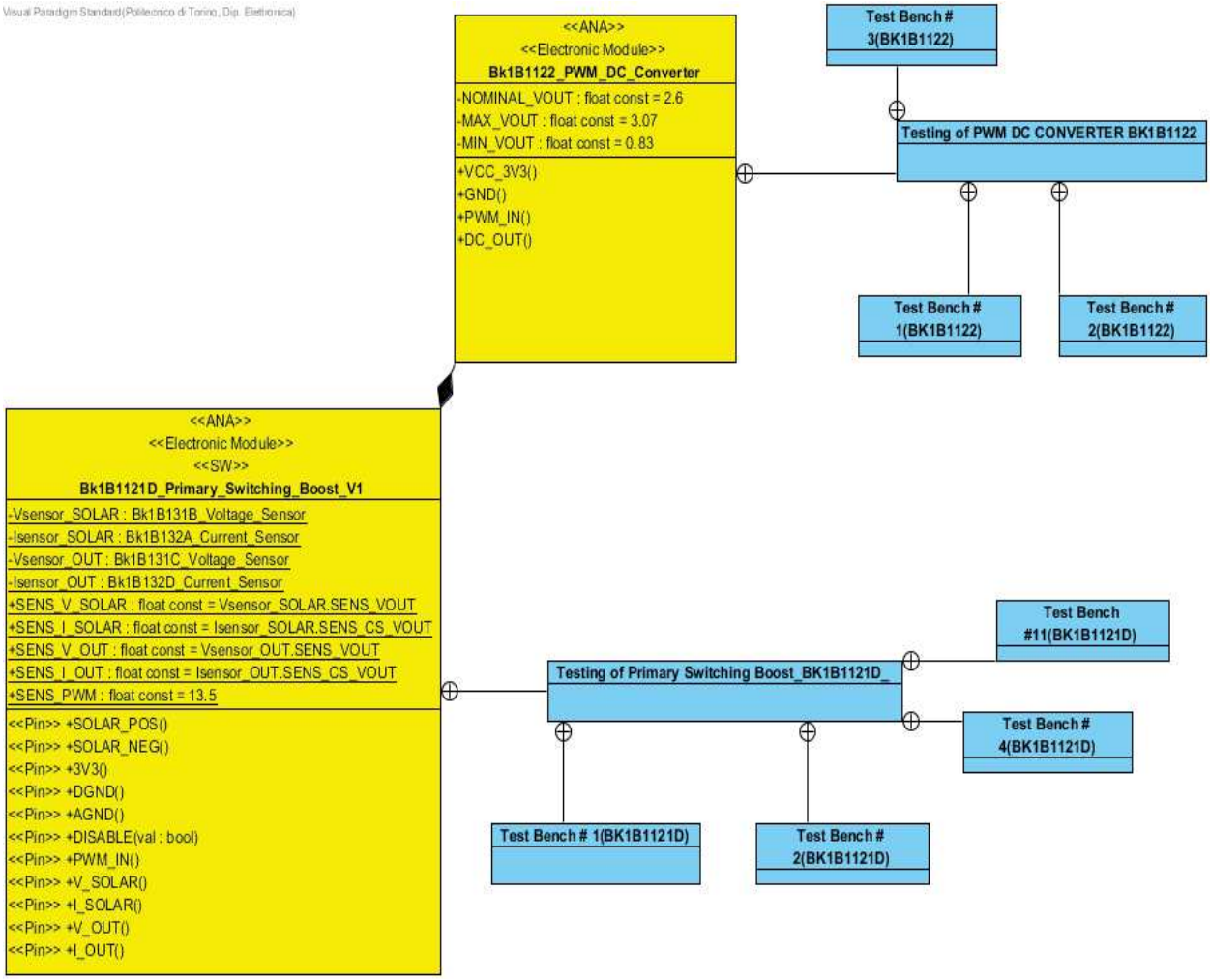


Figure 4.23: Class Diagram of Bk1B1121D_Primary_Switching_Boost_V1.

4.11.2 Description:

In both 1U and 3U 1B8_CubePMT, same boost converter is used for an AraMiS project. This module is the primary converter to be associated with an appropriate solar panel. It has three major functions:

- it sinks power from solar panel (when illuminated), while keeping it close to its maximum power point (MPP);
- it converts electric power with a high-efficiency switching regulator to a suitable voltage level;
- it delivers power to the spacecraft main power distribution bus

The Bk1B1121D_Primary_Switching_Boost_V1 is a boost regulator, that is, its output voltage cannot be lower than input voltage. It shall therefore be used with low voltage solar panels.

It contains a switching power converter which can be controlled in MPPT mode (Maximum Power Point Tracker) with the aid of an external microcontroller which keeps the operating point of the solar panel close to its highest efficiency point. This point depends on illumination and angle of incidence, panel temperature, panel aging and it can vary in case of faults of individual solar cells. The external processor shall measure input power and implement an MPPT algorithm and drive the control input of the converter accordingly.

The Bk1B1121D_Primary_Switching_Boost_V1 connects to a solar panel via its two terminals SOLAR_NEG () and SOLAR_POS () and it deliver power to the on board power bus via the PDBINT () and DGND () terminals. It also provides a few voltage outputs for monitoring the status of the system:

- V_SOLAR() outputs a voltage proportional to voltage across solar panel (system input);
- V_OUT() outputs a voltage proportional to voltage across power distribution bus (system output);
- I_SOLAR() outputs a voltage proportional to current coming from solar panel;
- I_OUT () outputs a voltage proportional to current going to power distribution bus.

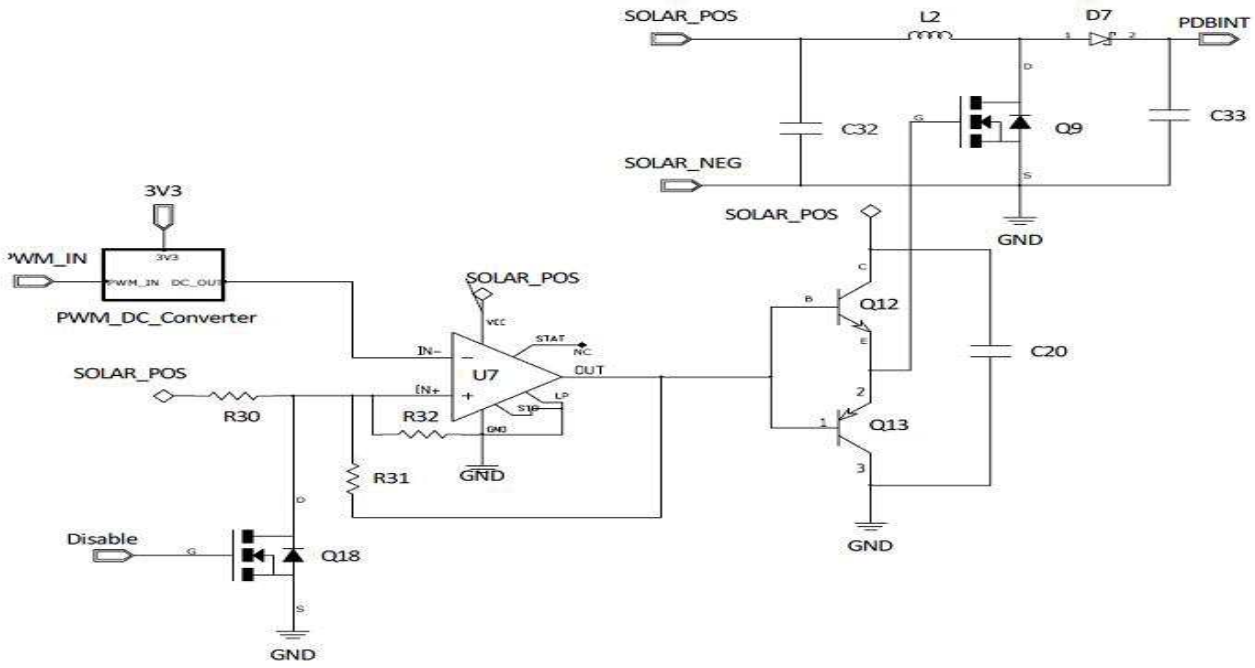
The MPPT algorithm is implemented on an external microprocessor which measures input and output currents and controls the point of operation of the system by means of the duty cycle of a PWM signal which has to be provided to the PWM_IN() digital input.

In case of absence of the PWM signal, the operating mode of the converter autonomously changes to a near-MPPT, where the operation point of the converts returns to a default value which can be set by Configurator by changing the value of a resistor, offering an increased level of tolerance to faults.

It can also be used in stand-alone mode without a microcontroller, by accepting a fixed point of operation, therefore a non optimal efficiency in some situations.

Being an MPPT (or near-MPPT) switching regulator, the output power is kept constant, close to the power sunk from the solar panel. Its output voltage is therefore unregulated as it automatically adapts to the current sunk by the external load across the PDBINT () and DGND () terminals. The

product of the output voltage and current is nearly constant, therefore the V-I characteristic of the



system is hyperbolic. The schematic diagram of boost converter is given blow in figure 4.27.

Figure 4.24: Schematic Diagram of Bk1B1121D_Primary_Switching_Boost_V1.

4.11.3 Specification:

Parameter	Min	Typ	Max	Unit
Input Voltage (SOLAR_POS()-SOLAR_NEG())	2.0		Min Output Voltage + 0.6V	V
Input Current (into SOLAR_POS())			1	A
Output Voltage (PDBINT()-DGND())	12		18	V
Output Current (from PDBINT()), for efficiency > 60%			0.5	A
Short Circuit Current (from PDBINT())		1		A
Efficiency (for V(PDBINT()) = 3.0 * V(SOLAR_POS()-SOLAR_NEG()))		85		%
Efficiency (for V(PDBINT()) > TBD V)	TBD			%
Operating Temperature measured at 5cm from Bk1B1121D_Primary_Switching_Boost_V1	-40		70	°C
PWM_IN() frequency	10			Hz
PWM_IN() logic low	0		0.4	V
PWM_IN() logic high	2.9		3.3	V
DISABLE(val : bool) logic low	0		0.4	V
DISABLE(val : bool) logic high	2.5		10	V
Sensitivity of I_SOLAR()	3.95	4.0	4.05	V/A
Sensitivity of I_OUT()	16.2	16.4	16.6	V/A
Sensitivity of V_SOLAR()	0.250	0254	0.258	V/V
Sensitivity of V_OUT()	0.1235	0.125	0.1265	V/V

Sensitivity of PWM_IN()		0.135 (TBC)		V/%

4.11.4 Testing of Primary Switching Boost_BK1B1121D

Testing's of Switching Regulator Bk1B1121D_Primary_Switching_Boost_V1 are given below.

Serial #	Parameter	Expected Value	Current Result	Verification	Pass/Fail	Test bench
1	Output Voltage (V)	14	14	Min:12V Max:18V V(pdbint)=14V	Pass	TEST#1
2	Tolerance (%)	1.1	1.1	Output Range:(12.980-12.6537)/2 T=0.1637/12.980=0.011=1.1%	Pass	Test#2
3	Input Voltage (V)	4.4	4.4	V(solar_pos)=4.4V	Pass	Test#4
4	Output Current (from PDB with efficiency > 60%) (mA)	max:500	(with Rload=222ohm) 85	I(Rload)=85mA	Pass	Test#1

Pin SOLAR_NEG ():

Serial #	Parameter	Expected Value	Current Result	Pass/Fail	Test bench
1	Voltage across DGND	0	0	Pass	Test#4

Pin SOLAR_POS ():

Serial #	Parameter	Expected Value	Current Result	Pass/Fail	Test bench
1	Maximum Input Voltage	4.4	4.4	Pass	Test#4

Pin AGND ():

Serial #	Parameter	Expected Value	Current Result	Pass/Fail	Test bench
1	Voltage across AGND (V)	0	0	Pass	Test#11

Pin DGND ():

Serial #	Parameter	Expected Value	Current Value	Pass/Failure	Test bench
1	Voltage across DGND (V)	0	0	Pass	Test#11

Pin 3V3 ():

Serial #	Parameter	Expected Value	Current Result	Pass/Fail	Test bench
1	Supply voltage for PWM (V)	3.3	3.3	Pass	Test#11

Pin DISABLE (val: bool):

Serial #	Parameter	Expected Value	Current Result	Pass/Fail	Test bench
1	Minimum Signal Voltage (V)	1.3	1.3	Pass	Test#11
2	Maximum Signal Voltage (V)	1.5	1.5	Pass	Test#11

Pin I_OUT ()

Serial #	Parameter	Expected Value	Current Result	Pass/Fail	Test bench
1	Max Output Current (mA)	152	130	Pass	Test#6

Pin I_SOLAR ():

Serial #	Parameter	Expected Value	Current Result	Pass/Fail	Test bench

1	Max Output Current (mA)	625	480	Pas	Test#6

Pin PWM_IN ():

Serial #	Parameter	Expected Value	Current Result	Pass/Fail	Test bench
1	PWM Input Pulse (V)	3.3	3.3	Pass	Test#11

Pin V_OUT ():

Serial #	Parameter	Expected Value	Current Result	Pass/Fail	Test bench
1	Maximum Output Voltage (V)	2.5	1.5	Fail	Test#7

Pin V_SOLAR ():

Serial #	Parameter	Expected Value	Current Result	Pass/Fail	Test bench
1	Maximum Output Voltage (V)	2.5	1	Fail	Test#7

- ## Test Bench # 1(BK1B1121D)

This test is used to measure the output of Switching Boost Converter in time domain. Here VCC_3V3 and PWM pulse is given as an input and we calculated the voltage across the output V (PDBINT) and current across the load. In 1U 1B8_CubePMT, this Boost Converter is the primary element to boost the input voltage from Solar Panel 4.4 to 14 V PDB. Below, I have attached the sim_adms file that represents how to test the output/input relationship of boost converter in LT-Spice.

```
.tran 100U 0.0008 0 50M
.include "..\..\genhdl\BK1B1121D_Primary_Switching_Boost_V1\BK1B1121D_Primary_Switching_Boost_V1.spi"
VGND1 AGND 0 DC 0
VGND2 DGND 0 DC 0
VPWM PWM_IN 0 DC 3.3 PULSE (0 3.3 100u 100n 100n 10u 15u)
V3V3 N3V3 0 DC 3.9
*RLOAD PDBINT 0 222
XCELL1 SOLAR_POS SOLAR_CEN SolarCell
XCELL2 SOLAR_CEN 0 SolarCell
.include "..\..\sym\SolarCell.mod"
VDisable Disable 0 DC 0
*******end of additional commands********
.end
```

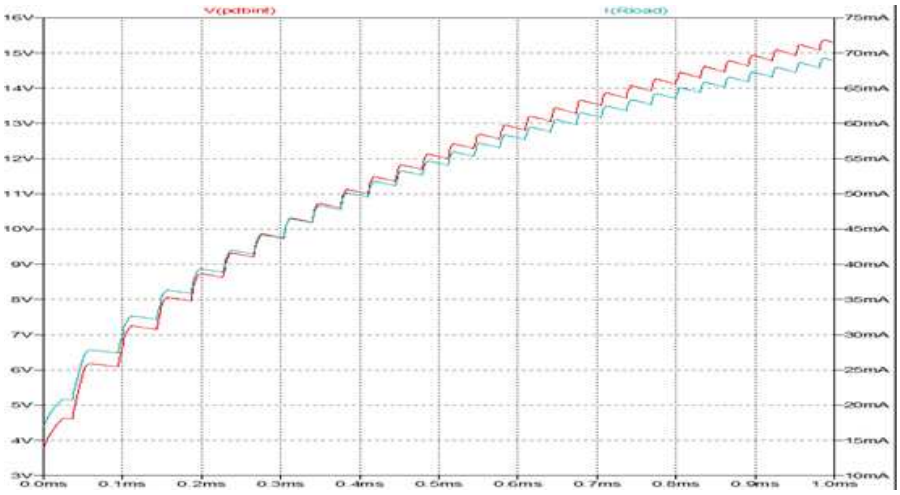


Figure 4.25: Output Voltage of Bk1B1121D_Primary_Switching_Boost_V1.

- ## Test Bench # 2(BK1B1121D)

This test is used to apply a Montecarlo approach in order to evaluate the error introduced by the manufacturing tolerances of the resistors in the main circuit. For this, zoom in the output voltage

VOUT plot and observed the range of output value in which select only those lines which are nearer to each other and then apply the standard deviation formula in order to approximate the tolerance. We will find their tolerances respectively. Below, I have attached the sim_adms file that represents how to test the tolerance of this boost converter in LT-Spice.

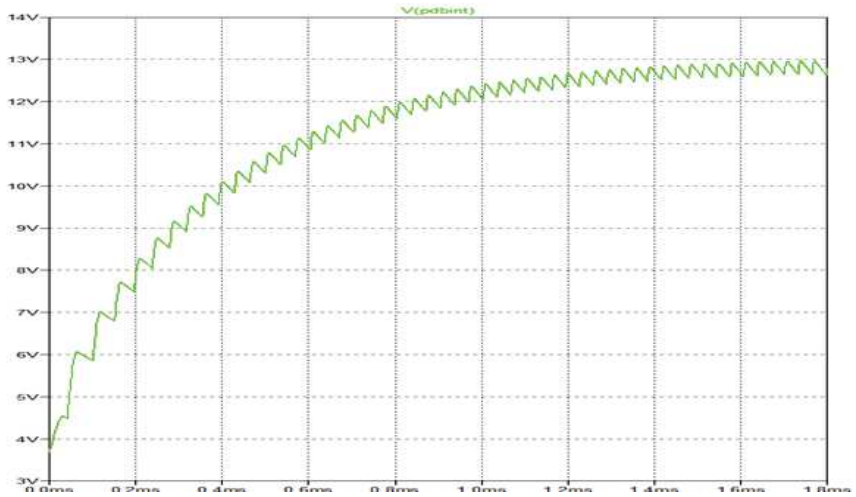


Figure 4.26: Tolerance of Bk1B1121D_Primary_Switching_Boost_V1

Here its tolerance is calculated as given below.

Output Voltage Range for both voltage sensor: 12.980V<------->12.6537V

$$\text{Tolerance} = \frac{12.980 - 12.6537}{2} = \frac{0.1637}{12.980} = 0.011 = 1.1\%$$

- ## Test Bench # 4(BK1B1121D)

This test is used to measure the input of Boost Converter in time domain. Here we gave Solar_POS & Solar_NEG voltage as an input. This is possible by making the sub-circuit of Solar cell so that it gives the maximum input of 4.4V to the boost converter and we calculated the voltage across the output V (PDBINT). The same sim_adms file is used that contains the input parameters of boost converter in LT-Spice.

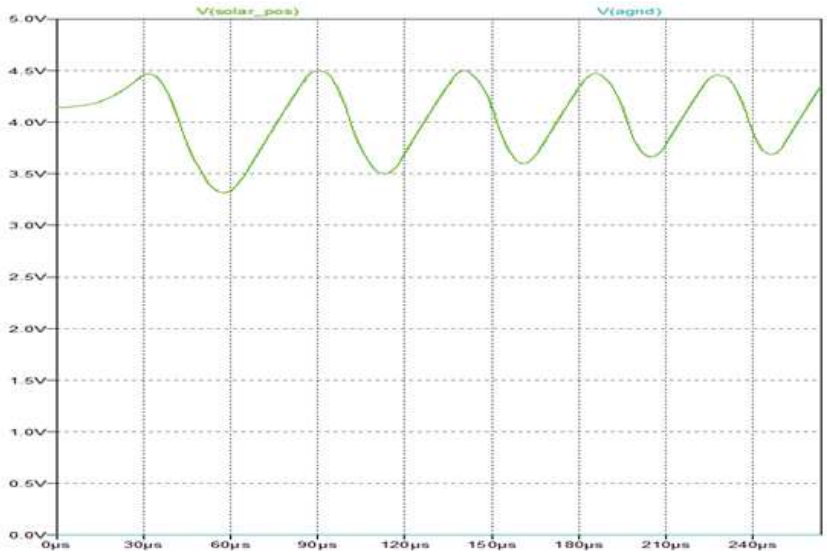


Figure 4.27: Input Source of Bk1B1121D_Primary_Switching_Boost_V1

- **Test Bench #11(BK1B1121D)**

This test is just used to measure the parameters of remaining terminal of the boost converter that may use in activation of some blocks. The reason for making this plot is to help in good reporting inside the visual paradigm. Here we calculated V (agnd), V (dgnd), V (3V3), V (disable), and V (pwm_in). The same sim_adms file is used that contains the input parameters of boost converter in LT-Spice.

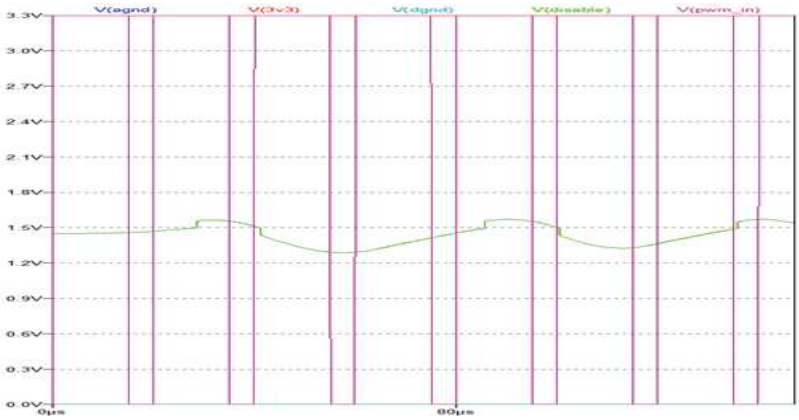


Figure 4.28: Other inputs of Bk1B1121D_Primary_Switching_Boost_V1

4.11.4 Spice Netlist of BK1121_Primary_Switching_Boost:

Once the schematic is created, it is netlisted in the Design Capture of the Mentor Graphics (Simulation→Netlist). It generates a spice netlist which can be used for simulating in the LTSpice

```
*Definition For Project Bk1B1318_Voltage_Sensor_V1
.SUBCKT Bk1B1318_Voltage_Sensor_V1 Vout Vin AGND
CC1 Vout AGND {MC( 10.000000N , 10.000000 /100)} TC=10.000000U
RR1 Vin Vout {MC( 390Kohms , 1000.000000M /100)} TC=100.000000U
RR2 Vout AGND {MC( 133Kohms , 1000.000000M /100)} TC=100.000000U
* CROSS-REFERENCE 0
.ENDS

*Definition For Project Bk1B1122_PWM_DC_Converter_V1                                                    t_V1
.SUBCKT Bk1B1122_PWM_DC_Converter_V1 DGND DC_OUT VCC_3V3 PWM_IN
CC1 N_1N18 N_1N14 {MC( 10.000000N , 10.000000 /100)} TC=10.000000U
RR1 PWM_IN N_1N18 {MC( 1Kohms , 1000.000000M /100)} TC=100.000000U
CC2 DC_OUT DGND {MC( 470.000000N , 20.000000 /100)} TC=10.000000U
CC3 VCC_3V3 DGND {MC( 100.000000N , 10.000000 /100)} TC=10.000000U
RR2 VCC_3V3 DC_OUT {MC( 27Kohms , 1000.000000M /100)} TC=100.000000U
DD1 N_1N14 VCC_3V3 BAT54
RR3 DC_OUT DGND {MC( 100Kohms , 1000.000000M /100)} TC=100.000000U
DD2 DGND N_1N14 BAT54
RR4 N_1N14 DC_OUT {MC( 10Kohms , 1000.000000M /100)} TC=100.000000U
* CROSS-REFERENCE 2
* _1N14=N_1N14
* _1N18=N_1N18
.ENDS

*Definition For Project Bk1B132D_Current_Sensor_V1
.SUBCKT Bk1B132D_Current_Sensor_V1 I_OUT CS_VOUT I_IN AGND
CC1 CS_VOUT AGND {MC( 0.01uF , 10.000000 /100)} TC=10.000000U
XU1 XSIG010025 XSIG010024 XSIG010025 AGND CS_VOUT INA138
RR2 CS_VOUT AGND {MC( 100Kohms , 1000.000000M /100)} TC=100.000000U
XR1 I_IN I_OUT XSIG010025 XSIG010024 RES_4wire R={MC(820Mohms,1000.000000M/100)} TC=250.000000U
* CROSS-REFERENCE 0
.ENDS


.include "..\..\genhdl\BK1B1121D_Primary_Switching_Boost_V1\BK1B1121D_Primary_Switching_Boost_V1_sources.spi"
.include "..\..\sym\B320A.mod"
.include "..\..\sym\BAT54.mod"
.include "..\..\sym\Bk1B12612_Short_Circuit.mod"
.include "..\..\sym\INA138.mod"
.include "..\..\sym\MAX975HS.mod"
.include "..\..\sym\MMBF0201.mod"
.include "..\..\sym\MMBT3904LT1G.mod"
.include "..\..\sym\MMBT3906.mod"
.include "..\..\sym\RES_4WIRE.mod"
.include "..\..\sym\SI7112ADN.mod"
*Definition For Project Bk1B132A_Current_Sensor_V1
.SUBCKT Bk1B132A_Current_Sensor_V1 AGND I_OUT CS_VOUT I_IN
CC1 CS_VOUT AGND {MC( 0.01uF , 10.000000 /100)} TC=10.000000U
XU1 XSIG010025 XSIG010024 XSIG010025 AGND CS_VOUT INA138
RR1 CS_VOUT AGND {MC( 100Kohms , 1000.000000M /100)} TC=100.000000U
XR2 I_IN I_OUT XSIG010025 XSIG010024 RES_4WIRE R={MC(200Mohms,1000.000000M/100)} TC=200.000000U
* CROSS-REFERENCE 0
.ENDS


*Definition For Project Bk1B12612_Short_Circuit
.SUBCKT Bk1B12612_Short_Circuit B A
* CROSS-REFERENCE 0
.ENDS
```

as shown below. Here I have attached the genhdl file that shows all the components of this primary switching boost and how they are connected in the schematic.

4.12 1B121 Load Switch:

Load switch is an integrated electronic relays used to turn on and turn off power rails. It consists of four pins for input voltage, output voltage, enable, and ground. When the device is enabled via the ON pin, the pass FET turns on, thereby allowing current to flow from the input pin to the output pin and power is passed to the downstream circuitry. The class diagram of Load Switches is given below in figure 4.29.

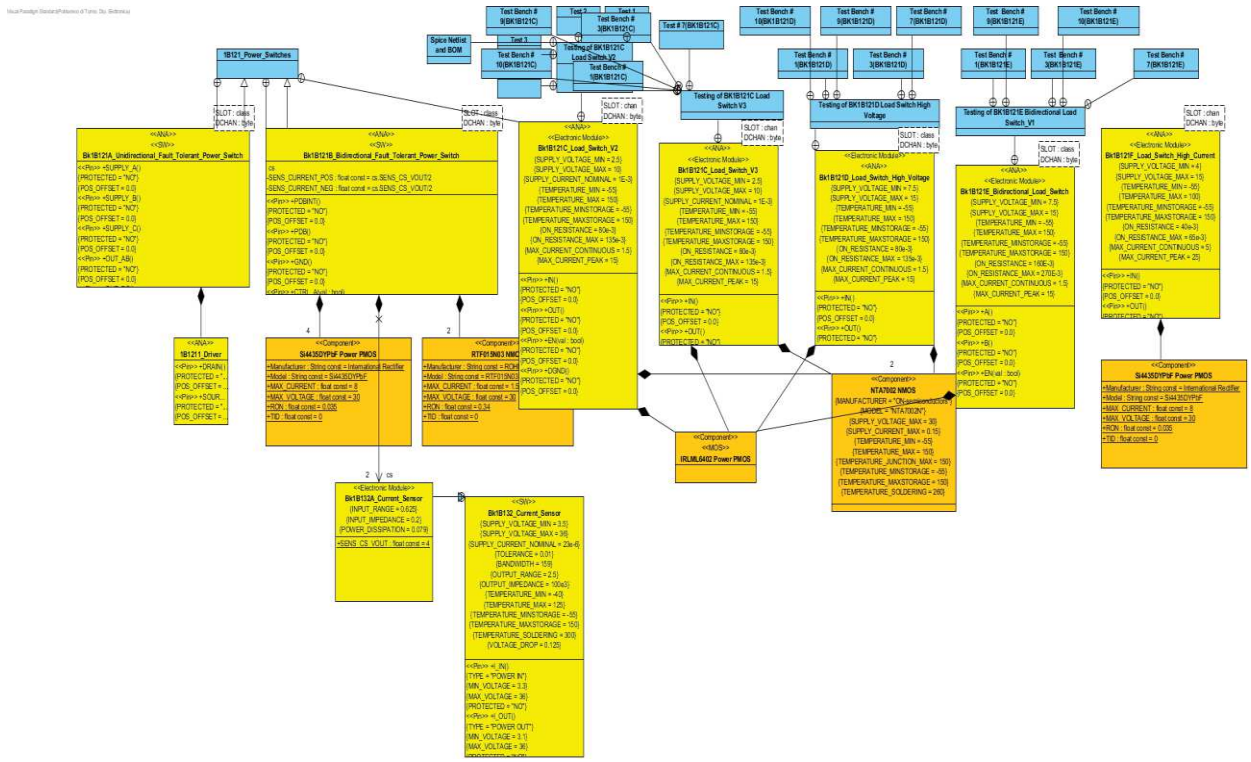


Figure 4.29: Class Diagram of Bk1B121_Load_Switch

4.12.1 Description:

Load switch is used to activate/deactivate power supply of other blocks. It requires an appropriate supply generator across pins IN () and DGND () capable of providing enough current to the external load connected across pins OUT () and DGND ().When voltage on EN (val: bool) pin (w.r.t. to DGND ()) is above threshold (1.9V), the OUT () pin is shorted to IN () with an ON resistance below 80mOhm. When voltage on EN (val : bool) pin (w.r.t. to DGND()) is below threshold (0.5V) , the OUT() pin is open with a leakage current (between IN() and OUT()) below 25uA at 70oC. Bk1B121C_Load_Switch has the following schematic diagram as shown in figure 4.30.

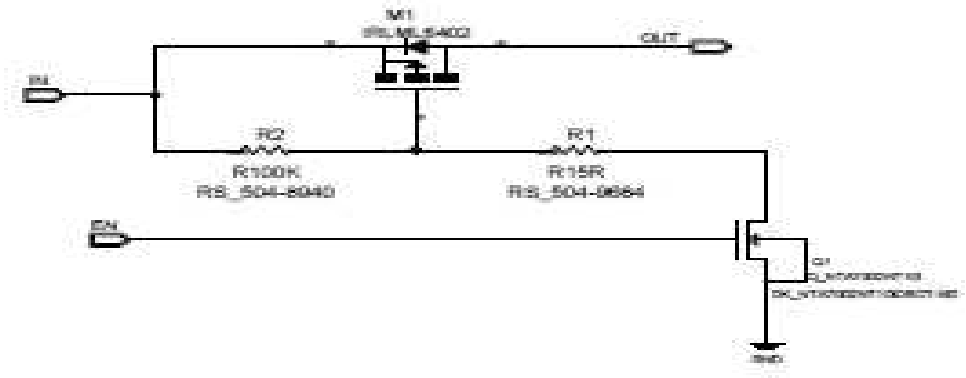


Figure 4.30: Schematic diagram of Bk1B121C_Load_Switch_V3

4.12.2 Testing of BK1B121C Load Switch V3

Testing of Bk1B121C_Load_Switch_V3 are given below.

Serial #	Parameter	Expected Value	Current Result	Verification	Pass/Fail	Test Bench
1	Maximum output Current(A)	1.5	1.49	Isink= Vout/RLOAD 1.5=10/ RLOAD Rload= 6.7	Pass	Test #3
2	Input Voltage(VAL)	Min:2.5 Max:10	Min:2.5 Max:10	IN-OUT=Result 2.5-2.478=0.022 5-4.973=0.027 7.5-7.464=0.036 10-9.956=0.044	Pass	Test#1
3	Temperature (Centigrade)	Min:-55 Max:150	Min:-55 Max:150	Min:-55-----> >Vout=2.478 Max:150-----> Vout=2.46	Pass	Test#7
4	On Resistance (Rds)	0.065	0.077	(Vin-Vout)/Ix(1i77:3)	Fail	Test#9
5	Rise and Fall time	Rise time:300nsec Fall time:220usec	Rise time:300nsec Fall time:220usec	Vout:from off to fully on take 300nsec Vout:from on to off take 220usec	Pass	Test#10

Pin IN ():

Serial #	Parameter	Expected Value	Current Result	Pass/Fail	Test Bench
1	Voltage Min(V)	2.5	2.5	Pass	Test#1
2	Voltage Max(V)	10	10	Pass	Test#1

Pin EN (val: bool):

Serial #	Parameters	Expected Value	Current Result	Pass/Fail	Test Bench
1	Enable (V)	1.3	1.3	Pass	Test#1

Pin DGND ():

Serial #	Parameters	Expected Value	Current Result	Verification	Pass/Fail	Test Bench
1	Supply output Peak(A)	1.5	1.49	Isink= Vout/RLOAD 1.5=10/ RLOAD Rload= 6.7	Pass	Test#3

Pin OUT ():

Serial #	Parameters	Expected Value	Current Result	Pass/Fail	Test Bench
1	Output Range(V)	2.5-10	2.5-10	Pass	Test#1

- ## Test Bench # 1(BK1B121C)

This test is used to measure the output of Load Switches with respect to input. Here we gave the dc voltage as an input and we calculated the output voltage. The maximum output voltage of this Load switch is 10V which is based on the designed passive components that help in using load switches in different purposes. Below, I have attached the sim_adms file that represents how to test the Input/output relationship of Load switch in LT-Spice.

```
.tran 1U 20000U
.include "..\..\genhdl\Bk1B121C_Load_Switch_V3\Bk1B121C_Load_Switch_V3.spi"
VVdgnd DGND 0 DC 0
VVen EN DGND DC 3.3 PULSE (0 3.3 10u 10n 10n 10m 20m )
RL OUT DGND 6.7
Vvin IN DGND DC 3.3
*******end of additional commands********
.end
```

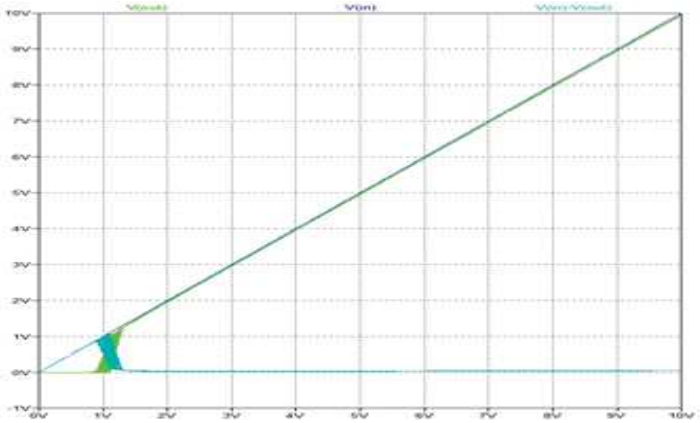


Figure 4.31: Input/Output Voltage of Bk1B121C_Load_Switch_V3

- ## Test Bench # 3(BK1B121C)

This test is used to measure the maximum supply current across the Load Switches. For this, sink current flow across the load resistance. In simulation of all Load Switches, we will get the same value of sink current that is 1.5A. Below, I have attached the sim_adms file that represents how to test the sink current of Load switch in LT-Spice.

```
.tran 1U 400U
.include "..\..\genhdl\Bk1B121C_Load_Switch_V3\Bk1B121C_Load_Switch_V3.spi"
VVdgnd DGND 0 DC 0
VVen EN DGND DC 1.3
RL OUT DGND 6.7
Vvin IN DGND DC 10
*******end of additional commands********
.end
```

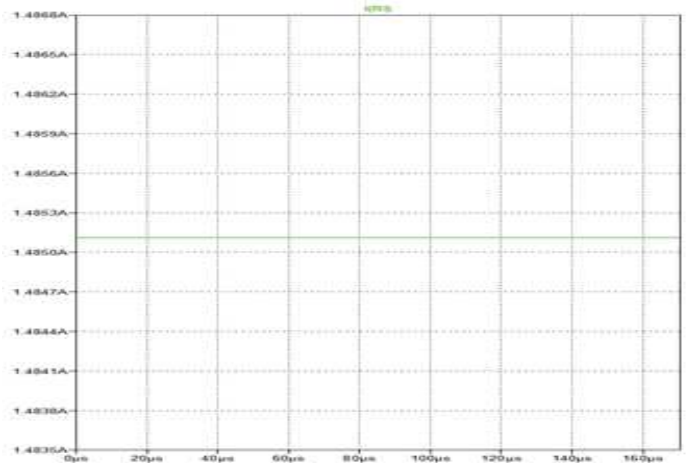


Figure 4.32: Maximum Supply Current of Bk1B121C_Load_Switch_V3

The expected value of this Load switch is designed as given below.

$$\text{Isink} = \frac{\text{Vout}}{\text{Rload}}$$
$$1.5 = \frac{10}{\text{Rload}}$$

Rload=6.7 ohm

- ## Test # 7(BK1B121C)

This test is used to measure the change of output voltage by changing the temperature. Below, I have attached the sim_adms file that represents how to test the output of load switch by changing the temperature in LT-Spice.

```
.dc temp -55 150 5
.include "..\..\genhdl\Bk1B121C_Load_Switch_V3\Bk1B121C_Load_Switch_V3.spi"
VVdgnd DGND 0 DC 0
VVen EN DGND DC 3.3 PULSE (0 3.3 20u 10n 10n 80u 2000u )
RL OUT DGND 6.7
Vvin IN DGND DC 2.5
*******end of additional commands********
.end
```

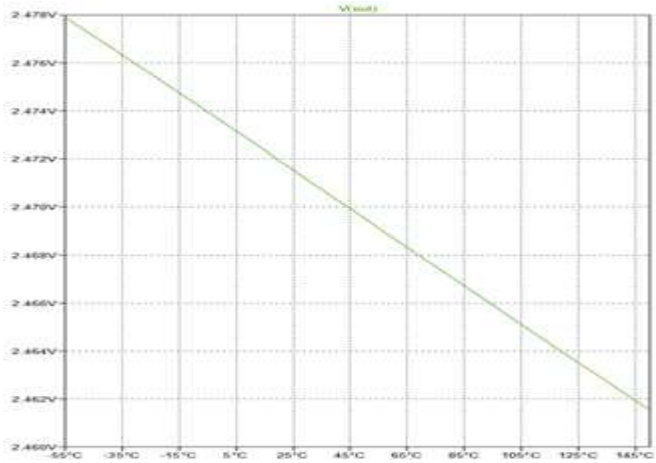


Figure 4.33: Temperature Vs Output Voltage of Bk1B121C_Load_Switch_V3

Here the maximum and minimum temperature effect on the output voltage is calculated as given below.

At -55 degree centigrade Vout=2.478 V
At 150 degree centigrade Vout=2.46 V

- ## Test Bench # 9(BK1B121C)

This test is used to measure the ON resistance in time domain. When voltage on EN (val: bool) pin (with respect to DGND ()) is above threshold (1.9V), the OUT () pin is shorted to IN () with an ON resistance below 80mΩ. Both expected and actual values are same for this Load Switches that is below 80mΩ. Below, I have attached the sim_adms file that represents how to test the On resistance of Load switch in LT-Spice. Here I have attached the genhdl file that shows all the components in this solar panel and how they are connected in the schematic.

```
.tran 1U 400U
.include "..\..\genhdl\Bk1B121C_Load_Switch_V3\Bk1B121C_Load_Switch_V3.spi"
VVdgnd DGND 0 DC 0
VVen EN DGND DC 1.3
RL OUT DGND 6.7
Vvin IN DGND DC 2.5
*******end of additional commands********
.end
```

Figure 4.34: On Resistance of Bk1B121C_Load_Switch_V3

4.12.3 Spice Netlist of BK1B121C_Load_Switch_V3:

Once the schematic is created, it is netlisted in the Design Capture of the Mentor Graphics (Simulation→Netlist). It generates a spice netlist which can be used for simulating in the LTSpice. Here I have attached the genhdl file that shows all the components of this load switch and how they are connected in the schematic.

```
* Project BK1B121C_Load_Switch_V3
* Mentor Graphics Virelist Created with Version 6.4.002
* File created Sun Nov 06 00:12:21 2016
* Inifile   :
* ConfigFile:  C:\MentorGraphics\7.9.4EE\SDD_HOME\standard\wspice.cfg
* Options   :  -__ -.spi -h -$ -7 -kC:\MentorGraphics\7.9.4EE\SDD_HOME\standard\wspice.cfg bk1b121c_load_switch_v3
* Levels    :
*
R1I506 IN N_1N67 {MC( 100Kohms , 1000.000000M /100)} TC=100.000000U
X1I478 OUT N_1N67 IN IRLML6402
X1I486 N_1N71 EN DGND NTA7002N
R1I496 N_1N67 N_1N71 {MC( 15ohms , 1000.000000M /100)} TC=100.000000U
* Dictionary 2
* _1N71=N_1N71
* _1N67=N_1N67
*Warning : No ground node (Label a net GND)

.include "..\..\genhdl\BK1B121C_Load_Switch_V3\BK1B121C_Load_Switch_V3_sources.spi"
.include "..\..\sym\IRLML6402.mod"
.include "..\..\sym\NTA7002N.mod"
```

4.13 BK1B125 Linear and Switching Regulator:

A voltage regulator is designed to automatically maintain a constant voltage level. It usually used for converting higher voltage level lower voltage levels. It is further divided into two categories (Linear and switching regulator). Its distinguished features are explained in below table.

Linear Regulators	Switching Regulators
Only Step down	Both Step up and Step down
Operate in Linear Region	Operate in Saturation and Cutoff Region
Economical	Costly
Less Efficient and small in size	More Efficient and larger in size
Low to medium power consumption	High power consumption

The class diagram of Bk1B1251_Linear and Switching Regulators is shown in below Figure 4.35.

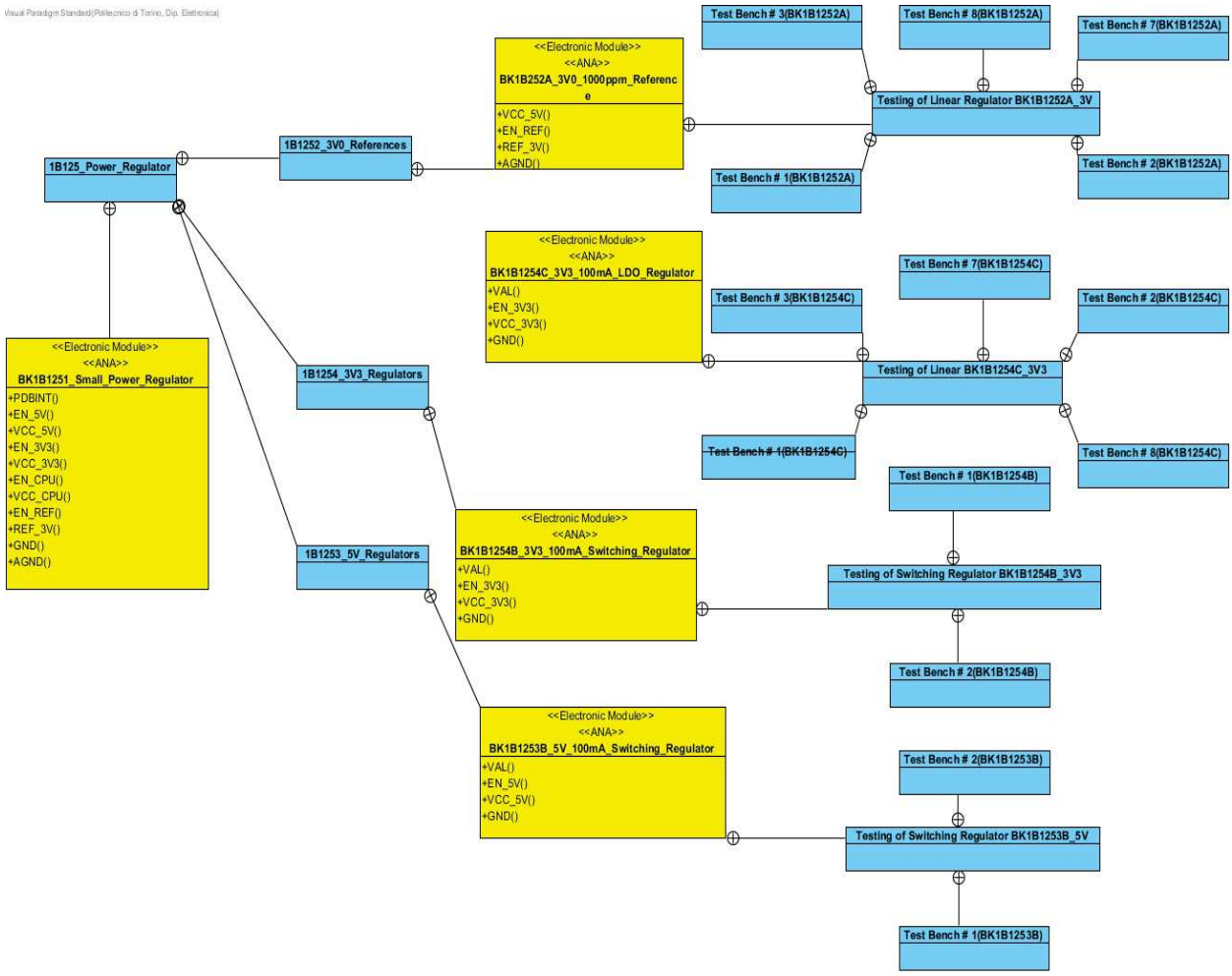


Figure 4.35: Class Diagram of Linear and Switching Regulators.

4.13.1 Description:

The regulator convert the input voltage between input pin VIN () and analog ground AGND () to an output voltage between pin VOUT () and analog ground AGND (). Input voltage shall range between 0 and a maximum value which depends on the specific specialization of Bk1B125_Power_Regulator (see tagged value INPUT_RANGE), while output voltage is always constant according to the specification of regulator.

In both IU and 3U 1B8_CubePMT, PDB voltage level has to be down converted to low voltage levels (i.e. REF_3V (), VCC_3V3 (), VCC_CPU () and VCC_5V ()) used by different subsystem components. For this purpose, BK1B1251_Small_Power_Regulator contains four regulators: two linear and two switching.

4.13.2 Testing of Linear Regulator_BK1B1252A_3V0

Class BK1B252A_3V0_1000ppm_Reference:

This linear regulator steps down VCC_5V () input to REF_3V () output in order to give this reference voltage REF_3V () to the CubePMT subsystems especially for the magnetometer and magnetic torque actuator.It works only when it is enabled EN_REF() from the Tile processor. Output current and input/output voltage difference is low; therefore a linear regulator is used. It is a National Semiconductor component with part number DK_LM4128AMF-3.0CT-ND and reference designator U1. The schematic of BK1B252A_3V0_1000ppm_Reference is shown in below Figure 4.36.

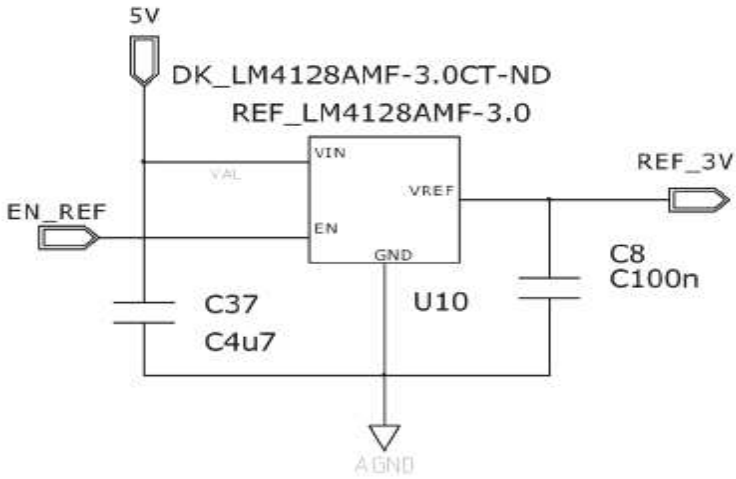


Fig 4.36: Schematic diagram of BK1B252A_3V0_1000ppm_Reference

Testing Results of Linear Regulator BK1B252A_3V0_1000ppm_Reference are given below.

Serial #	Parameter	Expected Value	Current Result	Verification	Pass/Fail	Test Bench
1	Maximum Supply Current(A)	100uA	100uA	Isink=V/Rsink=3/30k=100uA or I(Rload)=100uA	Pass	Test #3
2	Temperature(C)	Min:-40 Max:125	Min:-40 Max:125	-40:REF_3V=3V 125:REF_3V=3V	Pass	Test#7
3	Input Voltage(VAL)	Min:3.8 Max:7.4	Min:3.8 Max:7.4	I/P's 3.8 5 6 7.4 / O/P's 3 3 3 3	Pass	Test#1
4	Tolerance (%)	0	0	By Monte Carlos Approach	Pass	Test#2
5	Input Current (mA)	30mA	30mA	I(Vin)=30mA	Pass	Test#8

Pin VCC_5V ():

Serial #	Parameter	Expected Value	Current Result	Verification	Pass/Fail	Test Bench
1	Voltage Min(V)	3.8	3.4	REF_3V=3	Pass	Test#1
2	Voltage Max(V)	7.4	20	REF_3V=3	Pass	Test#1

Pin EN_REF ():

Serial #	Parameters	Expected Value	Current Result	Verification	Pass/Fail	Test Bench
1	Fixed Voltage(V)	5	5	VEN EN_5V 0 DC 5	Pass	Test#1

Pin REF_3V ():

Serial #	Parameters	Expected Value	Current Result	Verification	Pass/Fail	Test Bench
1	Output Range(V)	3	3	REF_3V=3	Pass	Test#1

Pin DGND ():

Serial #	Parameters	Expected Value	Current Result	Verification	Pass/Fail	Test Bench

1	Supply Current Peak(A)	0.0001	0.0001	Isink=REF_3V/Rsink=3/30K =100uA	Pass	Test#3

- ## Test Bench # 1(BK1B1252A)

This test is used to measure the output of Linear Regulators with respect to input. Here dc voltage is given as an input and we calculated the voltage across the output terminal. This regulator step down to constant voltage equal to 3V. Below, I have attached the sim_adms file that represent how to test this regulator in LT-Spice.

```
.tran 10U 500M 0 1U
.include "..\..\genhdl\Bk1B1254C_3V3_100mA_LDO_Regulator_V1\Bk1B1254C_3V3_100mA_LDO_Regulator_V1.spi"
VEN EN_3V3 0 DC 3.3
VGND DGND 0 DC 0
VSUPPLY VAL 0 PULSE (1 20 1U 500M )
*******end of additional commands********
.end
```

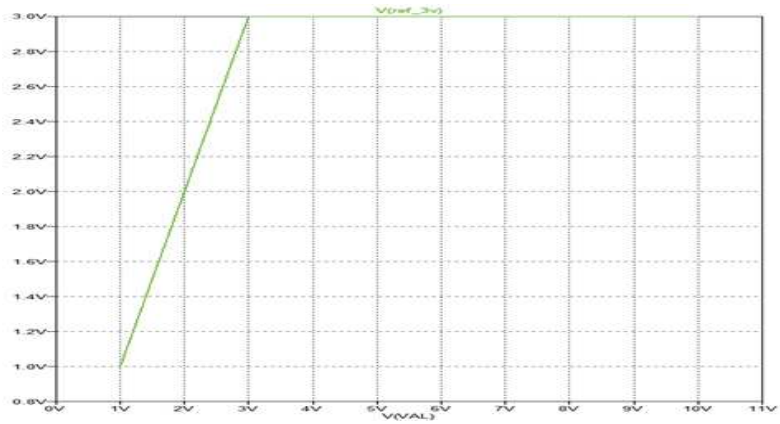


Fig 4.37: Output Vs Input Voltage of BK1B252A_3V0_1000ppm_Reference

- ## Test Bench # 2(BK1B1252A)

This test is used to apply a Montecarlo approach in order to evaluate the error introduced by the manufacturing tolerances of the resistors in the main circuit. For this, zoom in the output voltage VOUT plot and observed the range of output value in which select only those lines which are nearer to each other and then apply the standard deviation formula in order to approximate the tolerance. We will find their tolerances respectively. Below, I have attached the sim_adms file that represents how to test the tolerance of this current sensor in LT-Spice.

Fig 4.38: Tolerance of BK1B252A_3V0_1000ppm_Reference

Here we saw the same output value even we further zoom it. The obtained uncertainty is about 0%.

- ## Test Bench # 3(BK1B1252A)

This test is used to measure the maximum supply current across the circuit. For this, sink current flow across the load resistance. In simulation of this Linear Regulators, I will get more or less the same value of sink current that is 100uA. Below, I have attached the sim_adms file that represents how to test the maximum supply current of this regulator in LT-Spice.

```
.tran 0.01 1 0
.include "..\..\genhdl\Bk1B1252A_3V01000ppmRef_V1\Bk1B1252A_3V01000ppmRef_V1.spi"
VDGND DGND 0 DC 0
VEN EN_REF 0 DC 5
VIN VAL 0 DC 5
RLOAD REF_3V 0 30K
*******end of additional commands********
.end
```

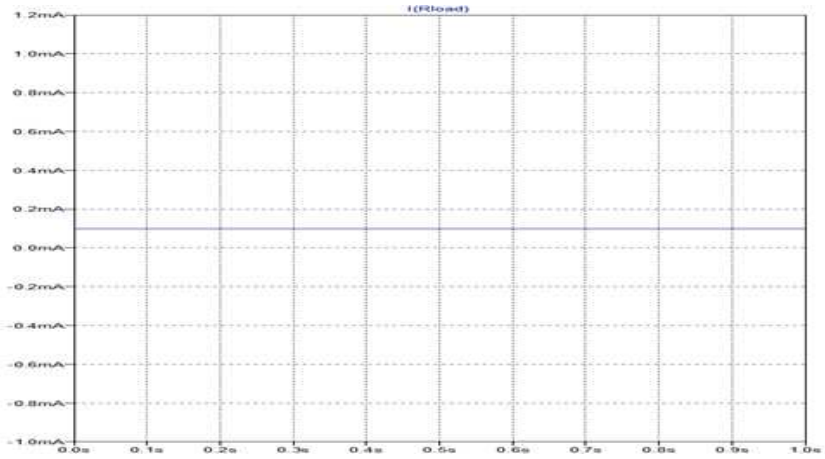


Fig 4.39: Maximum Supply current of BK1B252A_3V0_1000ppm_Reference

Here the expected values of maximum supply current is calculated as

$$\text{Imax} = \frac{V}{\text{Rsink}} = \frac{3}{30K} = 100\text{uA}$$

- ## Test Bench # 7(BK1B1252A)

This test is used to measure the change of output voltage by changing the temperature. Below, I have attached the sim_adms file that represents how to test the output of this regulator by changing the temperature in LT-Spice.

```
.dc temp -150 500 5
.include "..\..\genhdl\Bk1B1252A_3V01000ppmRef_V1\Bk1B1252A_3V01000ppmRef_V1.spi"
VDGND DGND 0 DC 0
VEN EN_REF 0 DC 5
VIN VAL 0 DC 5
RLOAD REF_3V 0 100
*******end of additional commands********
.end
```

Fig 4.40: Temperature Vs Output Voltage of BK1B252A_3V0_1000ppm_Reference

Here we will mention the maximum and minimum temperature effect on the output voltage.

At -40 degree centigrade: REF_3V=2.996V

At 125 degree centigrade: REF_3V=2.996V

- ## Test Bench # 8(BK1B1252A)

This test is used to measure the input current of Linear Regulator in time domain. Here the DC voltage and Enable pulse is given as an input.

```
.tran 0.01 1 0
.include "..\..\genhdl\Bk1B1252A_3V01000ppmRef_V1\Bk1B1252A_3V01000ppmRef_V1.spi"
VDGND DGND 0 DC 0
VEN EN_REF 0 DC 5 PULSE 0 5 0.1 1u 1u 0.5
VIN VAL 0 DC 5
RLOAD REF_3V 0 100
*******end of additional commands********
.end
```

Fig 4.41: Input current of BK1B252A_3V0_1000ppm_Reference

Here the input current of apply voltage is calculated as

Input Current=I (Vin) =30mA

4.13.3 Spice Netlist of BK1252A_3V01000ppmRef_V1:

Once the schematic is created, it is netlisted in the Design Capture of the Mentor Graphics (Simulation→Netlist). It generates a spice netlist which can be used for simulating in the LTSpice as shown below. Here I have attached the genhdl file that shows all the components of this voltage sensor and how they are connected in the schematic.

```
* Project Bk1B1252A_3V01000ppmRef_V1
* Mentor Graphics Wirelist Created with Version 6.4.002
* File created Fri Nov 04 18:29:47 2016
* Inifile   :
* ConfigFile:  C:\MentorGraphics\7.9.4EE\SDD_HOME\standard\wspice.cfg
* Options   :  -__ -.spi -h -$ -7 -kC:\MentorGraphics\7.9.4EE\SDD_HOME\standard\wspice.cfg bk1b1252a_3v01000ppmref_v1
* Levels    :
*
X1I218 EN_REF VAL REF_3V DGND LM4128_3V
C1I177 REF_3V DGND {MC( 100.000000N , 10.000000 /100)} TC=10.000000U
R1I197 REF_3V REF_3V VALUE
C1I167 VAL DGND {MC( 4.700000U , 10.000000 /100)} TC=10.000000U
* Dictionary 0
*Warning : No ground node (Label a net GND)

.include "..\..\genhdl\Bk1B1252A_3V01000ppmRef_V1\Bk1B1252A_3V01000ppmRef_V1_sources.spi"
.include "..\..\sym\LM4128_3V.mod"
```

4.14 Testing of Linear BK1B1254C_3V3

Class BK1B1254C_3V3_100mA_LDO_Regulator:
This linear regulator steps down VAL () input to VCC_3V3 (). The purpose of this LDO is to continuously give power VCC_3V3 () to Tile processor whenever the processor want and also make it independent from other sub circuit. It is enabled EN_3V3 () from the Tile processor. Input/ Output voltage difference is high but supply current is very low which results in negligible power loss; therefore a linear regulator is used. It is a National Semiconductor component with part number DK_LT1761ES5-3.3#TRMPBFCT-ND and reference designator U26. The schematic, IC pins layout and PCB layout are shown in the following figure 4.42.

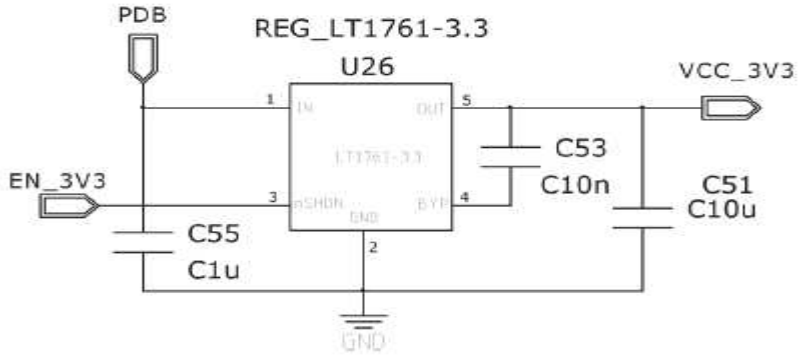


Fig 4.42: Schematic Diagram of BK1B1254C_3V3_100mA_LDO_Regulator

Testing Results of BK1B1254C_3V3_100mA_LDO_Regulator are given below.

Serial #	Parameter	Expected Value	Current Result	Verification	Pass/Fail	Test Bench
1	Maximum Supply Current(A)	100mA	100mA	Isink=V/Rsink=3.3/33=100mA	Pass	Test #3
2	Temperature(C)	Min:-40 Max:125	Min:-50 Max:150	-50:VCC=3.309V 150:VCC=3.31V	Pass	Test#7
3	Input Voltage(PDB)	Min:3.4V Max:20V	Min:3.4V Max:20V	I/P's O/P's 5 3.3 10 3.3 13 3.3 19 3.3	Pass	Test#1
4	Tolerance (%)	0	0	By Monte Carlos Approach	Pass	Test#2
5	Input	35	35	I(Vin)=35mA	Pass	Test#8

	Current(mA)					

Pin VAL ():

Serial #	Parameter	Expected Value	Current Result	Verification	Pass/Fail	Test Bench
1	Supply Voltage Min(V)	3.4	3.4	VCC_3V3=3.3	Pass	Test#1
2	Supply Voltage Max(V)	20	20	VCC_3V3=3.3	Pass	Test#1

Pin EN_3V3 ():

Serial #	Parameters	Expected Value	Current Result	Verification	Pass/Fail	Test Bench
1	Fixed Voltage(V)	3.3	3.3	From Tile Processor	Pass	Test#1

Pin VCC_3V3 ():

Serial #	Parameters	Expected Value	Current Result	Verification	Pass/Fail	Test Bench
1	Output Range(V)	3.3	3.3	VCC_3V3=3.3	Pass	Test#1

Pin GND ():

Serial #	Parameters	Expected Value	Current Result	Verification	Pass/Fail	Test Bench
1	Supply Current Peak(A)	0.1	0.1	Isink=V/Rsink=3.3/33=100mA	Pass	Test#3

- # Test Bench # 1(BK1B1254C)

This test is used to measure the output of Linear Regulators with respect to input. Here the dc voltage is given as an input and we calculated the voltage across the output terminal. This regulator step down to constant voltage equal to 3.3V. Below, I have attached the sim_adms file that represents how to test the Output voltage in LT-Spice.

```
.tran 10U 500M 0 1U
.include "..\..\genhdl\Bk1B1254C_3V3_100mA_LDO_Regulator_V1\Bk1B1254C_3V3_100mA_LDO_Regulator_V1.spi"
VEN EN_3V3 0 DC 3.3
VGND DGND 0 DC 0
VSUPPLY VAL 0 PULSE (1 20 1U 500M )
*******end of additional commands********
.end
```

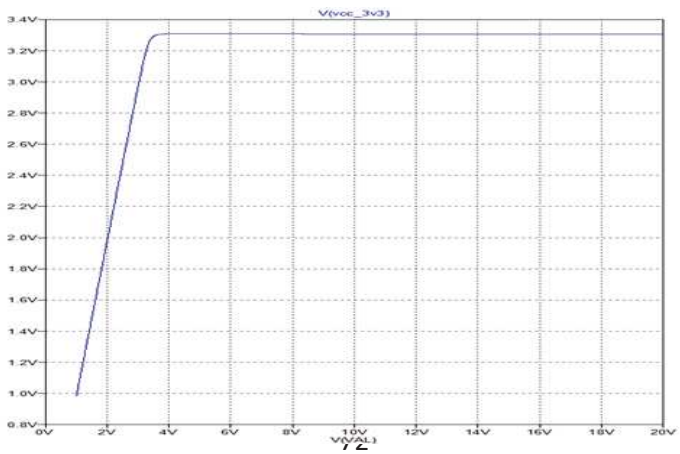


Fig 4.43: Output Vs Input Voltage of BK1B1254C_3V3_100mA_LDO_Regulator

- ## Test Bench # 2(BK1B1254C)

In this test we applied Montecarlo approach in order to evaluate the error introduced by the manufacturing tolerances of the resistors in the main circuit. For this, I zoom in the output voltage V (PDBINT) plot and observed the range of output value in which we select only the lines which are nearer to each other and then apply the standard deviation formula in order to approximate the tolerance. Adding step command in previous sim_adms file is used that contains the input parameters of boost converter in LT-Spice.

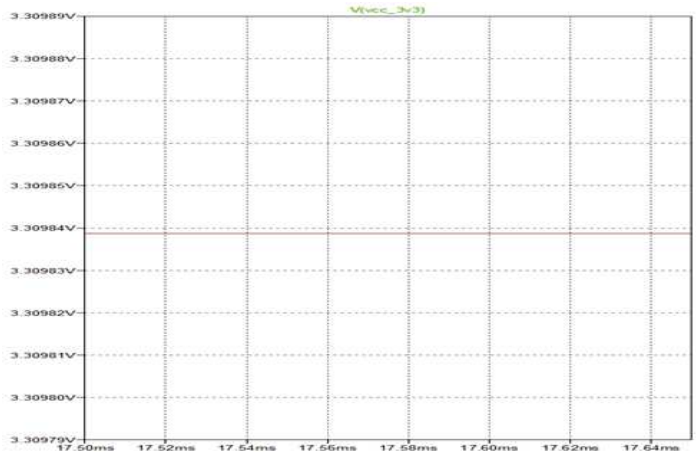


Fig 4.44: Tolerance of BK1B1254C_3V3_100mA_LDO_Regulator

Here, the obtained uncertainty is about 0%.

- ## Test Bench # 3(BK1B1254C)

This test is used to measure the maximum supply current across the circuit. For this, sink current flow across the load resistance. In simulation of this Linear Regulators, I will get more or less the same value of sink current that is 100uA. Below, I have attached the sim_adms file that represents how to test the maximum supply current of this regulator in LT-Spice.

```
.tran 0 0.1 0.001
.include "..\..\genhdl\Bk1B1254C_3V3_100mA_LDO_Regulator_V1\Bk1B1254C_3V3_100mA_LDO_Regulator_V1.spi"
VGND DGND 0 DC 0
VREFERENXCE EN_3V3 0 DC 3.3
VSUPPLY VAL 0 DC 13
RSINK VCC_3V3 0 33
******end of additional commands*******
.end
```

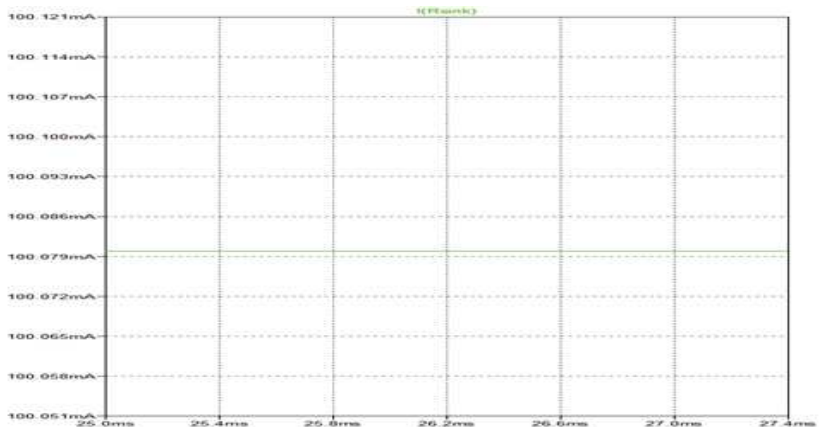


Fig 4.45: Maximum Supply Current of BK1B1254C_3V3_100mA_LDO_Regulator

Here the expected values of sink current is calculated as

$$\text{Imax} = \frac{V}{\text{Rsink}} = \frac{3.3}{33} = 100\text{mA}$$

- ## Test Bench # 7(BK1B1254C)

This test is used to measure the change of output voltage by changing the temperature. Below, I have attached the sim_adms file that represents how to test the output of this regulator by changing the temperature in LT-Spice.

```
.dc TEMP -50 150 5
.include "..\..\genhdl\Bk1B1254C_3V3_100mA_LDO_Regulator_V1\Bk1B1254C_3V3_100mA_LDO_Regulator_V1.spi"
VGND DGND 0 DC 0
VREFERENXCE EN_3V3 0 DC 3.3
VSUPPLY VAL 0 DC 13
*******end of additional commands********
.end
```

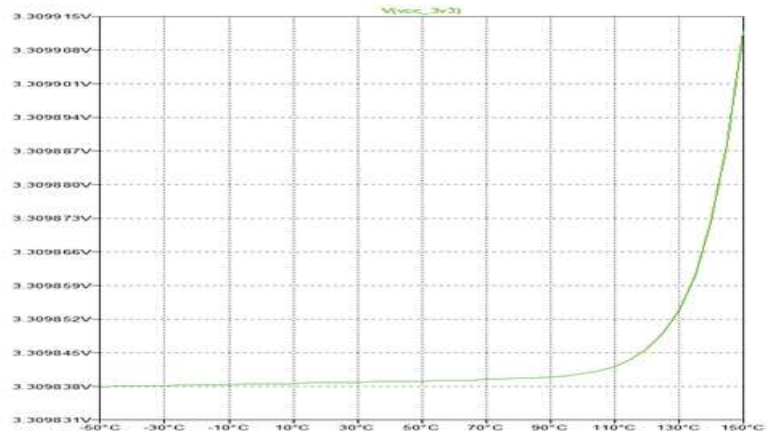


Fig 4.46: Temperature Vs Output Voltage of BK1B1254C_3V3_100mA_LDO_Regulator

Here we will mention the maximum and minimum temperature effect on the output voltage.
At -50 degree centigrade: VCC=3.309V
At 125 degree centigrade: VCC=3.309V

- ## Test Bench # 8(BK1B1254C)

This test is used to measure the input current of Linear Regulator in time domain. Here the DC voltage and Enable pulse is given as an input. Below, I have attached the sim_adms file that represents how to test the input current of this regulator in LT-Spice.

```
.tran 0 0.1 0.001
.include "..\..\genhdl\Bk1B1254C_3V3_100mA_LDO_Regulator_V1\Bk1B1254C_3V3_100mA_LDO_Regulator_V1.spi"
VGND DGND 0 DC 0
VREFERENXCE EN_3V3 0 DC 3.3
VSUPPLY VAL 0 DC 13
RSINK VCC_3V3 0 33
*******end of additional commands********
.end
```

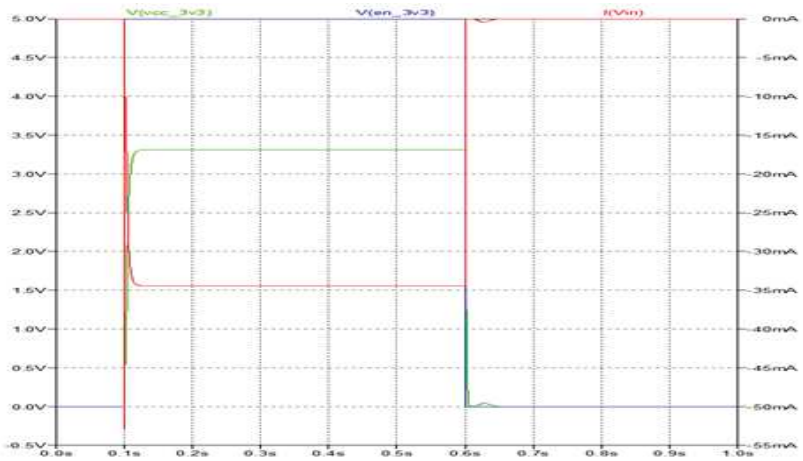


Fig 4.47: Input Current of BK1B1254C_3V3_100mA_LDO_Regulator

Here we calculated the input current of this DC voltage.

Input Current=I (Vin) =35mA

4.14.1 Spice Netlist of BK1254C_3V3_LDO_Regulator:

Once the schematic is created, it is netlisted in the Design Capture of the Mentor Graphics (Simulation→Netlist). It generates a spice netlist which can be used for simulating in the LTSpice as shown below. Here I have attached the genhdl file that shows all the components of this linear regulator and how they are connected in the schematic.

```
* Project Bk1B1254C_3V3_100mA_LDO_Regulator_V1
* Mentor Graphics Wirelist Created with Version 6.4.002
* File created Fri Feb 17 16:01:18 2017
* Inifile   :
* ConfigFile:  C:\MentorGraphics\7.9.4EE\SDD_HOME\standard\wspice.cfg
* Options   :  -__ -.spi -h -$ -7 -kC:\MentorGraphics\7.9.4EE\SDD_HOME\standard\wspice.cfg bk1b1254c_3v3_100ma_ldo_regulator_v1
* Levels    :
*
R1I241 VCC_3V3 VCC_3V3 0
*Warning: No Value For R1I241.Defaulting to 0
X1I234 VAL DGND EN_3V3 XSIG010007 VCC_3V3 lt1761-3.3
C1I213 VCC_3V3 DGND {MC( 10.000000U , 10.000000 /100)} TC=10.000000U
C1I204 VCC_3V3 XSIG010007 {MC( 10.000000N , /100)} TC=
C1I193 VAL DGND {MC( 1000.000000N , 15.000000 /100)} TC=10.000000U
* Dictionary 0
*Warning : No ground node (Label a net GND)

.include "..\..\genhdl\Bk1B1254C_3V3_100mA_LDO_Regulator_V1\Bk1B1254C_3V3_100mA_LDO_Regulator_V1_sources.spi"
.include "..\..\sym\lt1761-3.3.mod"
```

4.15 Testing of Switching Regulator BK1B1254B_3V3

Class BK1B1254B_3V3_100mA_Switching_Regulator:

This regulator converts VAL() input to VCC_3V3() output that give power to all the subsystem of 1B8_CubePMT instead of processor. So there is no any involvement of this regulator with the processor. It draws high current from the power supply so that's why it consumes more power and contains a lot of noise problem. The schematic of the 3.3V Switching Regulator BK1B1254B_3V3_100mA_Switching_Regulator is shown in below Figure 4.48.

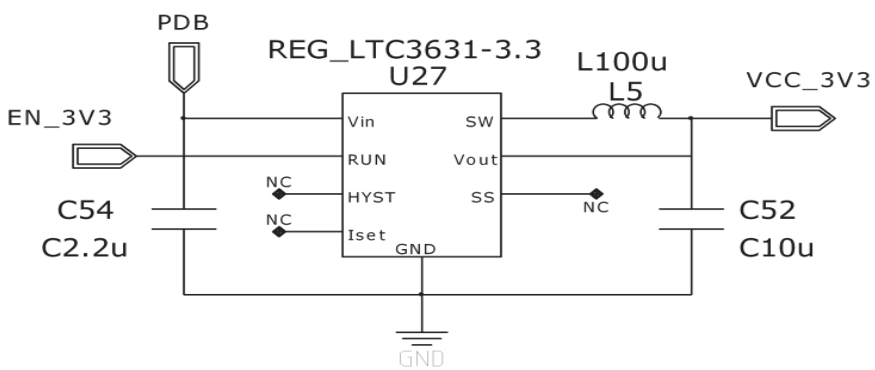


Fig 4.48: Schematic diagram of BK1B1254B_3V3_100mA_Switching_Regulator

Testing of Switching Regulator BK1B1254B_3V3_100mA_Switching_Regulator are given below.

Serial #	Parameters	Expected Value	Current Result	Verification	Pass/Fail	Test Bench
1	Maximum Supply Current(A)	100mA	100mA	Isink=VC_3V3/RLOAD=3.3/33=100mA or I(Rload)=100mA	Pass	Test #3
2	Input Voltage(VAL)	Min:4.5 Max:45	Min:4.5 Max:45	I/P's 5 10 15 20 — O/P's 3.3 3.3 3.3 3.3	Pass	Test#1
3	Tolerance(%)	0	0	By Monte Carlos Approach	Pass	Test#2

Pin VAL ():

Serial #	Parameters	Expected Value	Current Result	Verification	Pass/Fail	Test Bench
1	Voltage Min(V)	4.5	4.5	VCC_3V3=3.3	Pass	Test#1
2	Voltage Max(V)	45	45	VCC_3V3=3.3	Pass	Test#1

Pin EN_3V3 ():

Serial #	Parameters	Expected Value	Current Result	Verification	Pass/Fail	Test Bench
1	Fixed Voltage(V)	3.3	3.3	VEN EN_3V3 0 DC 3.3	Pass	Test#1

Pin VCC_3V3 ():

Serial #	Parameters	Expected Value	Current Result	Verification	Pass/Fail	Test Bench
1	Output Range(V)	3.3	3.3	VCC_3V3=3.3	Pass	Test#1

Pin GND ():

Serial #	Parameters	Expected Value	Current Result	Verification	Pass/Fail	Test Bench
1	Supply Current Peak(A)	0.1	0.1	Isink=VCC_3V3/RLOAD=3.3/33=100mA	Pass	Test#3

- ## Test Bench # 1(BK1B1254B)

This test is used to measure the output of Switching Regulators in time domain. Here we gave the DC voltage as an input and we calculated the voltage across the output terminal. This regulator gives 3.3V (to all subsystem except processor). This regulator generates switching voltage (like charging and discharging) across the SW terminal of the regulator. Below plot has already been checked from the data sheet. Here, I have attached the sim_adms file that represents how to test the output of switching regulator in LT-Spice.

```
.tran 0.1 1 0
.include "..\..\genhdl\Bk1B1254B_3V3_100mA_Regulator_V1\Bk1B1254B_3V3_100mA_Regulator_V1.spi"
VGND DGND 0 DC 0
VEN EN_3V3 0 DC 3.3
*VIN VAL 0 DC 10
VIN VAL 0 PULSE (0 4.5 10m 0.1U 0.1 100M )
RLOAD VCC_3V3 0 100
******end of additional commands*******
.end
```

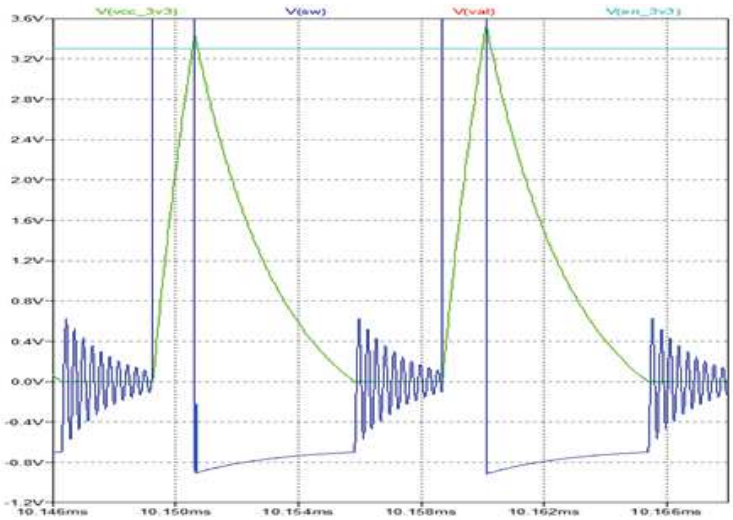


Fig 4.49: Output Vs Input Voltage of BK1B1254B_3V3_100mA_Switching_Regulator

- ## Test Bench # 2(BK1B1254B)

This test is used to measure the maximum supply current across the circuit. For this, sink current flow across the load resistance. For the simulation of this Switching Regulators, we will get the same value of sink current that is 100mA with respect to expected value.

```
.tran 0.1 1 0
.include "..\..\genhdl\Bk1B1254B_3V3_100mA_Regulator_V1\Bk1B1254B_3V3_100mA_Regulator_V1.spi"
VGND GND 0 DC 0
VEN EN_3V3 0 DC 3.3
*VIN VAL 0 DC 10
VIN VAL 0 PULSE (0 10 10m 0.1U 0.1 100M )
RLOAD VCC_3V3 0 33
******end of additional commands*******
.end
```

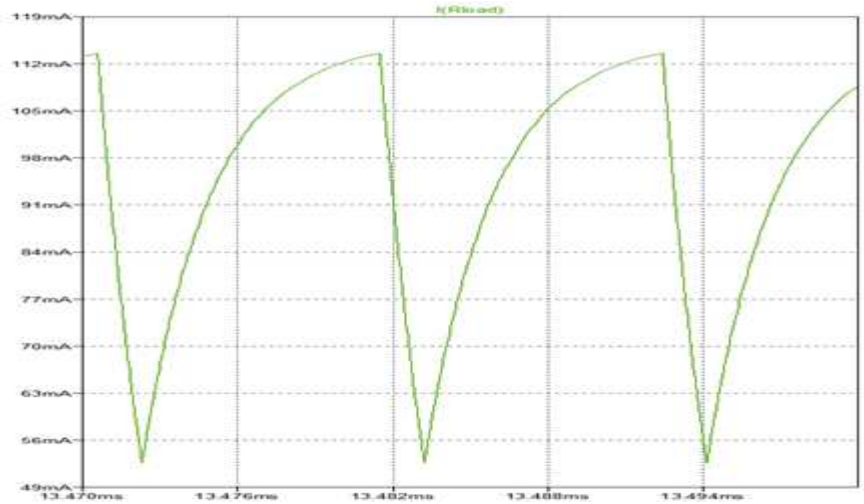


Fig 4.50: Maximum Supply Current of BK1B1254B_3V3_100mA_Switching_Regulator

Here the expected values of maximum supply current is calculated as

$$Imax = \frac{VC\_3V3}{Rload} = \frac{3.3}{33} = 100mA$$

4.15.1 Spice Netlist of BK1254B_3V3_100mA_Regulator_V1:

Once the schematic is created, it is netlisted in the Design Capture of the Mentor Graphics (Simulation→Netlist). It generates a spice netlist which can be used for simulating in the LTSpice as shown below. Here I have attached the genhdl file that shows all the components of this switching regulator and how they are connected in the schematic.

```
* Project Bk1B1254B_3V3_100mA_Regulator_V1
* Mentor Graphics Wirelist Created with Version 6.4.002
* File created Fri Nov 04 18:57:14 2016
* Inifile   :
* ConfigFile:  C:\MentorGraphics\7.9.4EE\SDD_HOME\standard\wspice.cfg
* Options   :  -__ -.spi -h -$ -7 -kC:\MentorGraphics\7.9.4EE\SDD_HOME\standard\wspice.cfg bk1b1254b_3v3_100ma_regulator_v1
* Levels    :
*
L1I455 VCC_3V3 XSIG010010 {MC( 100.000000U , 20.000000 /100)} RSER=1.820000
X1I609 XSIG010010 VAL XSIG010005 XSIG010012 EN_3V3 VCC_3V3 XSIG010004 DGND LTC3631-33X
C1I474 VAL DGND {MC( 2.200000U , 10.000000 /100)} TC=10.000000U
R1I587 VCC_3V3 VCC_3V3 0
*Warning: No Value For R1I587.Defaulting to 0
C1I512 VCC_3V3 DGND {MC( 10.000000U , 10.000000 /100)} TC=10.000000U
* Dictionary 0
*Warning : No ground node (Label a net GND)
*Warning: Could not open data file sym\ltc3631-3.3.mod

.include "..\..\genhdl\Bk1B1254B_3V3_100mA_Regulator_V1\Bk1B1254B_3V3_100mA_Regulator_V1_sources.spi"
.include "..\..\sym\LTC3631-33X.mod"
```

4.16 Testing of Switching Regulator BK1B1253B_5V

Class BK1B1253B_5V_100mA_Switching_Regulator:
This regulator converts VAL () input to VCC_5V () output in order to give VCC_5V () to all the subsystem of 1B8_CubePMT. It also draws high current from the power supply so that's why it consumes more power and contains a lot of noise problem. It is enabled EN_5V () from the Tile processor. The schematic of the 5V Switching Regulator BK1B1253B_5V_100mA_Switching_Regulator is shown in below Figure 4.51.

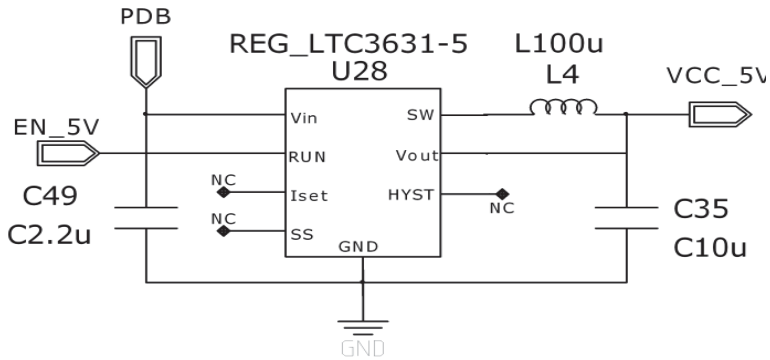


Fig 4.51: Schematic diagram of BK1B1253B_5V_100mA_Switching_Regulator

Testing Results of Switching Regulator BK1B1253B_5V_100mA_Switching_Regulator are given below.

Serial #	Parameter	Expected Value	Current Result	Verification	Pass/Fail	Test Bench
1	Maximum Supply Current(A)	100mA	100mA	Isink=VCC_5V/RLOAD=5/50=100mA or I(Rload)=100mA	Pass	Test #3

2	Input Voltage(PDB)	Min:4.5 Max:45	Min:4.5 Max:45	I/P's 3.8 10 15 20	O/P's 5 5 5 5	Pass	Test#1
3	Tolerance(%)	0	0	By Monte Carlos Approach		Pass	Test#2

Pin VAL ():

Serial #	Parameter	Expected Value	Current Result	Verification	Pass/Fail	Test Bench
1	Voltage Min(V)	4.5	4.5	VCC_5V=5	Pass	Test#1
2	Voltage Max(V)	45	45	VCC_5V=5	Pass	Test#1

Pin EN_5V ():

Serial #	Parameters	Expected Value	Current Result	Verification	Pass/Fail	Test Bench
1	Fixed Voltage(V)	5	5	VEN EN_5V 0 DC 5	Pass	Test#1

Pin VCC_5V ():

Serial #	Parameters	Expected Value	Current Result	Verification	Pass/Fail	Test Bench
1	Output Range(V)	5	5	VCC_5V=5	Pass	Test#1

Pin DGND ():

Serial #	Parameters	Expected Value	Current Result	Verification	Pass/Fail	Test Bench
1	Supply Current Peak(A)	0.1	0.1	Isink=VCC_5V/RLOAD=5/50=100mA	Pass	Test#3

- # Test Bench # 1(BK1B1253B)

This test is used to measure the output of Switching Regulators in time domain. Here we gave the DC voltage as an input and we calculated the voltage across the output terminal. This regulator gives 5V (to all subsystem).This generates switching voltage (like charging and discharging) across the SW terminal of the regulator. Below plot has already been checked from the data sheet. Below, I have attached the sim_adms file that represents how to test the output of switching regulator in LT-Spice.

```
.tran 0.1 1 0
.include "..\..\genhdl\Bk1B1253B_5V_100mA_Regulator_V1\Bk1B1253B_5V_100mA_Regulator_V1.spi"
VEN EN_5V 0 DC 5
VGND DGND 0 DC 0
*VIN VAL 0 DC 10
VIN VAL 0 DC 36 PULSE (0 36 10m 0.1U 0.1 100M )
RLOAD VCC_5V 0 145
.include "LTC3631-5.sub"
*******end of additional commands********
.end
```

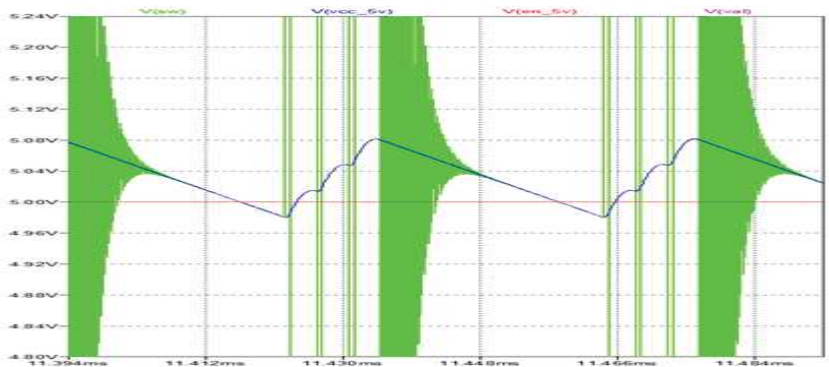


Fig 4.52: Output waveform of BK1B1253B_5V_100mA_Switching_Regulator

- ## Test Bench # 2(BK1B1253B)

This test is used to measure the maximum supply current across the circuit. For this, sink current flow across the load resistance. In simulation of this Switching Regulator, we will get the same value of sink current that is 100mA with respect to expected value. Below, I have attached the sim_adms file that represents how to test the maximum supply current of this regulator in LT-Spice.

```
.tran 0.1 1 0
.include "..\..\genhdl\Bk1B1253B_5V_100mA_Regulator_V1\Bk1B1253B_5V_100mA_Regulator_V1.spi"
VEN EN_5V 0 DC 5
VGND DGND 0 DC 0
*VIN VAL 0 DC 10
VIN VAL 0 DC 10 PULSE (0 10 10m 0.1U 0.1 100M )
RLOAD VCC_5V 0 50
.include "LTC3631-5.sub"
*******end of additional commands*******
.end
```

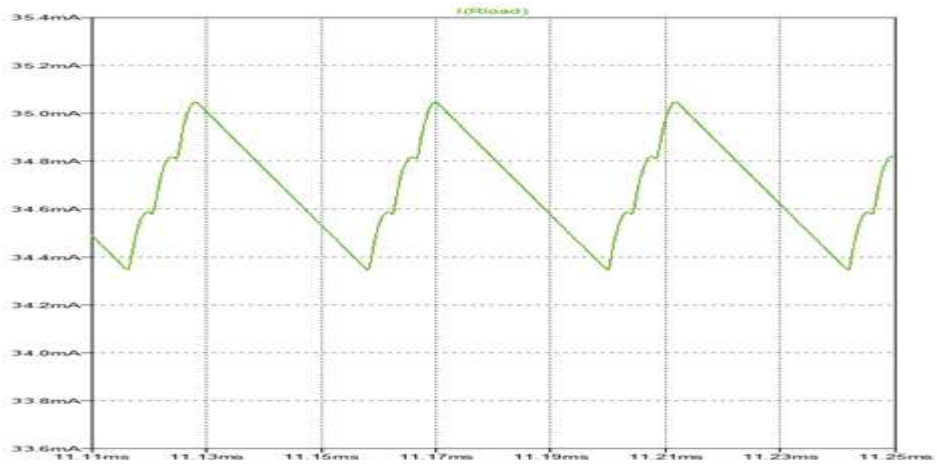


Fig 4.53: Maximum Supply current of BK1B1253B_5V_100mA_Switching_Regulator

Here the expected values of maximum supply current is calculated as

$$\text{Imax} = \frac{\text{VCC\_5V}}{\text{Rload}} = \frac{5}{50} = 100\text{mA}$$

4.16.1 Spice Netlist of BK1253B_5V_100mA_Regulator_V1:

Once the schematic is created, it is netlisted in the Design Capture of the Mentor Graphics (Simulation→Netlist). It generates a spice netlist which can be used for simulating in the LTSpice as shown below. Here I have attached the genhdl file that shows all the components of this switching regulator and how they are connected in the schematic.

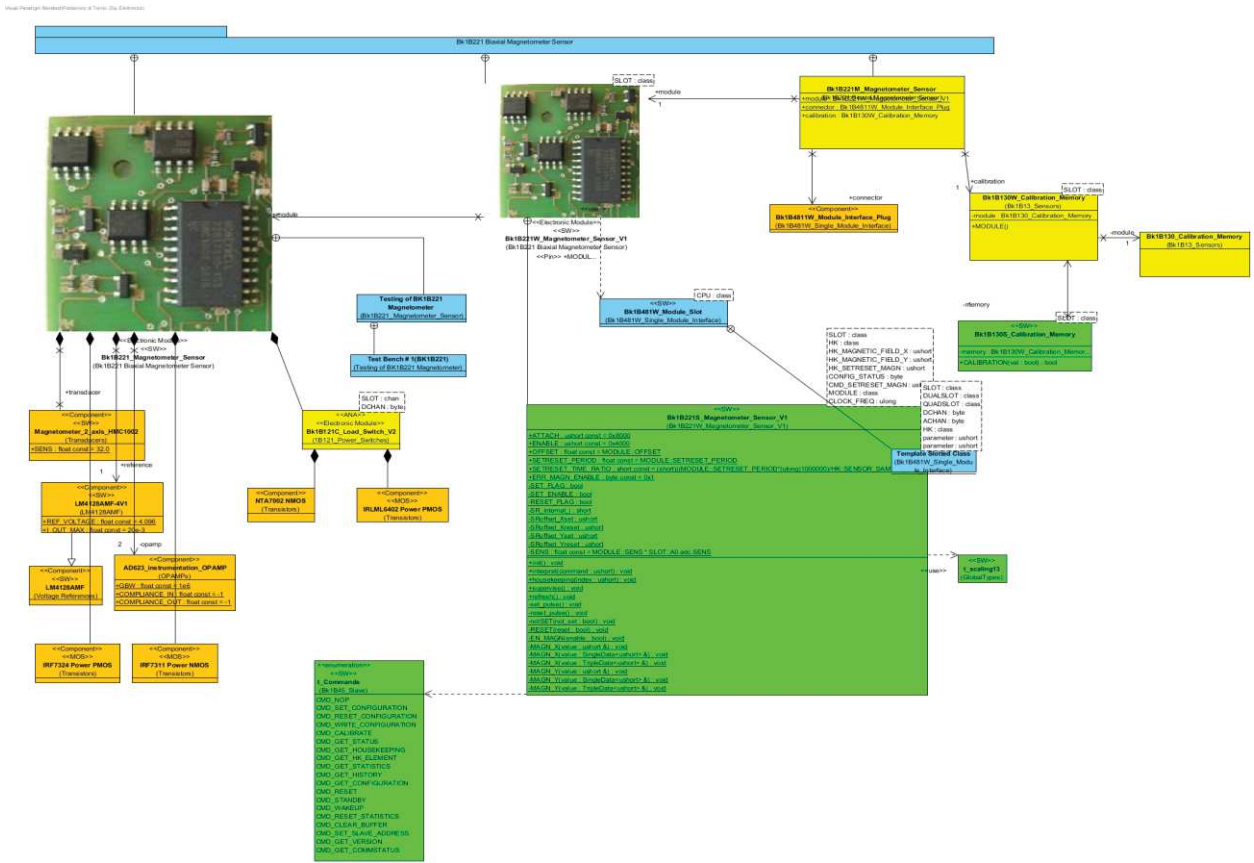
```
* Project Bk1B1253B_5V_100nA_Regulator_V1
* Mentor Graphics Wirelist Created with Version 6.4.002
* File created Fri Nov 04 18:44:18 2016
* Inifile    :
* ConfigFile:  C:\MentorGraphics\7.9.4EE\SDD_HOME\standard\wspice.cfg
* Options    :  -__ -.spi -h -$ -7 -kC:\MentorGraphics\7.9.4EE\SDD_HOME\standard\wspice.cfg bk1b1253b_5v_100na_regulator_v1
* Levels     :
*
L1I253 VCC_5V SW {MC( 100.000000U , 20.000000 /100)} RSER=1.820000
R1I220 VCC_5V VCC_5V VALUE
X1I350 SW VAL N1N186 N1N91 EN_5V VCC_5V N1N185 DGND LTC3631-5X
C1I244 VCC_5V DGND {MC( 10.000000U , 10.000000 /100)} TC=10.000000U
C1I235 VAL DGND {MC( 2.200000U , 10.000000 /100)} TC=10.000000U
* Dictionary 0
*Warning : No ground node (Label a net GND)
*Warning: Could not open data file sym\ltc3631-5.mod

.include "..\..\genhdl\Bk1B1253B_5V_100nA_Regulator_V1\Bk1B1253B_5V_100nA_Regulator_V1_sources.spi"
.include "..\..\sym\LTC3631-5X.mod"
```

4.17 Bk1B221_Magnetometer_Sensor

A sensor that measures the earth magnetic field for the determination of attitude parameter is known as Magnetometer.Bk1B221_Magnetometer_Sensor is a 2-axis magnetic sensor for space applications based on a Magnetometer_2_axis_HMC1002 from Honeywell. The bridge-based reading of magnetic field for each of the two orthogonal axes is converted to a single ended voltage signal for each axis, available on the MAGN_X() and MAGN_Y() outputs.

4.17.1 Description:

The circuit operates with two supply voltage (3V3 (), 5V ()) and it requires a reference voltage REF_3V (). The Bk1B221_Magnetometer_Sensor can be disabled by pulling down the signal EN_MAGN () both to reduce power consumption and to isolate the circuit in case of faults. The two inputs notSET() and RESET() are used to trigger the so-called set-reset operation of the magnetic field transducer Magnetometer_2_axis_HMC1002, as detailed in the corresponding datasheet. Because of its high current consumption when active (up to 50mW), this sensor should be activated only when necessary. When activated once per second, for a period of 1ms, its average power consumption becomes around 50µW. For optimal performance, the system requires periodic activation of a so-called "set/reset" operation, as per datasheet of Magnetometer_2_axis_HMC1002. Suggested activation of this procedure is every 10 minutes approximately, unless exposed to magnetic fields higher than 2 gauss. When earth magnetic field (-0.625 to 0.625 G) is incident on



this sensor, it give the output (0 to 2.5V) to the tile processor. It is because of two Wheatstone bridge A and B that convert this incident magnetic field to two differential output voltage VA and VB. The class diagram of Bk1B1251_Linear and Switching Regulators is shown in below Figure 4.54.

Figure 4.54: Class diagram of Bk1B221_Magnetometer

Schematic diagram of BK1B221_Magnetometer are given below in figure 4.55.

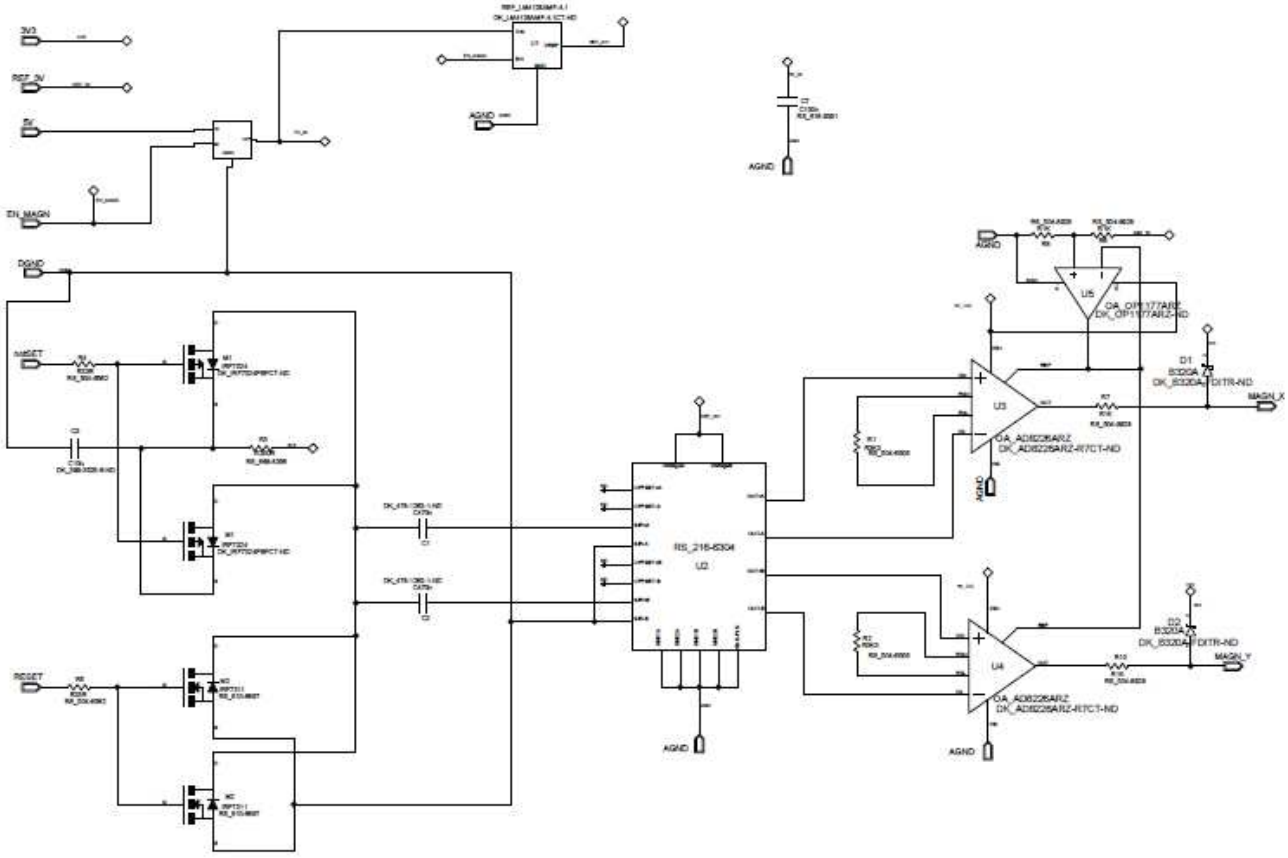


Fig 4.55: Schematics of a Bk1B221_Magnetometer_Sensor.

4.17.2 Specifications:

Parameter	Min	Max	Unit
Channels (X and Y)		2	
Supply voltage	5	12	V
Field range	-2	+2	gauss
Accuracy (with internal calibration)			
Linearity		0.005	gauss
Hysteresis		0.001	gauss
Temperature sensitivity	-0.28	-0.32	%/oC
Cross axis effect (when calibrated)		0.3	%
Settling time after activation		1	ms
Power consumption when active,		50	mW

at 5V supply			
Power consumption when used once per second, 1ms activation		50	µW
Energy per set/reset operation		5	µJ
Operating temperature	-40	80	oC

4.17.3 Testing of BK1B221 Magnetometer

Class Bk1B221_Magnetometer_Sensor:
Testing results of Bk1B221_Magnetometer_Sensor are given below.

Serial #	Parameter	Expected Value	Current Result	Verification	Pass/Fail	Test bench
1	Supply Current (A)	without load:0.000150 with Rload:0.000136	without load:0.000150 with load:0.000136	1.5/10k=0.000150A 1.36/10k=0.000136A	Pass	Test#1
2	Output Voltage with no Rload (V)	1.5 1.709 1.29	1.5 1.709 1.29	FIELD=0G:- MAGN_X=Voffset(1.5)+Sensitivity(0.2093V/G)=1.50V FIELD=1G:- MAGN_X=Voffset(1.5)+Sensitivity(0.2093V/G)=1.709V FIELD=-1G:- MAGN_X=Voffset(1.5)+Sensitivity(0.2093V/G)=1.29V	Pass	Test#1
3	Output Voltage with Rload=10K (V)	1.36 1.55 1.17	1.36 1.55 1.17	MAGN_X=10k/(10k+1k)*1.5=1.36V MAGN_X=10k/(10k+1k)*1.709=1.55V MAGN_X=10k/(10k+1k)*1.29=1.17V	Pass	Test#1

Pin 5V ():

Serial #	Parameter	Expected Value	Current Result	Verification	Pass/Fail	Test bench
1	Input DC voltage (V)	5	5	V5V N5V 0 DC 5	Pass	Test#1

Pin REF_3V ():

Serial #	Parameter	Expected Value	Current Result	Verification	Pass/Fail	Test bench
1	Input DC voltage (V)	3	3	VREF REF_3V 0 DC 3	Pass	Test#1

Pin DGND ():

Serial #	Parameter	Expected Value	Current Result	Verification	Pass/Fail	Test bench
1	Digital Ground (V)	0	0	VDGND AGND 0 DC 0	Pass	Test#1

Pin AGND ():

Serial #	Parameter	Expected Value	Current Result	Verification	Pass/Fail	Test bench
1	Analog Ground (V)	0	0	VAGND AGND 0 DC 0	Pass	Test#1

Pin EN_MAGN ():

Serial #	Parameter	Expected Value	Current Result	Verification	Pass/Fail	Test bench
1	Input Enable Pulse (V)	5	5	VEN EN_MAGN 0 DC 5 PULSE (0 5 10U 100n 100N 100M 200M)	Pass	Test#1

Pin RESET ():

Serial #	Parameter	Expected Value	Current Result	Verification	Pass/ Fail	Test bench
1	Input Reset Pulse (V)	3.3	3.3	VRESET RESET 0 DC 3.3 PULSE (3.3 0 100U 100N 100N 10U 400U)	Pass	Test#1

Pin notSET():

Serial #	Parameter	Expected Value	Current Result	Verification	Pass/Fail	Test bench
1	Input notReset Pulse (V)	3.3	3.3	VnotSET notSET 0 DC 3.3 PULSE (3.3 0 102U 100N 100N 6U 400U)	Pass	Test#1

Pin MAGN_X ():

Serial #	Parameter	Expected Value	Current Result	Verification	Pass/ Fail	Test bench
1	Output Voltage with no Rload (V)	1.5 1.70 1.285	1.5 1.70 1.285	FIELD=0G:MAGN_X=Voffset(1.5)+Sensitivity(0.2093V/G)=1.50V FIELD=1G:MAGN_X=Voffset(1.5)+Sensitivity(0.2093V/G)=1.709V FIELD=-1G:MAGN_X=Voffset(1.5)+Sensitivity(0.2093V/G)=1.29V	Pass	Test#1
2	Output Voltage with Rload=10K (V)	1.36 1.55 1.17	1.36 1.55 1.17	MAGN_X=10k/(10k+1k)*1.5=1.36V MAGN_X=10k/(10k+1k)*1.709=1.55V MAGN_X=10k/(10k+1k)*1.29=1.17V	Pass	Test#1

Pin MAGN_Y ():

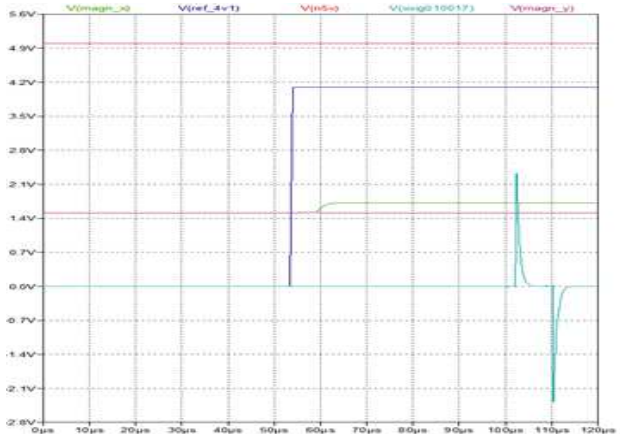
Serial #	Parameter	Expected Value	Current Result	Verification	Pass/ Fail	Test bench
1	Output Voltage with no Rload (V)	1.5 1.709 1.29	1.5 1.709 1.29	FIELD=0G:-MAGN_Y=Voffset(1.5)+Sensitivity(0.2093V/G)=1.50V FIELD=1G:-MAGN_Y=Voffset(1.5)+Sensitivity(0.2093V/G)=1.709V FIELD=-1G:-MAGN_Y=Voffset(1.5)+Sensitivity(	Pass	Test#1

				0.2093V/G)=1.29V		
2	Output Voltage with Rload=10K (V)	1.36 1.55 1.17	1.36 1.55 1.17	MAGN_Y=10k/(10k+1k)*1.5=1.36V MAGN_Y=10k/(10k+1k)*1.709=1.55V MAGN_Y=10k/(10k+1k)*1.29=1.17V	Pass	Test#1

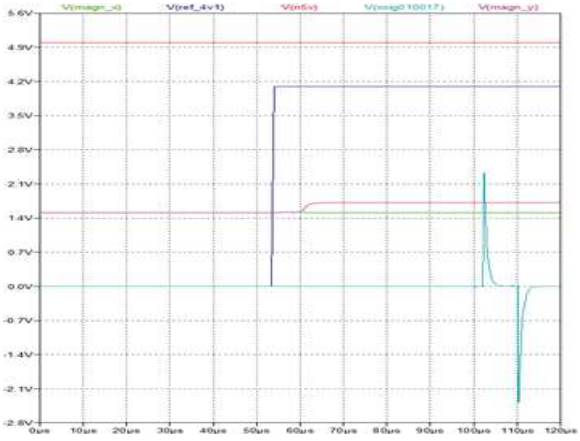
- ## Test Bench # 1(BK1B221)

This test is used to measure the output of Magnetometer in the form of Voltage with respect to incoming low magnetic field (in range of -2 to 2 Gauss). Here the constant 4.1V is given as an input to the magnetometer with the help of LM4128 Regulator and BK1B121C Load Switch. On the other hand magnetometer receives constant pulses from the set/reset circuitry in order to generate the output voltage across magnetometer accordingly. Below, I have attached the sim_adms file that represents how to test the output of magnetometer in the form of voltage when it receive magnetic field across its input in LT-Spice.

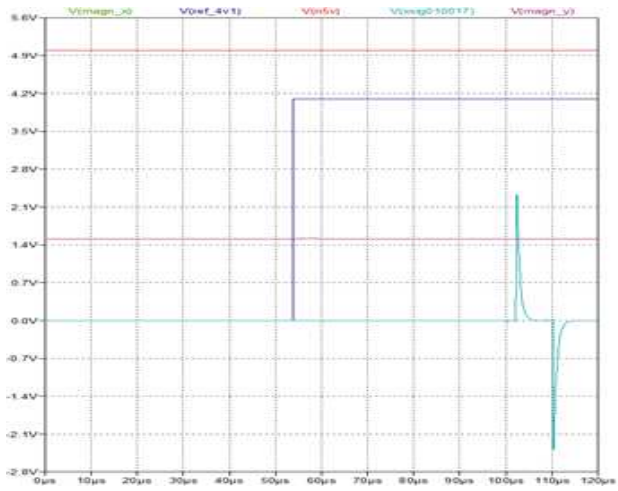
```
.tran 500U 120u 0 400U
.include "..\..\genhdl\BK1B221_Magnetometer_V1\BK1B221_Magnetometer_V1.spi"
VAGND AGND 0 DC 0
VDGND DGND 0 DC 0
V1 N3V3 0 DC 3.3
VREF REF_3V 0 DC 3
V5V N5V 0 DC 5
VREF5V2 N5V_int 0 DC 5
VEN EN_MAGN 0 DC 5 PULSE (0 5 10U 100n 100N 100M 200M)
VRESET RESET 0 DC 3.3 PULSE (3.3 0 100U 100N 100N 10U 400U)
VnotSET notSET 0 DC 3.3 PULSE (3.3 0 102U 100N 100N 6U 400U)
*******end of additional commands********
.end
```



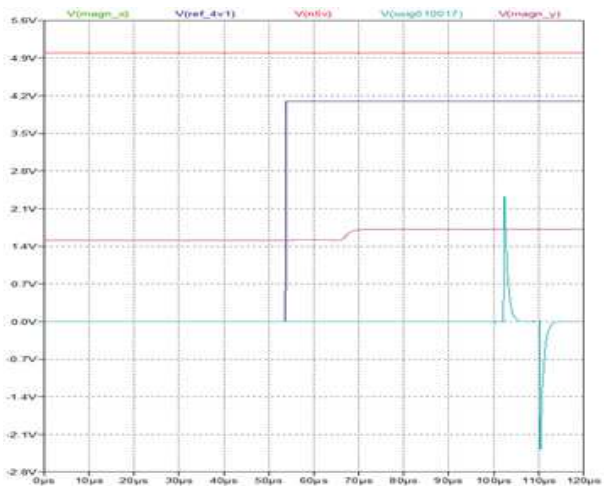
FIELD (0, 1)



FIELD (1, 0)



FIELD (0, 0)



FIELD (1, 1)

The output voltage is calculated from the formula which I am going to mention below.

Sensitivity=Ref. Voltage*Sensitivity of Transducer*Gain

Sensitivity=4.096V*32V/V/T*15.96=2093.1V/T

We know that 1Tesla=10^4*1Gauss. So,

Sensitivity=0.2093V/G

V (OUT) =MAGN_X= Voffset+ Sensitivity* Input Field in Gauss

MAGN_X=1.5+0.2093V/G*0G=1.5V

MAGN_X=1.5+0.2093V/G*1G=1.709V

MAGN_X=1.5+0.2093V/G*-1G=1.29V

This calculation will be the same for bridge B. Below we mentioned the values of simulated results for both Bridge A and Bridge B whose graphs are shown there accordingly.

FIELD_A	FIELD_B	MAGN_X	MAGN_Y
0	0	1.5	1.5
0	1	1.5	1.709
1	0	1.709	1.5
1	1	1.709	1.709
-1	0	1.29	1.5
-1	1	1.29	1.709

4.18 1B111Solar Panel:

Solar panel refers to a panel designed to absorb the sun's rays as a source of energy for generating electricity or heating. It contains solar cells that converts the energy of light directly into electricity by the photovoltaic effect.

4.18.1 Description:

1U 1B8_CubePMT have two solar cells which are made from GaAs material CESI-TJ-CTJH-SolarCell-70x40 whose efficiency is almost 26%.These solar cells are connected in series in order to generate 4.4V from both of them. A simple schottky diode across each solar cell is placed that can help in generating 2.2V from single cell when the other cell becomes damaged. The solar cells are surrounded by ground plane to trap any incoming charged particle. The class diagram of Bk1B111B_Solar_Panel is shown in below Figure 4.56.

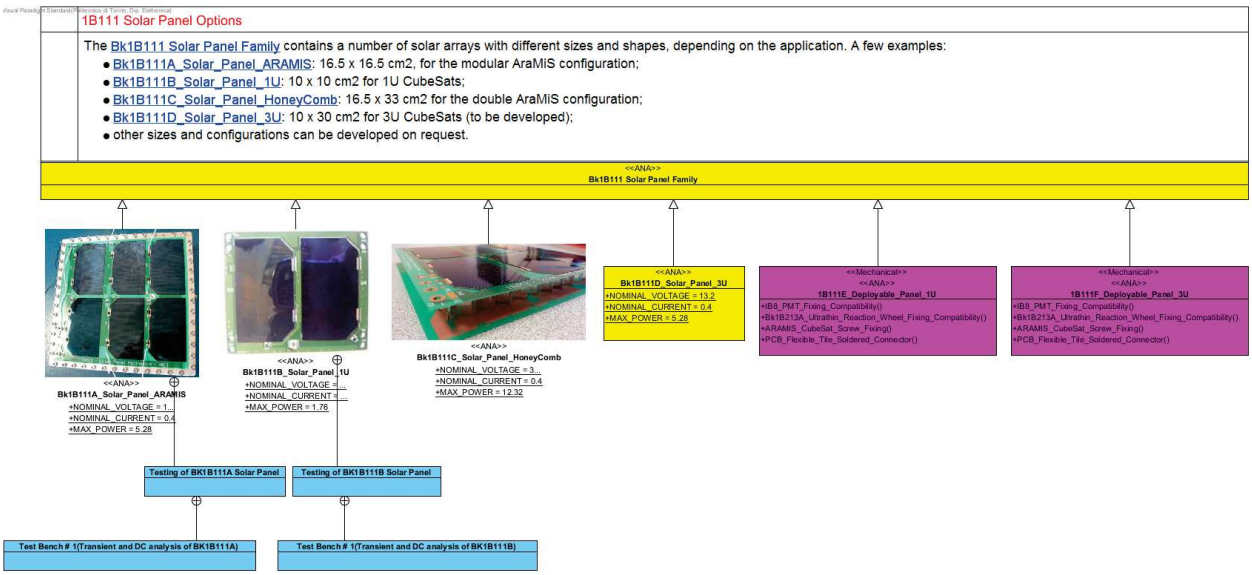


Fig 4.56: Class Diagram of 1B111_Solar_Panels

Schematic diagram of BK1B221_Magnetometer are given below in figure 4.57.

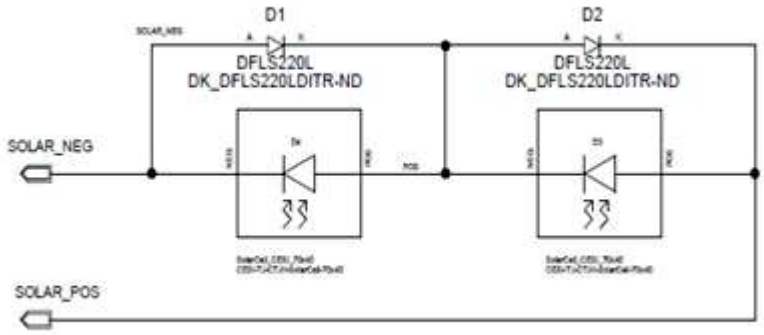


Fig 4.57: Schematic diagram of Bk1B111B_Solar_Panel_1U.

4.18.2 Testing of BK1B111B Solar Panel

Testing results of Bk1B111B_Solar_Panel_1U are given below.

Serial #	Parameter	Expected Value	Current Result	Verification	Pass/ Fail	Test bench
1	Output Voltage in Transient (V)	SOLAR_POS=4.4 POS=2.2 SOLAR_NEG=0	SOLAR_POS=4.4 POS=2.2 SOLAR_NEG=0	.tran 100U 1 0 50M	Pass	Test#1
2	Output Current in DC (A)	I(V2)=0.4A	I(V2)=0.4A	.dc V2 0 5 0.1 I(V2)=0.4A across 4.4V for MPP=1.76W	Pass	TEST#1

Pin SOLAR_POS ():

Serial #	Parameter	Expected Value	Current Result	Pass/Fail	Test bench
1	Output voltage (V)	4.4	4.4	Pass	Test#1

Pin SOLAR_NEG ():

Serial #	Parameter	Expected Value	Current Result	Pass/Fail	Test bench
1	Output voltage (V)	0	0	Pass	Test#1

- **Test Bench # 1(Transient and DC analysis of BK1B111B)**

This test is used to measure the output of Solar Panel by making the spice model of solar cell. Firstly we performed Transient analysis and then DC analysis on LT-Spice for checking the maximum output voltage and current. Here we got the current across the output which is 0.4A up to the maximum output voltage= 4.4V and then fall down. So, we got a constant power equal to 1.76W across maximum power point. Below, I have attached the sim_adms file that represents how to test the transient analysis of solar panel in LT-Spice. Below, I have attached the sim_adms file that represent how to test the DC analysis of solar panel in LT-Spice.

```
.tran 100U 1 0 50M
.include "..\..\genhdl\BK1B111B_Solar_Panel_CubeSat_V1\BK1B111B_Solar_Panel_CubeSat_V1.spi"
VSOLAR_NEG SOLAR_NEG 0 DC 0
*******end of additional commands*******
.end
```

Figure 4.58: Transient Analysis of Bk1B111B_Solar_Panel

```
.dc V2 0 5 0.1
.include "..\..\genhdl\BK1B111B_Solar_Panel_CubeSat_V1\BK1B111B_Solar_Panel_CubeSat_V1.spi"
V2 SOLAR_POS SOLAR_NEG DC 4.4
RLOAD SOLAR_NEG 0 50
*******end of additional commands*******
.end
```

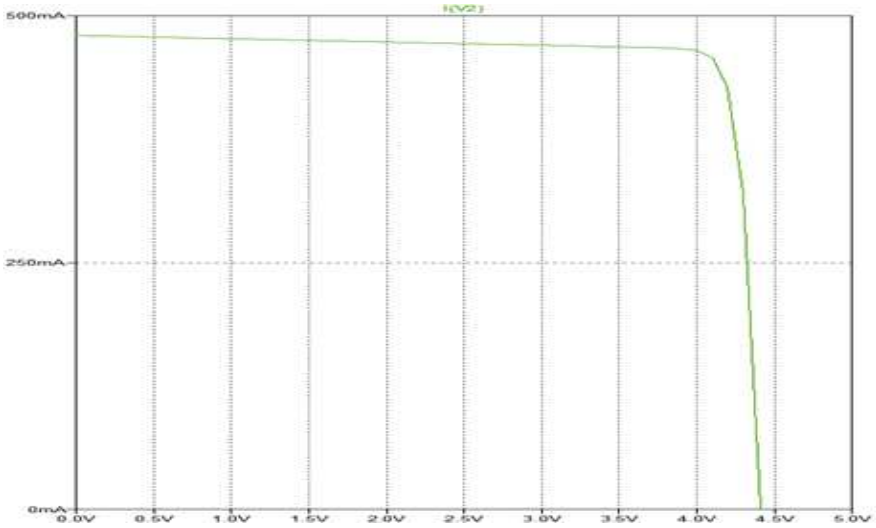


Figure 4.59: DC Analysis of Bk1B111B_Solar_Panel

4.18.3 Spice Netlist of BK111B_Solar_Panel_CubeSat_V1:

Once the schematic is created, it is netlisted in the Design Capture of the Mentor Graphics (Simulation→Netlist). It generates a spice netlist which can be used for simulating in the LTSpice as shown below. Here I have attached the genhdl file that shows all the components of this solar panel and how they are connected in the schematic.

```
* Project BK1B111B_Solar_Panel_CubeSat_V1
* Mentor Graphics Wirelist Created with Version 6.4.002
* File created Fri Nov 25 19:07:17 2016
* Inifile    :
* ConfigFile:  C:\MentorGraphics\7.9.4EE\SDD_HOME\standard\wspice.cfg
* Options    :  -__ -.spi -h -$ -kC:\MentorGraphics\7.9.4EE\SDD_HOME\standard\wspice.cfg bk1b111b_solar_panel_cubesat_v1
* Levels     :
*
X1I371 POS SOLAR_NEG CESI-TJ-CTJH-70x40
X1I378 SOLAR_POS POS CESI-TJ-CTJH-70x40
D1I385 SOLAR_NEG POS DFLS220L
D1I393 POS SOLAR_POS DFLS220L
* Dictionary 0
*Warning : No ground node (Label a net GND)

.include "..\..\sym\CESI-TJ-CTJH-70x40.mod"
.include "..\..\sym\DFLS220L.mod"
```

4.19 1B235_Sun_Sensor

The sensor which generate the voltage cross the output terminal when sun light fall on it is known as Sun Sensor. Its class diagram is shown below in figure 4.60.

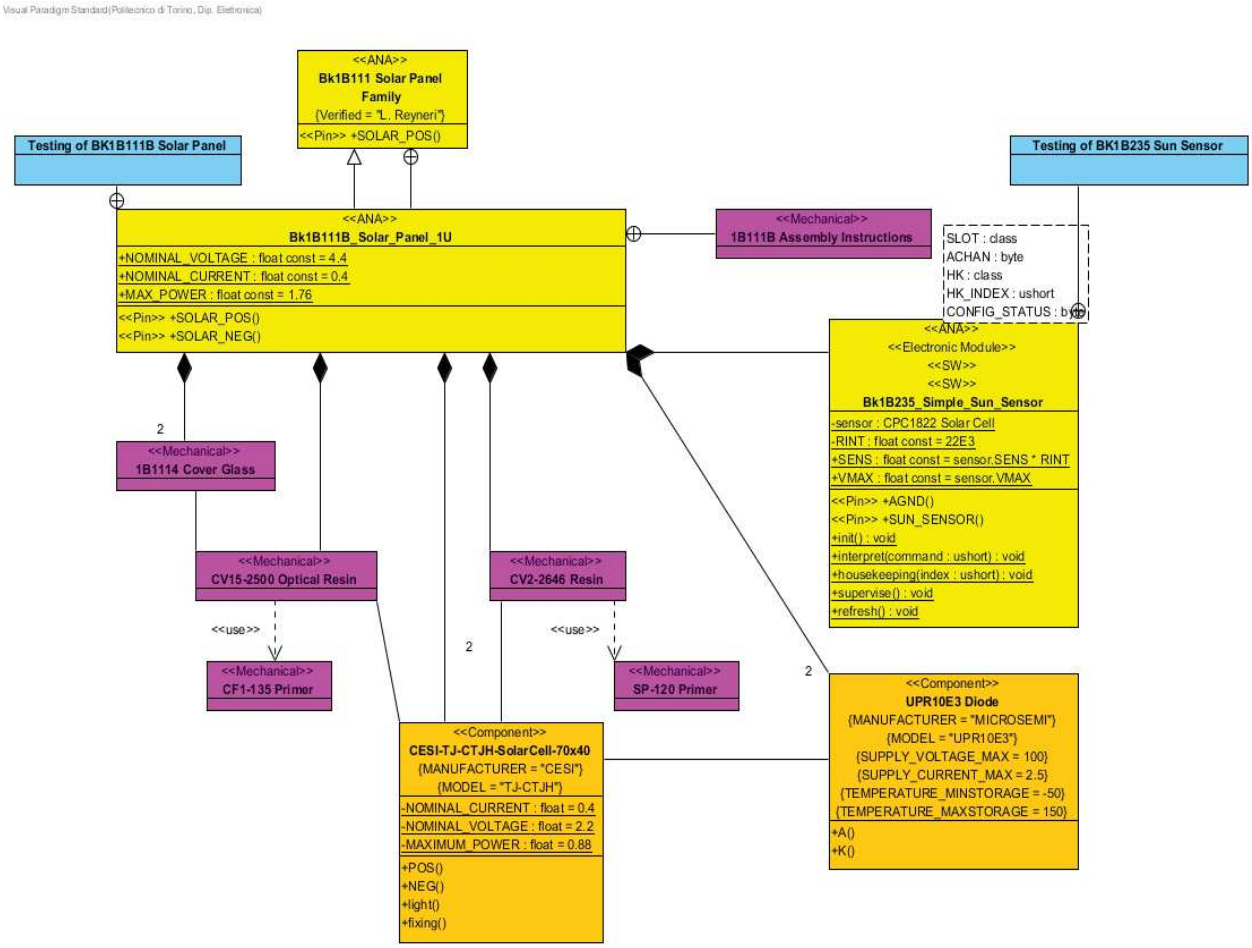


Figure 4.60: Class diagram of Bk1B235_Sun_Sensor

4.19.1 Description:

Solar cell CPC1822 is utilized as sun detector. It is a monolithic photovoltaic string of solar cells. In presence of sun or artificial light it generates a voltage at its output SUN_SENSOR which is sufficient to drive ADC of tile processor. Output resistor keeps the output voltage value within the range of tile processor (0V~2.5V). Schematic diagram of sun sensor is shown in below Figure 4.2. The open circuit voltage of a solar cell is proportional to the cosine of the angle of incident light as given below.

$$V_o = V_{max}\cos(\theta)$$

Where V_{max} = 1.65V +/- 20%

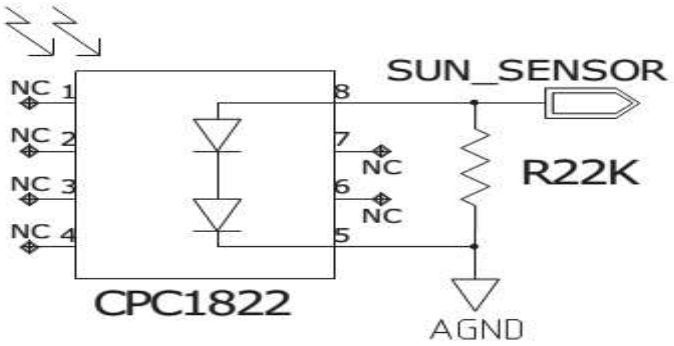


Fig 4.61: Schematic diagram of Bk1B235_Sun_Sensor

4.19.2 Testing of BK1B235 Sun Sensor

Testing results of Bk1B235_Simple_Sun_Sensor is given below.

Serial #	Parameter	Expected Value	Current Result	Verification	Pass/Fail	Test Bench
1	Output Voltage (V)	1.65+/- 20% 1.32<---->1.98	1.65+/- 20% 1.32<---->1.98	1.32V------>I(Vout)=-6.02mA 1.65V----->I(Vout)=-137.28mA 1.98V------>I(Vout)=-1.39A	Pass	Test#1

Pin SUN_SENSOR ():

Serial #	Parameter	Expected Value	Current Result	Pass/Fail	Test Bench
1	Output Voltage (V)	1.65+/- 20% 1.32<---->1.98	1.65+/- 20% 1.32<--->1.98	Pass	Test # 1

Pin AGND ():

Serial #	Parameters	Expected Value	Current Result	Pass/Fail	Test Bench
1	Ground Voltage (V)	0	0	Pass	Test#3

- ## Test Bench # 1(BK1B235)

This test is used to measure the output of Sun Sensor in the form of Voltage with respect to incoming solar energy. Here we gave 4.75V across the output terminal of Sun Sensor and then sweep it from 0V to 5V with step of 0.1. Below, I have attached the sim_adms file that represents how to test the output of Sun Sensor in LT-Spice.

```
.dc VOUT 0 5 0.1
.include "..\..\genhdl\BK1B235_Sun_Sensor\BK1B235_Sun_Sensor.spi"
VAGND AGND 0 DC 0
VOUT SUN_SENSOR AGND DC 4.75
*******end of additional commands********
.end
```

Figure 4.62: Maximum Output Voltage of Bk1B235_Sun_Sensor

4.19.3 Spice Netlist of BK1B235_Sun_Sensor:

Once the schematic is created, it is netlisted in the Design Capture of the Mentor Graphics (Simulation→Netlist). It generates a spice netlist which can be used for simulating in the LTSpice as shown below. Here I have attached the genhdl file that shows all the components of this solar panel and how they are connected in the schematic.

```
* Project BK1B235_Sun_Sensor
* Mentor Graphics Wirelist Created with Version 6.4.002
* File created Thu Oct 27 15:01:54 2016
* Inifile   :
* ConfigFile:  C:\MentorGraphics\7.9.4EE\SDD_HOME\standard\vspice.cfg
* Options   :  -__ -.spi -h -$ -7 -kC:\MentorGraphics\7.9.4EE\SDD_HOME\standard\vspice.cfg bk1b235_sun_sensor
* Levels    :
*
X1I453 N1N407 N1N408 N1N409 N1N410 AGND N1N411 N1N412 SUN_SENSOR CPC
R1I440 SUN_SENSOR AGND {HC( 22Kohms , 1000.000000M /100)} TC=100.000000U
* Dictionary 0
*Warning : No ground node (Label a net GND)

.include "..\..\genhdl\BK1B235_Sun_Sensor\BK1B235_Sun_Sensor_sources.spi"
.include "..\..\sym\CPC.mod"
```

4.20 1B133 Temperature Sensor:

Temperature sensor is the sensor that can sense the temperature and give the output in the form of voltage. BK1B133A measures the temperature within the range from -30˚C to 70˚C .Between these temperature ranges, the resistance value is varied between 2.2kΩ ~100kΩ and accordingly we will get the specified range of Output voltage(0 to 2.5V) by utilizing 3V of reference regulator.

Due to negative temperature coefficient, temperature and output voltage are inversely proportional to each other. Lower the temperature is, the higher the value of voltage equal to 2.5V (within the dynamics of the A / D converter) and the increase of this value tends to decrease as temperature, more or less linearly. Tolerance level of Temperature sensors are almost 1% that corresponds to high accuracy. Its schematic diagram is shown below in figure 4.63.

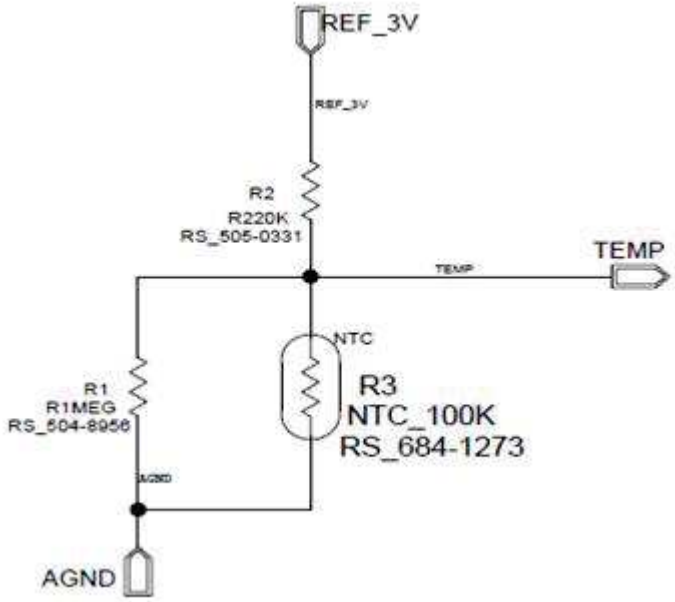


Fig 4.63: Schematic diagram of Bk1B133A_Temperature_Sensor

Output voltage is calculated by below formula:

$$TEMP = 3V * (R2//R3)/(R2//R3+R1)$$

Where R3=R25.exp (β25 (1/T-1/T25)), T25 =298.15K (Temperature at 25 degree centigrade), R25=100kΩ (resistance of sensor at 25 degree centigrade), β = 4100K.

4.20.1 Description:

This is the signal conditioning of a non-linear temperature sensor for an AraMiS project. It mostly converts temperature on a transducer (at point T ()) to and output voltage between pin TEMP () and analog ground AGND (). Temperature shall be in range T_MIN to T_MAX. Temperature shall be in a range which depends on the specific implementation of Bk1B133_Temperature_Sensor, while output voltage is in the range 0 to OUTPUT_RANGE. It requires a 3V reference voltage between REF_3V () and AGND (). The sensitivity and the offset in each Bk1B133_Temperature_Sensor are calculated that have a linearization of the characteristic in the range between T_MIN and T_MAX. Output voltage is a non linear function of temperature at point T (); this is plotted (for each implementation) in a referenced plot.

4.20.2 Testing of BK1B133A Temperature Sensor

Testing results of Bk1B133A_Temperature_Sensor are given below.

Serial #	Parameter	Expected Value	Current Result	Verification	Pass/Fail	Test bench
1	Output Voltage (V)	2.5	2.33	-40:TEMP=2.33V **70**:TEMP=0.215V	Fail	Test#1
2	Tolerance (%)	1	0.33	Output Range:(1.862-1.848/2) T=0.007/1.855=0.00377=0.377%	Fail	Test#2
3	Output Impedance(Zo)	220Kohm	230Kohm	V(ref_3v)/I(R1i109)=220mohm)	Fail	Test#6

Pin REF_3V ():

Serial #	Parameter	Expected Value	Current Result	Pass/Fail	Test bench
1	Input Voltage	3	3	Pass	Test#1

Pin AGND ():

Serial #	Parameter	Expected Value	Current Result	Pass/Fail	Test bench
1	Ground Voltage	0	0	Pass	Test#1

Pin TEMP ():

Serial #	Parameter	Expected Value	Current Result	Pass/Fail	Test bench
1	Maximum Output Voltage	2.5	2.33	Fail	Test#1

- ### Test Bench # 1(BK1B133A)

This test is used to measure the output of temperature sensor with respect to input. Here the dc voltage is given as an input where NTC100K will sense it the temperature range from -30 to 70 degree centigrade and we calculated the output voltage across it. Output voltage of the sensor is linearly proportional to temperature. Here we gave the dc voltage as an input and we calculated the voltage across the output terminal. Below, I have attached the sim_adms file that represents how to test the output of temperature sensor in LT-Spice.

```
.step TEMP -40 70 10
.include "..\..\genhdl\Bk1B133A_Temperature_Sensor_V1\Bk1B133A_Temperature_Sensor_V1.spi"
.option tnom=27
*.option dcmode=all gmin=1e-12 nodeset=1
*.option trmode=fast
.option method=trap

VVREF REF_3V 0 DC 3
VAGND AGND 0 DC 0


******end of additional commands*******
.end
```

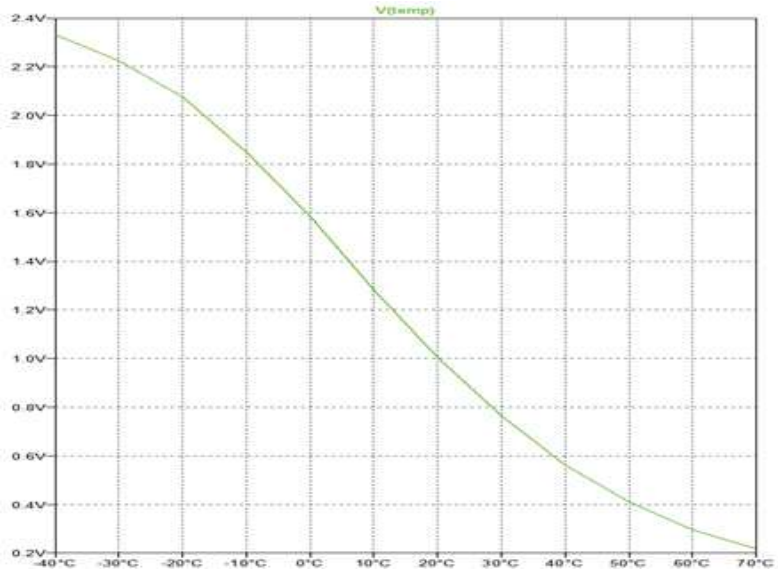


Figure 4.64: Output Voltage of Bk1B133A_Temperature_Sensor

- ## Test Bench # 2(BK1B133A)

In this test we applied Montecarlo approach in order to evaluate the error introduced by the manufacturing tolerances of the resistors in the main circuit. For this, I zoom in the V (temp) plot and observed the range of output value in which we select only the lines which are nearer to each other and then apply the standard deviation formula in order to approximate the tolerance. Below,I have attached the sim_adms generated picture with the help of step command in LT-Spice.

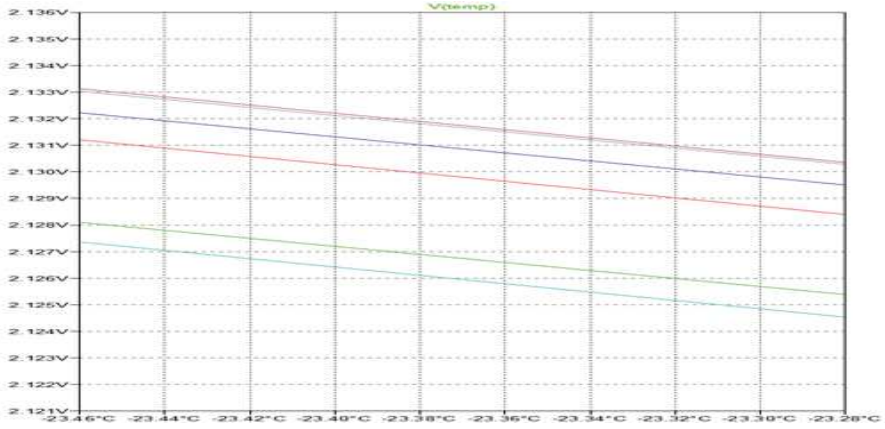


Figure 4.65: Tolerance of Bk1B133A_Temperature_Sensor

From the above graph, the output voltage range is from 1.848V to 1.862V. Its tolerance is calculated as given below.

Tolerance = (1.862-1.848)/2 = 0.007

Tolerance = 0.007/1.855=0.00377=0.377%

- ## Test Bench # 6(BK1B133A)

This test is used to measure the output impedance of temperature sensor. Below, I have attached the sim_adms file that represent how to test the impedance of this sensor in LT-Spice.

```
.step TEMP -40 70 10
.include "..\..\genhdl\Bk1B133A_Temperature_Sensor_V1\Bk1B133A_Temperature_Sensor_V1.spi"
VVREF REF_3V 0 DC 3
VAGND AGND 0 DC 0
*******end of additional commands********
.end
```

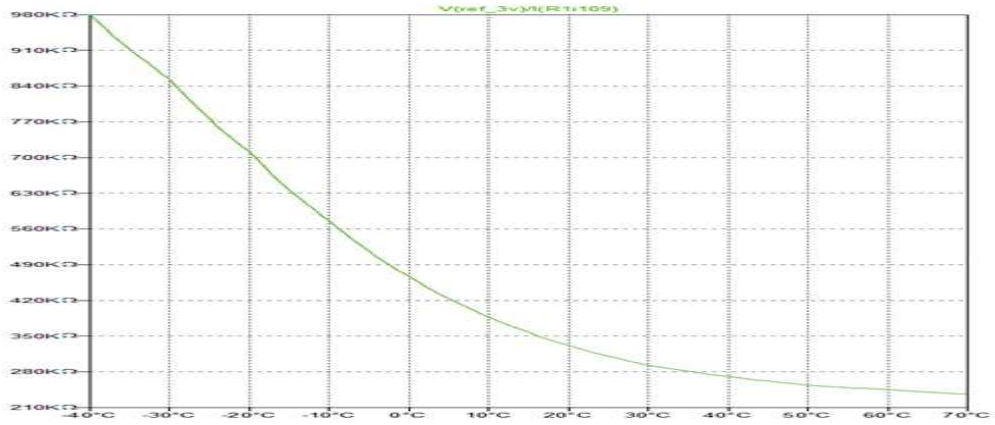


Figure 4.66: Output Impedance of Bk1B133A_Temperature_Sensor

Here the output impedance is calculated as given below

V (ref_3V)/I (R1I109) =230K ohm

4.20.3 Spice Netlist of BK1B133A_Temperature_Sensor:

Once the schematic is created, it is netlisted in the Design Capture of the Mentor Graphics (Simulation→Netlist). It generates a spice netlist which can be used for simulating in the LTSpice as shown below. Here I have attached the genhdl file that shows all the components of this solar panel and how they are connected in the schematic.

```
* Project Bk1B133A_Temperature_Sensor_V1
* Mentor Graphics Wirelist Created with Version 6.4.002
* File created Mon May 23 16:37:11 2016
* IniFile   :
* ConfigFile:  C:\MentorGraphics\7.9.4EE\SDD_HOME\standard\wspice.cfg
* Options   :  -__ -.spi -h -$ -7 -kC:\MentorGraphics\7.9.4EE\SDD_HOME\standard\wspice.cfg bk1b133a_temperature_sensor_v1
* Levels    :
*
R1I129 TEMP AGND {MC( 1MEGohms , 1000.000000M /100)} TC=100.000000U
R1I109 REF_3V TEMP {MC( 220Kohms , 1000.000000M /100)} TC=100.000000U
X1I91 TEMP AGND NTC100K
* Dictionary 0
*Warning : No ground node (Label a net GND)

*.include "..\..\genhdl\Bk1B133A_Temperature_Sensor_V1\Bk1B133A_Temperature_Sensor_V1_sources.spi"
.include "..\..\sym\NTC100K.mod"
```

4.21 1B8_CubePMT_1U_V1

1B8_CubePMT is the power management, attitude determination and control tile for AraMiSC1 satellite. 1B8_CubePMT is mounted on the four external faces of the AraMiS-C1 satellite. The class diagram of 1B8_CubePMT_1U_V1 is shown below in figure 4.67.

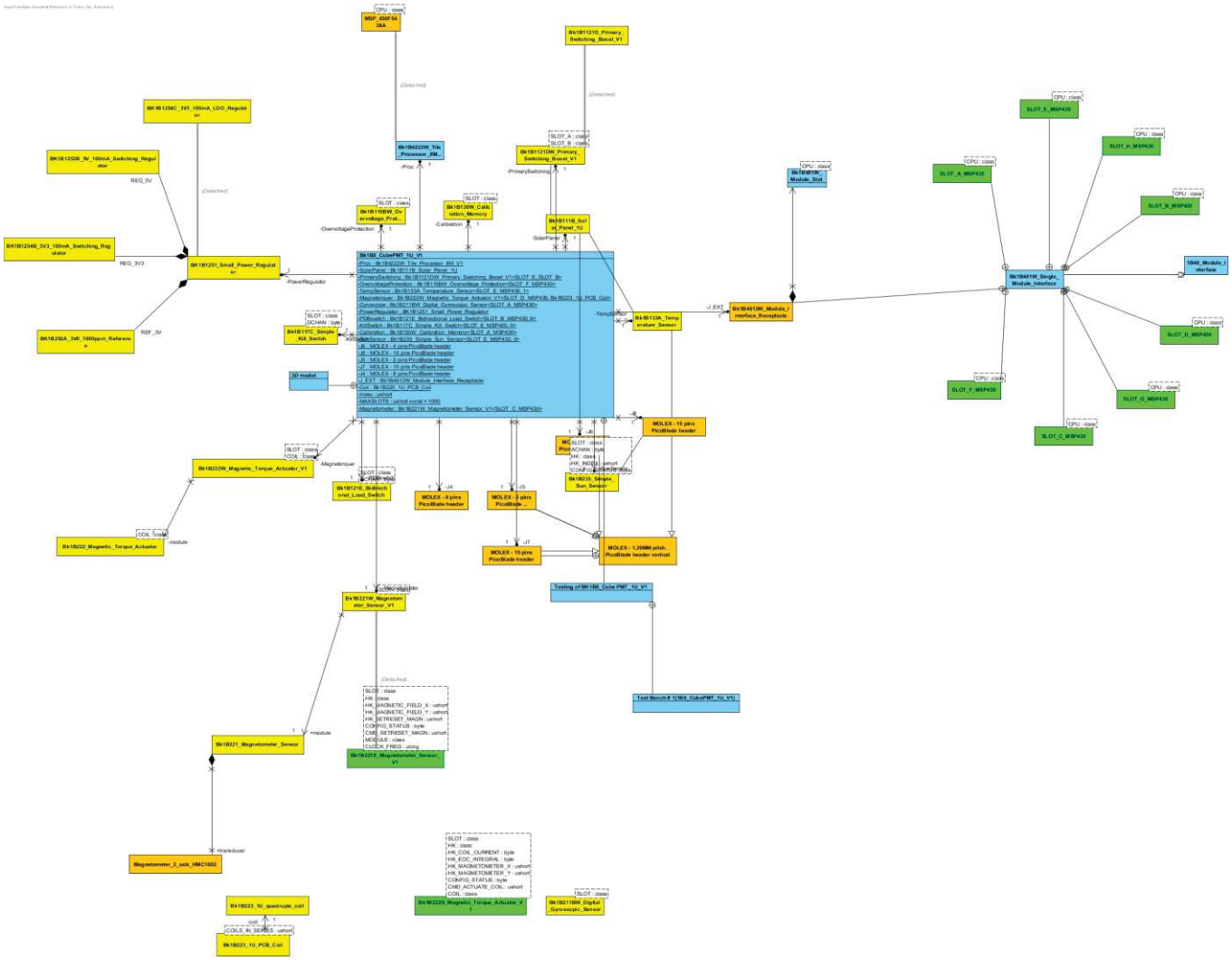


Figure 4.67: Class Diagram of Bk1B8CubePMT_1U_V1

- **Test Bench # 1(1B8_CubePMT_1U_V1)**

This test is called a global test that is used to measure the output across all the sub modules of Bk1B8_CubePMT_1U_V1 with respect to all the applied inputs. Here we gave the dc voltages as an input of different blocks and we calculated the voltage across their output terminals respectively. The same sim_adms files of different modules connected together in order to measure the system globally. Below, I have attached the sim_adms file that represents how to test the output of these sub modules in LT-Spice.

```
.tran 0.1U 600U 0
.include "..\..\genhdl\1B8_CubePMT_Subsystem\1B8_CubePMT_Subsystem.spi"
********************General*********************
VAGND AGND 0 DC 0
VGND GND 0 DC 0
**************Bidirectional_LoadSwitch*********
VEN1 B_D9_EN_PWM2 0 DC 1.3 PULSE (0 1.3 0.1U 100N)
*****************Solar Panel*****************
*VSOLAR_NEG SOLAR_NEG 0 DC 0
******************BOOST_Converter***********
VPWM 1B1121DV_PRIMAR4:A_D5_PWM 0 DC 3.3 PULSE (0 3.3 0.1U 100N 100N 0.5U 0.6U)
VDISABLE 1B1121DV_PRIMAR4:A_D4_CLK 0 DC 0
V3V3 1B1121DV_PRIMAR4:A_3V3 0 DC 3.7
**************Temperature_Sensor*********
*VE_REF1 E_REF 0 DC 3
**************Regulators******************
VB_D5_PWM B_D5_PWM 0 DC 3.3 PULSE (0 3.3 0.1U 100N)
VPDBINT POWER_REGULATOR2:PDB 0 DC 10 PULSE (0 10 0.1U 100N)
VVCC_5V POWER_REGULATOR2:VCC_5V 0 DC 5 PULSE (0 5 0.1U 100N)
VEN_5V POWER_REGULATOR2:B_D0_RX_SOMI 0 DC 5 PULSE (0 5 0.1U 100N)
VEN_3V3 POWER_REGULATOR2:B_D1_TX_SIMO 0 DC 3.3 PULSE (0 3.3 0.1U 100N)
VEN_REF POWER_REGULATOR2:B_D8_ID 0 DC 3.3 PULSE (0 3.3 0.1U 100N)
**************Magnetometer***********
*V1 1B221V_MAGNETOMETER5:M3V3 0 DC 3.3
*VREF_3V 1B221V_MAGNETOMETER5:REF 0 DC 3
*V5V 1B221V_MAGNETOMETER5:M5V 0 DC 5
*VEN2 1B221V_MAGNETOMETER5:D9_EN_PWM2 0 DC 5 PULSE (0 5 10U 100n 100N 100N 200N)
*VRESET1 1B221V_MAGNETOMETER5:D1_TX_SIMO 0 DC 3.3 PULSE (3.3 0 100U 100N 100N 10U 400U)
*VnotSET1 1B221V_MAGNETOMETER5:D0_RX_SOMI 0 DC 3.3 PULSE (3.3 0 102U 100N 100N 6U 400U)
*********************************Power Regulator*****************************************
R16                    POWER_REGULATOR2:1B1261C_OCTAL_I2:1B1261A_INTERNO8:A_REF    0 1neg
R17                    POWER_REGULATOR2:1B1261C_OCTAL_I2:1B1261A_INTERNO7:A_REF    0 1neg
R18                    POWER_REGULATOR2:1B1261C_OCTAL_I2:1B1261A_INTERNO6:A_REF    0 1neg
R19                    POWER_REGULATOR2:1B1261C_OCTAL_I2:1B1261A_INTERNO5:A_REF    0 1neg
R20                    POWER_REGULATOR2:1B1261C_OCTAL_I2:1B1261A_INTERNO4:A_REF    0 1neg
R21                    POWER_REGULATOR2:1B1261C_OCTAL_I2:1B1261A_INTERNO3:A_REF    0 1neg
R22                    POWER_REGULATOR2:1B1261C_OCTAL_I2:1B1261A_INTERNO2:A_REF    0 1neg
R23                    POWER_REGULATOR2:1B1261C_OCTAL_I2:1B1261A_INTERNO8:A_PDB    0 1neg
R24                    POWER_REGULATOR2:1B1261C_OCTAL_I2:1B1261A_INTERNO7:A_PDB    0 1neg
R25                    POWER_REGULATOR2:1B1261C_OCTAL_I2:1B1261A_INTERNO6:A_PDB    0 1neg
R26                    POWER_REGULATOR2:1B1261C_OCTAL_I2:1B1261A_INTERNO5:A_PDB    0 1neg
R27                    POWER_REGULATOR2:1B1261C_OCTAL_I2:1B1261A_INTERNO4:A_PDB    0 1neg
R28                    POWER_REGULATOR2:1B1261C_OCTAL_I2:1B1261A_INTERNO3:A_PDB    0 1neg
R29                    POWER_REGULATOR2:1B1261C_OCTAL_I2:1B1261A_INTERNO2:A_PDB    0 1neg
R30                    POWER_REGULATOR2:1B1261C_OCTAL_I2:1B1261A_INTERNO8:A_5V     0 1neg
R31                    POWER_REGULATOR2:1B1261C_OCTAL_I2:1B1261A_INTERNO7:A_5V     0 1neg
R32                    POWER_REGULATOR2:1B1261C_OCTAL_I2:1B1261A_INTERNO6:A_5V     0 1neg
R33                    POWER_REGULATOR2:1B1261C_OCTAL_I2:1B1261A_INTERNO5:A_5V     0 1neg
R34                    POWER_REGULATOR2:1B1261C_OCTAL_I2:1B1261A_INTERNO4:A_5V     0 1neg
R35                    POWER_REGULATOR2:1B1261C_OCTAL_I2:1B1261A_INTERNO3:A_5V     0 1neg
R36                    POWER_REGULATOR2:1B1261C_OCTAL_I2:1B1261A_INTERNO2:A_5V     0 1neg
R37                    POWER_REGULATOR2:1B1261C_OCTAL_I2:1B1261A_INTERNO8:A_3V3    0 1neg
R38                    POWER_REGULATOR2:1B1261C_OCTAL_I2:1B1261A_INTERNO7:A_3V3    0 1neg
R39                    POWER_REGULATOR2:1B1261C_OCTAL_I2:1B1261A_INTERNO6:A_3V3    0 1neg
R40                    POWER_REGULATOR2:1B1261C_OCTAL_I2:1B1261A_INTERNO5:A_3V3    0 1neg
R41                    POWER_REGULATOR2:1B1261C_OCTAL_I2:1B1261A_INTERNO4:A_3V3    0 1neg
R42                    POWER_REGULATOR2:1B1261C_OCTAL_I2:1B1261A_INTERNO3:A_3V3    0 1neg
R43                    POWER_REGULATOR2:1B1261C_OCTAL_I2:1B1261A_INTERNO2:A_3V3    0 1neg
```

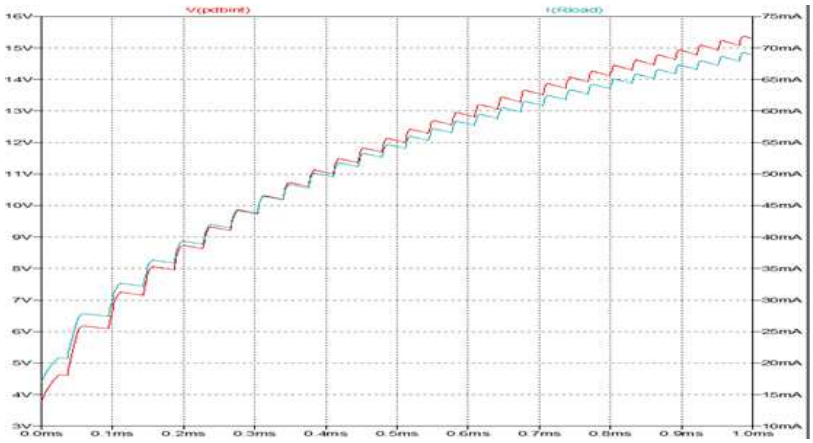


Figure 4.68: Output Voltage across boost module in Bk1B8_CubePMT_1U_V1

4.21.1 Spice Netlist of BK18_CubePMT_1U_V1:

Once the schematic is created, it is netlisted in the Design Capture of the Mentor Graphics (Simulation→Netlist). It generates a spice netlist which can be used for simulating in the LTSpice as shown below. Here I have attached the genhdl file that shows all the components of this power management tile.

```
* Project 1B8_CubePMT_Subsystem
* Mentor Graphics Wirelist Created with Version 6.4.002
* File created Wed Nov 02 11:37:21 2016
* ConfigFile:  C:\MentorGraphics\7.9.4EE\SDD_HOME\standard\wspice.cfg
* Options    :  -__ -.spi -h -$ -kC:\MentorGraphics\7.9.4EE\SDD_HOME\standard\wspice.cfg 1b8_cubepmt_subsystem
R1I1137 DGND AGND {MC( 20Mohms , 1000.000000M /100)} TC=200.000000U
XCMP131 DGND SOLAR_POS PDB_OUT DGND VM7608CT
X1I1244 DGND SOLAR_POS BK1B111B_Solar_Panel_CubeSat_V1
X1I1114 AGND E_D7_A1 E_REF Bk1B133A_Temperature_Sensor_V1
X1B1121DV_Primar4 DGND SOLAR_POS F_PDB B_PDB 1B1121DV_Primary_Switching_Boost_V1
XCMP148 TDO DGND TDI VCC_CPU TDO TCK TEST RST VM7612CT
X1B115BV_Overvol2 F_PDB 1B115BV_Overvoltage_Protection_V1
X1I1110 E_D6_A0 AGND BK1B235_Sun_Sensor
X1B117C_Simple_K1 A_3V3 KS E_D9_EN_PWM2 1B117C_Simple_Kill_Switch_V1
X1I1082 DGND A_PDB Bk1B130V_Calibration_Memory_V1
R1I1150 XSIG011306 DGND {MC( 100ohms , 1000.000000M /100)} TC=100.000000U
C1I1170 B_D5_PWM XSIG011306 {MC( 18.000000P , 5.000000 /100)} TC=10.000000U
R1I1160 F_PDB XSIG011306 {MC( 100ohms , 1000.000000M /100)} TC=100.000000U
R1I1179 M1N1189 XSIG011436 {MC( 100ohms , 1000.000000M /100)} TC=100.000000U
X1B2118V_Digital1 A_PDB 1B2118V_Digital_Gyroscopic_Sensor_V1
X1B223_1U_PCB_Co3 COIL1 COIL2 1B223_1U_PCB_Coil_V1
X1B222V_Magnetic5 COIL1 COIL2 D_PDB 1B222V_Magnetic_Torque_Actuator_V1
RXCMP224 COIL2 COIL2 0
*Warning: No value for RXCMP224. Defaulting to 0
RXCMP225 COIL1 COIL1 0
*Warning: No value for RXCMP225. Defaulting to 0
XPower_Regulator2 XSIG011306 B_PDB XSIG011436 H_PDB G_PDB F_PDB E_PDB D_PDB C_PDB A_PDB Power_Regulator
X1B4222_Tile_Process1 VCC_CPU TDO INTRA_D0 H_PDB G_PDB F_PDB E_PDB C_PDB D_PDB A_PDB B_PDB 1B4222_Tile_Processor_8N_V2
RXCMP226 C_D0_RX_SOMI C_D0_RX_SOMI 0
*Warning: No value for RXCMP226. Defaulting to 0
RXCMP242 C_D1_TX_SIMO C_D1_TX_SIMO 0
*Warning: No value for RXCMP242. Defaulting to 0
RXCMP243 C_D9_EN_PWM2 C_D9_EN_PWM2 0
*Warning: No value for RXCMP243. Defaulting to 0
RXCMP244 D_D9_EN_PWM2 D_D9_EN_PWM2 0
*Warning: No value for RXCMP244. Defaulting to 0
RXCMP245 D_D0_RX_SOMI D_D0_RX_SOMI 0
*Warning: No value for RXCMP245. Defaulting to 0
RXCMP246 D_D1_TX_SIMO D_D1_TX_SIMO 0
*Warning: No value for RXCMP246. Defaulting to 0
RXCMP247 D_D4_CLK D_D4_CLK 0
*Warning: No value for RXCMP247. Defaulting to 0
RXCMP248 D_D5_PWM D_D5_PWM 0
*Warning: No value for RXCMP248. Defaulting to 0
RXCMP249 F_D5_PWM F_D5_PWM 0
*Warning: No value for RXCMP249. Defaulting to 0
RXCMP250 F_D4_CLK F_D4_CLK 0
*Warning: No value for RXCMP250. Defaulting to 0
RXCMP251 B_D9_EN_PWM2 B_D9_EN_PWM2 0
*Warning: No value for RXCMP251. Defaulting to 0
RXCMP253 A_REF A_REF 0
*Warning: No value for RXCMP253. Defaulting to 0
RXCMP254 F_D6_A0 F_D6_A0 0
*Warning: No value for RXCMP254. Defaulting to 0
RXCMP255 XSIG011519 DGND 1uohms RES1
XCMP256 XSIG011519 Connector_1PIN
XCMP257 XSIG011519 Connector_1PIN
XCMP259 XSIG011521 Connector_1PIN
XCMP260 XSIG011522 Connector_1PIN
```

```
XCMP261 XSIG011523 Connector_1PIN
XCMP262 XSIG011524 Connector_1PIN
XCMP263 XSIG011525 Connector_1PIN
XCMP264 XSIG011526 Connector_1PIN
RXCMP265 F_D7_A1 F_D7_A1 0
*Warning: No value for RXCMP265. Defaulting to 0
RXCMP266 B_D6_A0 B_D6_A0 0
*Warning: No value for RXCMP266. Defaulting to 0
RXCMP267 B_D7_A1 B_D7_A1 0
*Warning: No value for RXCMP267. Defaulting to 0
RXCMP268 C_D6_A0 C_D6_A0 0
*Warning: No value for RXCMP268. Defaulting to 0
RXCMP269 C_D7_A1 C_D7_A1 0
*Warning: No value for RXCMP269. Defaulting to 0
RXCMP270 D_D6_A0 D_D6_A0 0
*Warning: No value for RXCMP270. Defaulting to 0
RXCMP271 E_D6_A0 E_D6_A0 0
*Warning: No value for RXCMP271. Defaulting to 0
RXCMP272 E_D7_A1 E_D7_A1 0
*Warning: No value for RXCMP272. Defaulting to 0
RXCMP273 A_D8_ID A_D8_ID 0
*Warning: No value for RXCMP273. Defaulting to 0
XCMP274 A_3V3 DGND A_D3_SDA_SIMO A_D2_SCL_SOMI KS WM7609CT WM7609CT
*Warning: No Model For XCMP274.Defaulting to WM7609CT
X1B221W_Magnetometer5 C_PDB 1B221W_Magnetometer_V1
XCMP275 A_3V3 DGND G_D0_RX_SOMI G_D1_TX_SIMO KS WM7609CT WM7609CT
*Warning: No Model For XCMP275.Defaulting to WM7609CT
R1I1224 A_3V3 A_D3_SDA_SIMO {MC( 10Kohms , 1000.000000M /100)} TC=100.000000U
R1I1234 A_3V3 A_D2_SCL_SOMI {MC( 10Kohms , 1000.000000M /100)} TC=100.000000U
X1I1100 PDB_OUT F_PDB B_D9_EN_PWM2 DGND BK1B121E_Bidirectional_Load_Switch_V1
* Dictionary 0
*Warning : No ground node (Label a net GND)
*Definition For Project BK1B121E_Bidirectional_Load_Switch_V1
.SUBCKT BK1B121E_Bidirectional_Load_Switch_V1 B A EN DGND
XM1 XSIG010014 XSIG010002 A IRLML6402
DD1 XSIG010023 XSIG010019 1N4148
RR2 XSIG010005 XSIG010019 {MC( 200Kohms , 1000.000000M /100)} TC=100.000000U
XQ1 XSIG010005 EN DGND NTA7002N
XM2 XSIG010014 XSIG010023 B IRLML6402
RR4 XSIG010023 B {MC( 100Kohms , 1000.000000M /100)} TC=100.000000U
RR1 XSIG010020 XSIG010005 {MC( 200Kohms , 1000.000000M /100)} TC=100.000000U
DD5 XSIG010021 XSIG010014 CZRU52C7V5
DD2 XSIG010021 XSIG010023 1N4148
RR3 A XSIG010002 {MC( 100Kohms , 1000.000000M /100)} TC=100.000000U
DD3 XSIG010021 XSIG010002 1N4148
DD4 XSIG010002 XSIG010020 1N4148
* CROSS-REFERENCE 0
.ENDS
*Definition For Project 1B221W_Magnetometer_V1
.SUBCKT 1B221W_Magnetometer_V1 MODULE
X1I346 M5V D9_EN_PWM2 D6_A0 D7_A1 D1_TX_SIMO D0_RX_SOMI REF M3V3 M0 M1 BK1B221_Magnetometer_V1
.ENDS
*Definition For Project BK1B221_Magnetometer_V1
.SUBCKT BK1B221_Magnetometer_V1 M5V EN_MAGN MAGN_Y MAGN_X RESET notSET REF_3V M3V3 AGND DGND
XU3 XSIG010024 XSIG010031 XSIG010030 XSIG010025 AGND M1MA78 XSIG010046 M5V_int ad8226
CC3 DGND XSIG010008 {MC( 10.000000U , 10.000000 /100)} TC=10.000000U
RR3 XSIG010008 M3V3 {MC( 200ohms , 100.000000M /100)} TC=100.000000U
XLMA128 EN_MAGN M5V_int REF_AV1 AGND LMA128_AV1
RR1 XSIG010030 XSIG010031 {MC( 3.3Kohms , 1000.000000M /100)} TC=200.000000U
RR2 XSIG010029 XSIG010028 {MC( 3.3Kohms , 1000.000000M /100)} TC=200.000000U
XU2 REF_AV1 REF_AV1 AGND AGND AGND AGND AGND XSIG010022 XSIG010023 XSIG010020 XSIG010021 XSIG010017 DGND XSIG010018 DGND XSIG010025 XSIG010024 XSIG010027
+XSIG010026 HMC1002
X1I2166 M5V_int M5V EN_MAGN DGND BK1B121C_Load_Switch_V3
DD1 MAGN_X M3V3 B320A
RR6 M1M1981 REF_3V {MC( 1Kohms , 1000.000000M /100)} TC=100.000000U
RR7 XSIG010006 MAGN_X {MC( 1Kohms , 1000.000000M /100)} TC=100.000000U
CC1 XSIG010013 XSIG010017 {MC( 470.000000M , 20.000000 /100)} TC=10.000000U
DD2 MAGN_Y M3V3 B320A
RR8 AGND M1M1981 {MC( 1Kohms , 1000.000000M /100)} TC=100.000000U
CC2 XSIG010013 XSIG010018 {MC( 470.000000M , 20.000000 /100)} TC=10.000000U
RR4 notSET XSIG010003 {MC( 33ohms , 1000.000000M /100)} TC=100.000000U
RR5 RESET XSIG010005 {MC( 33ohms , 1000.000000M /100)} TC=100.000000U
XM2 XSIG010013 XSIG010005 DGND irF7311
X0 XSIG010013 XSIG010005 DGND irF7311
XU4 XSIG010026 XSIG010028 XSIG010029 XSIG010027 AGND M1MA78 XSIG010044 M5V_int ad8226
XM1 XSIG010013 XSIG010003 XSIG010008 IRF7324
X1 XSIG010013 XSIG010003 XSIG010008 IRF7324
XU5 M1M1981 M1MA78 M5V_int AGND M1MA78 op1177
CC7 M5V_int AGND {MC( 100.000000M , 10.000000 /100)} TC=10.000000U
RR10 XSIG010044 MAGN_Y {MC( 1Kohms , 1000.000000M /100)} TC=100.000000U
.ENDS
*Definition For Project 1BA222_Tile_Processor_8M_V2
.SUBCKT 1BA222_Tile_Processor_8M_V2 VCC_CPU MODULE_JTAG MODULE_INTRA MODULE_H MODULE_G MODULE_F MODULE_E MODULE_C MODULE_D MODULE_A MODULE_B
X1I1A20 A_D3_SDA_SIMO B_D3_SDA_SIMO 1B1261Z_Short_Circuit
X1I1A21 A_D2_SCL_SOMI B_D2_SCL_SOMI 1B1261Z_Short_Circuit
X1I1A22 C_D3_SDA_SIMO D_D3_SDA_SIMO 1B1261Z_Short_Circuit
X1I1A23 C_D2_SCL_SOMI D_D2_SCL_SOMI 1B1261Z_Short_Circuit
X1I1A24 E_D3_SDA_SIMO F_D3_SDA_SIMO 1B1261Z_Short_Circuit
X1I1A25 E_D2_SCL_SOMI F_D2_SCL_SOMI 1B1261Z_Short_Circuit
X1I1A26 G_D3_SDA_SIMO H_D3_SDA_SIMO 1B1261Z_Short_Circuit
X1I1A27 G_D2_SCL_SOMI H_D2_SCL_SOMI 1B1261Z_Short_Circuit
C1I1A98 RST 0 {MC( 10.000000M , 10.000000 /100)} TC=10.000000U
C1I1535 0 VCC_CPU {MC( 100.000000M , 10.000000 /100)} TC=10.000000U
C1I1526 0 VCC_CPU {MC( 10.000000U , 10.000000 /100)} TC=10.000000U
XCMP18 C_D6_A0 C_D7_A1 D_D6_A0 E_D6_A0 F_D7_A1 G_D6_A0 G_D7_A1 H_D6_A0
+E_D7_A1 F_D6_A0 VCC_CPU AGND XSIG010096 XSIG010097 0 VCC_CPU A_D9_ID
+A_D9_EN_PWM2 B_D8_ID G_D9_EN_PWM2 C_D8_ID C_D9_EN_PWM2 D_D8_ID D_D9_EN_PWM2
+E_D8_ID F_D9_EN_PWM2 F_D8_ID E_D9_EN_PWM2 G_D8_ID 0 VCC_CPU B_D9_EN_PWM2
+H_D8_ID H_D9_EN_PWM2 A_D4_CLK A_D3_SDA_SIMO A_D2_SCL_SOMI B_D4_CLK
+A_D1_TX_SIMO A_D0_RX_SOMI C_D4_CLK C_D3_SDA_SIMO A_D5_PWM B_D5_PWM C_D5_PWM
+D_D5_PWM E_D5_PWM F_D5_PWM XSIG010199 0 VCC_CPU G_D5_PWM D_D7_A1
+C_D2_SCL_SOMI D_D4_CLK C_D1_TX_SIMO C_D0_RX_SOMI INTRA_D2 H_D0_RX_SOMI
+B_D1_TX_SIMO D_D0_RX_SOMI D_D1_TX_SIMO H_D5_PWM F_D1_TX_SIMO H_D0_RX_SOMI
+H_D1_TX_SIMO VCC_CPU 0 XSIG010445 XSIG010447 TEST TDO TDI TMS TCK RST A_D6_A0
+ A_D7_A1 B_D6_A0 B_D7_A1 F_D0_RX_SOMI E_D4_CLK E_D3_SDA_SIMO E_D2_SCL_SOMI
+F_D4_CLK E_D1_TX_SIMO E_D0_RX_SOMI INTRA_D3 H_D7_A1 XSIG010451 XSIG010452
```

```
+XSIG010453 G_D4_CLK G_D3_SDA_SIMO G_D2_SCL_SOMI H_D4_CLK G_D1_TX_SIMO
+G_D0_RX_SOMI INTRA_D0 INTRA_D1 MSP430F5438 MSP430F5438
*Warning: No Model For XCMP18.Defaulting to MSP430F5438
R1I1556 VCC_CPU RST {MC( 47Kohms , 1000.000000M /100)} TC=100.000000U
RXCMP18 XSIG010451 XSIG010451 0
*Warning: No value for RXCMP18. Defaulting to 0
RXCMP19 XSIG010452 XSIG010452 0
*Warning: No value for RXCMP19. Defaulting to 0
RXCMP20 XSIG010453 XSIG010453 0
*Warning: No value for RXCMP20. Defaulting to 0
X1I1482 XSIG010445 XSIG010447 X_4MEG
CXCMP22 0 XSIG010445 18pF CAP1
CXCMP23 0 XSIG010447 18pF CAP1
CXCMP27 0 XSIG010097 0 CAP1
*Warning: No value for CXCMP27. Defaulting to 0
C1I1441 XSIG010096 0 {MC( 12.000000P , 20.000000 /100)} TC=10.000000U
X1I1470 XSIG010096 XSIG010097 QZ532768
.ENDS
*Definition For Project Power_Regulator
.SUBCKT Power_Regulator EN_CPU MODULE_B VCC_CPU MODULE_H MODULE_G MODULE_F MODULE_E MODULE_D MODULE_C MODULE_A
X1B1251_Small_Po1 PDB B_D0_ID EN_CPU B_D1_TX_SIMO B_D0_RX_SOMI VCC_CPU VCC_3V3 VCC_5V REF_3V 1B1251_Small_Power_Regulator_V1
X1B1261C_Octal_I2 REF_3V VCC_3V3 VCC_5V PDB B_PDB A_PDB H_PDB G_PDB F_PDB E_PDB D_PDB C_PDB 1B1261C_Octal_InterModule_Power_Distribution
.ENDS
*Definition For Project 1B1261C_Octal_InterModule_Power_Distribution
.SUBCKT 1B1261C_Octal_InterModule_Power_Distribution REF_3V VCC_3V3 VCC_5V PDB MODULE_B MODULE_A MODULE_H MODULE_G MODULE_F MODULE_E MODULE_D MODULE_C
X1B1261A_InterMo2 B_PDB A_PDB 1B1261A_InterModule_Power_Distribution
X1B1261A_InterMo3 C_PDB A_PDB 1B1261A_InterModule_Power_Distribution
X1B1261A_InterMo4 D_PDB A_PDB 1B1261A_InterModule_Power_Distribution
X1B1261A_InterMo5 E_PDB A_PDB 1B1261A_InterModule_Power_Distribution
X1B1261A_InterMo6 F_PDB A_PDB 1B1261A_InterModule_Power_Distribution
X1B1261A_InterMo7 G_PDB A_PDB 1B1261A_InterModule_Power_Distribution
X1B1261A_InterMo8 H_PDB A_PDB 1B1261A_InterModule_Power_Distribution
* CROSS-REFERENCE 0
.ENDS
*Definition For Project 1B1261A_InterModule_Power_Distribution
.SUBCKT 1B1261A_InterModule_Power_Distribution MODULE_B MODULE_A
X1B1261Z_Short_C2 B_PDB A_PDB 1B1261Z_Short_Circuit
X1B1261Z_Short_C3 B_5V A_5V 1B1261Z_Short_Circuit
X1B1261Z_Short_C4 B_3V3 A_3V3 1B1261Z_Short_Circuit
X1B1261Z_Short_C5 B_REF A_REF 1B1261Z_Short_Circuit
* CROSS-REFERENCE 0
.ENDS
*Definition For Project 1B1261Z_Short_Circuit
.SUBCKT 1B1261Z_Short_Circuit 0 0
* CROSS-REFERENCE 0
.ENDS
*Definition For Project 1B1251_Small_Power_Regulator_V1
.SUBCKT 1B1251_Small_Power_Regulator_V1 PDBINT EN_REF EN_CPU EN_3V3 EN_5V
+VCC_CPU VCC_3V3 VCC_5V REF_3V
X1I348 PDBINT EN_3V3 VCC_3V3 N0 Bk1B1254B_3V3_100mA_Regulator_V1
* Pin  is not connected
X1I351 N1 PDBINT EN_CPU VCC_CPU Bk1B1254C_3V3_100mA_LDO_Regulator_V1
* Pin  is not connected
X1I354 N2 VCC_5V EN_REF REF_3V Bk1B1252A_3V01000ppmRef_V1
* Pin  is not connected
X1I345 N3 EN_5V VCC_5V PDBINT Bk1B1253B_5V_100mA_Regulator_V1
* Pin  is not connected
* CROSS-REFERENCE 0
.ENDS
*Definition For Project Bk1B1253B_5V_100mA_Regulator_V1
.SUBCKT Bk1B1253B_5V_100mA_Regulator_V1 DGND EN_5V VCC_5V VAL
LL1 VCC_5V SW {MC( 100.000000U , 20.000000 /100)} RSER=1.820000
RTP1 VCC_5V VCC_5V 0
*Warning: No value for RTP1. Defaulting to 0
XU1 SW VAL N1N186 N1N91 EN_5V VCC_5V N1N185 DGND LTC3631-5
CC1 VCC_5V DGND {MC( 10.000000U , 10.000000 /100)} TC=10.000000U
CC2 VAL DGND {MC( 2.200000U , 10.000000 /100)} TC=10.000000U
.ENDS
*Definition For Project Bk1B1252A_3V01000ppmRef_V1
.SUBCKT Bk1B1252A_3V01000ppmRef_V1 DGND VAL EN_REF REF_3V
XU1 EN_REF VAL REF_3V DGND LM4128_3V
CC1 REF_3V DGND {MC( 100.000000N , 10.000000 /100)} TC=10.000000U
RTP1 REF_3V REF_3V 0
*Warning: No value for RTP1. Defaulting to 0
CC2 VAL DGND {MC( 4.700000U , 10.000000 /100)} TC=10.000000U
.ENDS
*Definition For Project Bk1B1254C_3V3_100mA_LDO_Regulator_V1
.SUBCKT Bk1B1254C_3V3_100mA_LDO_Regulator_V1 DGND VAL EN_3V3 VCC_3V3
XU1 VAL DGND EN_3V3 XSIG010007 VCC_3V3 lt1761-3.3
RTP1 VCC_3V3 VCC_3V3 0
*Warning: No value for RTP1. Defaulting to 0
CC1 VCC_3V3 DGND {MC( 10.000000U , 10.000000 /100)} TC=10.000000U
CC2 VCC_3V3 XSIG010007 {MC( 10.000000N , 25.000000 /100)} TC=10.000000U
CC3 VAL DGND {MC( 1000.000000N , 15.000000 /100)} TC=10.000000U
.ENDS
*Definition For Project Bk1B1254B_3V3_100mA_Regulator_V1
.SUBCKT Bk1B1254B_3V3_100mA_Regulator_V1 VAL EN_3V3 VCC_3V3 DGND
LL1 VCC_3V3 XSIG010010 {MC( 100.000000U , 20.000000 /100)} RSER=1.820000
RXCMP2 VCC_3V3 VCC_3V3 0
*Warning: No value for RXCMP2. Defaulting to 0
CC1 VAL DGND {MC( 2.200000U , 10.000000 /100)} TC=10.000000U
CC2 VCC_3V3 DGND {MC( 0 , 20.000000 /100)} TC=10.000000U
*Warning: No value for CC2. Defaulting to 0
XU1 XSIG010010 VAL XSIG010005 XSIG010012 EN_3V3 VCC_3V3 XSIG010004 DGND LTC3631-3.3
.ENDS
*Definition For Project 1B222W_Magnetic_Torque_Actuator_V1
.SUBCKT 1B222W_Magnetic_Torque_Actuator_V1 COIL1 COIL2 MODULE
X1B222_Magnetic_1 N5V PDB REF D0_RX_SOMI D5_PWM D4_CLK D6_A0 D9_EN_PWM2 D1_TX_SIMO COIL1 COIL2 1B222_Magnetic_Torque_Actuator_V1
* CROSS-REFERENCE 1
* 5V=N5V
.ENDS
*Definition For Project 1B222_Magnetic_Torque_Actuator_V1
.SUBCKT 1B222_Magnetic_Torque_Actuator_V1 N5V PDBINT REF_3V NOT_ENABLE PHASE NOT_BRAKE SENSE EN_COIL MODE COIL1 COIL2
C1I403 PDBINT_EN 0 {MC( 10.000000U , 80.000000 /100)} TC=10.000000U
R1I393 REF_3V XSIG010001 {MC( 18Kohms , 1000.000000M /100)} TC=100.000000U
C1I374 XSIG010004 0 {MC( 470.000000P , 10.000000 /100)} TC=10.000000U
X1I416 N0 PDBINT_EN EN_COIL PDBINT Bk1B121D_Load_Switch_High_Voltage_V1
* Pin  is not connected
R1I383 XSIG010001 0 {MC( 10Kohms , 1000.000000M /100)} TC=100.000000U
X1I337 N5V_int N5V EN_COIL N1 BK1B121C_Load_Switch_V3
* Pin  is not connected
C1I355 N5V_int 0 {MC( 100.000000N , 10.000000 /100)} TC=10.000000U
R1I364 XSIG010004 0 {MC( 38Kohms , 100.000000M /100)} TC=15.000000U
X1I343 XSIG010018 0 XSIG010049 XSIG010050 RES_4WIRE R={MC(200Mohms,1000.000000M/100)} TC=200.000000U
XCMP9 NOT_BRAKE XSIG010001 XSIG010004 PHASE NOT_ENABLE COIL2 MODE XSIG010018 COIL1 PDBINT_EN 0 N5V_int A3953 A3953
*Warning: No Model For XCMP9.Defaulting to A3953
X1I334 AGND SENSE N5V_int XSIG010049 XSIG010050 BK1B137A_Differential_Voltage_Sensor_V1
.ENDS
```

```
.SUBCKT 8K1B137A_Differential_Voltage_Sensor_V1 VREF VOUT N5V VINPOS VINNEG
RR1 XSIG010027 AGND {MC( 7.5Kohms , 100.000000M /100)} TC=100.000000U
RR2 VREF XSIG010027 {MC( 10.5Kohms , 100.000000M /100)} TC=25.000000U
RR3 XSIG010016 XSIG010023 {MC( 1MEGohms , 100.000000M /100)} TC=25.000000U
CC1 N5V AGND {MC( 100.000000N , 10.000000 /100)} TC=10.000000U
RR4 XSIG010015 VOUT {MC( 1MEGohms , 100.000000M /100)} TC=25.000000U
XU1 XSIG010027 XSIG010023 N5V AGND XSIG010023 LM6142
RR5 VINPOS XSIG010016 {MC( 100Kohms , 100.000000M /100)} TC=100.000000U
RR6 VINNEG XSIG010015 {MC( 100Kohms , 100.000000M /100)} TC=100.000000U
X0 XSIG010016 XSIG010015 N5V AGND VOUT LM6142
.ENDS
*Definition For Project 8K1B121C_Load_Switch_V3
.SUBCKT 8K1B121C_Load_Switch_V3 OUT IN EN DGND
RR1 N_1N67 N_1N71 {MC( 15ohms , 1000.000000M /100)} TC=100.000000U
RR2 IN N_1N67 {MC( 100Kohms , 1000.000000M /100)} TC=100.000000U
XM2 OUT N_1N67 IN IRLML6402
XM1 N_1N71 EN DGND NTA7002N
.ENDS
*Definition For Project 8k1B121D_Load_Switch_High_Voltage_V1
.SUBCKT 8k1B121D_Load_Switch_High_Voltage_V1 DGND OUT EN IN
XM1 OUT GATE IN IRLML6402
RR1 GATE XSIG010005 {MC( 200Kohms , 1000.000000M /100)} TC=100.000000U
RR2 IN GATE {MC( 100Kohms , 1000.000000M /100)} TC=100.000000U
XQ1 XSIG010005 EN DGND NTA7002N
* CROSS-REFERENCE 0
.ENDS
*Definition For Project 1B223_1U_PCB_Coil_V1
.SUBCKT 1B223_1U_PCB_Coil_V1 COIL1 COIL2
R1I367 COIL1 XSIG010004 {MC( 20Mohms , 1000.000000M /100)} TC=200.000000U
R1I357 COIL1 XSIG010006 {MC( 20Mohms , 1000.000000M /100)} TC=200.000000U
R1I347 COIL1 XSIG010015 {MC( 20Mohms , 1000.000000M /100)} TC=200.000000U
N1I343 COIL1 XSIG010016 XSIG010004 XSIG010008 XSIG010006 XSIG010009 XSIG010015 XSIG010014
R1I377 XSIG010016 XSIG010004 {MC( 20Mohms , 1000.000000M /100)} TC=200.000000U
R1I407 COIL2 XSIG010014 {MC( 20Mohms , 1000.000000M /100)} TC=200.000000U
R1I417 COIL2 XSIG010009 {MC( 20Mohms , 1000.000000M /100)} TC=200.000000U
R1I427 XSIG010016 COIL2 {MC( 20Mohms , 1000.000000M /100)} TC=200.000000U
R1I437 XSIG010009 XSIG010015 {MC( 20Mohms , 1000.000000M /100)} TC=200.000000U
R1I447 XSIG010008 XSIG010006 {MC( 20Mohms , 1000.000000M /100)} TC=200.000000U
R1I457 COIL2 XSIG010008 {MC( 20Mohms , 1000.000000M /100)} TC=200.000000U
* CROSS-REFERENCE 0
.ENDS
*Definition For Project 1B2118V_Digital_Gyroscopic_Sensor_V1
.SUBCKT 1B211BV_Digital_Gyroscopic_Sensor_V1 MODULE
X1B211B_Digital_1 N3V3 D9_EN_PWM2 N5V D4_CLK D1_TX_SIMO D5_PWM D0_RX_SOMI 1B211B_Digital_Gyroscopic_Sensor_V1
.ENDS
*Definition For Project 1B211B_Digital_Gyroscopic_Sensor_V1
.SUBCKT 1B211B_Digital_Gyroscopic_Sensor_V1 N3V3 ENABLE N5V SCLK DIN nCS DOUT
XCMP3 DIN SCLK DOUT XSIG010006 XSIG010007 XSIG010018 XSIG010008 XSIG010014 0 XSIG010012 XSIG010011 XSIG010010 OUT nCS ADIS16080 ADIS16080
X1B121C_Load_Swi1 N5V ENABLE OUT
X1B121C_Load_Swi2 N3V3 ENABLE XSIG010018
RXCMP4 DIN DIN 0
*Warning: No value for RXCMP4. Defaulting to 0
RXCMP5 SCLK SCLK 0
*Warning: No value for RXCMP5. Defaulting to 0
RXCMP6 DOUT DOUT 0
*Warning: No value for RXCMP6. Defaulting to 0
RXCMP7 nCS nCS 0
*Warning: No value for RXCMP7. Defaulting to 0
.ENDS
```

```
*Definition For Project 8K1B130V_Calibration_Memory_V1
.SUBCKT 8K1B130V_Calibration_Memory_V1 DGND MODULE
XCMP1 D8_ID DGND DS2502 REUSE CELL REF DES
RTP1 D8_ID D8_ID 0
*Warning: No value for RTP1. Defaulting to 0
.ENDS
*Definition For Project 1B117C_Simple_Kill_Switch_V1
.SUBCKT 1B117C_Simple_Kill_Switch_V1 N3V3 KS DEPLOYED
R1I315 N3V3 KS {MC( 10Kohms , 1000.000000M /100)} TC=100.000000U
.ENDS
*Definition For Project 8K1B235_Sun_Sensor
.SUBCKT 8K1B235_Sun_Sensor SUN_SENSOR AGND
XU1 N1NA07 N1NA08 N1NA09 N1NA10 AGND N1NA11 N1NA12 SUN_SENSOR CPC
RR1 SUN_SENSOR AGND {MC( 22Kohms , 1000.000000M /100)} TC=100.000000U
* CROSS-REFERENCE 0
.ENDS
*Definition For Project 1B115BV_Overvoltage_Protection_V1
.SUBCKT 1B115BV_Overvoltage_Protection_V1 MODULE
X1B115B_Overvolt1 PDB 1B115B_Overvoltage_Protection_V1
* CROSS-REFERENCE 0
.ENDS
*Definition For Project 1B115B_Overvoltage_Protection_V1
.SUBCKT 1B115B_Overvoltage_Protection_V1 PDB
D1I344 XSIG010001 PDB SMAZ10
D1I352 0 XSIG010001 SMAZ10
.ENDS
*Definition For Project 1B1121DV_Primary_Switching_Boost_V1
.SUBCKT 1B1121DV_Primary_Switching_Boost_V1 SOLAR_NEG SOLAR_POS MODULE_A MODULE_B
X1I372 A_D4_CLK A_D5_PWM A_3V3 SOLAR_NEG B_D6_A0 B_D7_A1 A_PDB A_D6_A0 A_D7_A1 SOLAR_POS N0 N1 8K1B1121D_Primary_Switching_Boost_V1
* Pin  is not connected
* Pin  is not connected
.ENDS
*Definition For Project 8K1B1121D_Primary_Switching_Boost_V1
.SUBCKT 8K1B1121D_Primary_Switching_Boost_V1 Disable PWM_IN N3V3 SOLAR_NEG
*V_out I_out PDBINT V_Solar I_Solar SOLAR_POS AGND DGND
QQ1 SOLAR_POS XSIG010012 XSIG010011 MMBT3904LT1G
X111869 DGND DC_OUT N3V3 PWM_IN 8K1B1122_PWM_DC_Converter_V1
XNMOSH_X XSIG010026 Disable DGND MMBF0201
RR1 SOLAR_POS XSIG010026 {MC( 2.2Kohms , 1000.000000M /100)} TC=100.000000U
CC3 SOLAR_POS DGND {MC( 47.000000N , 10.000000 /100)} TC=10.000000U
CC1 I_OUT DGND {MC( 10.000000U , 10.000000 /100)} TC=0.000000F
XU1 XSIG010026 DC_OUT SOLAR_POS DGND XSIG010012 XSIG010036 DGND DGND
+MAX975HS
X111078 PDBINT CS_VOUT I_IN AGND 8k1B132D_Current_Sensor_V1
X8k1B132A_Current_Sensor AGND I_OUT I_Solar SOLAR_POS
+8k1B132A_Current_Sensor_V1
RR2 XSIG010026 DGND {MC( 5.6Kohms , 1000.000000M /100)} TC=100.000000U
RXCMP51 I_OUT I_OUT 0
RXCMP52 I_IN I_IN 0
X11959 Vout PDBINT AGND 8k1B131C_Voltage_Sensor_V1
X8k1B131B_Voltage_Sensor V_Solar SOLAR_POS AGND 8k1B131B_Voltage_Sensor_V1
XNMOSH_PW_X XSIG010063 XSIG010011 DGND SI7112ADN
CC2 I_IN DGND {MC( 10.000000U , 10.000000 /100)} TC=0.000000F
RR3 XSIG010026 XSIG010012 {MC( 26.7Kohms , 1000.000000M /100)}
+TC=100.000000U
LL1 XSIG010063 I_OUT {MC( 47.000000U , 20.000000 /100)} RSER=71.900000M
DD1 XSIG010063 I_IN B320A
QQ3 DGND XSIG010012 XSIG010011 MMBT3906
.ENDS
```

```
*Definition For Project Bk1B131B_Voltage_Sensor_V1
.SUBCKT Bk1B131B_Voltage_Sensor_V1 Vout Vin AGND
CC1 Vout AGND {MC( 0.01uF , 10.000000 /100)} TC=10.000000U
RR1 Vin Vout {MC( 390Kohms , 1000.000000M /100)} TC=100.000000U
RR2 Vout AGND {MC( 133Kohms , 1000.000000M /100)} TC=100.000000U
* CROSS-REFERENCE 0
.ENDS
*Definition For Project Bk1B131C_Voltage_Sensor_V1
.SUBCKT Bk1B131C_Voltage_Sensor_V1 Vout Vin AGND
CC1 Vout AGND {MC( 10.000000N , 10.000000 /100)} TC=10.000000U
RR2 Vout AGND {MC( 120Kohms , 1000.000000M /100)} TC=100.000000U
RR1 Vin Vout {MC( 820Kohms , 1000.000000M /100)} TC=100.000000U
.ENDS
*Definition For Project Bk1B132A_Current_Sensor_V1
.SUBCKT Bk1B132A_Current_Sensor_V1 AGND I_OUT CS_VOUT I_IN
CC1 CS_VOUT AGND {MC( 0.01uF , 10.000000 /100)} TC=10.000000U
RR1 CS_VOUT AGND {MC( 100Kohms , 1000.000000M /100)} TC=100.000000U
XR2 I_IN I_OUT XSIG010025 XSIG010024 RES_4WIRE R={MC(200mohms,1000.000000M/100)} TC=200.000000U
XU1 XSIG010025 XSIG010024 XSIG010025 AGND CS_VOUT INA138
.ENDS
*Definition For Project Bk1B132D_Current_Sensor_V1
.SUBCKT Bk1B132D_Current_Sensor_V1 I_OUT CS_VOUT I_IN AGND
CC1 CS_VOUT AGND {MC( 0.01uF , 10.000000 /100)} TC=10.000000U
XR1 I_IN I_OUT XSIG010025 XSIG010024 RES_4wire R={MC(820Mohms,1000.000000M/100)} TC=250.000000U
RR2 CS_VOUT AGND {MC( 100Kohms , 1000.000000M /100)} TC=100.000000U
XU1 XSIG010025 XSIG010024 XSIG010025 AGND CS_VOUT INA138
.ENDS
*Definition For Project Bk1B1122_PWM_DC_Converter_V1
.SUBCKT Bk1B1122_PWM_DC_Converter_V1 DGND DC_OUT VCC_3V3 PWM_IN
RR1 VCC_3V3 DC_OUT {MC( 27Kohms , 1000.000000M /100)} TC=100.000000U
RR2 DC_OUT DGND {MC( 100Kohms , 1000.000000M /100)} TC=100.000000U
CC1 VCC_3V3 DGND {MC( 100.000000N , 10.000000 /100)} TC=10.000000U
CC2 N_1N18 N_1N14 {MC( 10.000000N , 10.000000 /100)} TC=10.000000U
RR3 N_1N18 PWM_IN {MC( 1Kohms , 1000.000000M /100)} TC=100.000000U
DD1 N_1N14 VCC_3V3 BAT54
CC3 DC_OUT DGND {MC( 470.000000N , 20.000000 /100)} TC=10.000000U
RR4 N_1N14 DC_OUT {MC( 10Kohms , 1000.000000M /100)} TC=100.000000U
DD2 DGND N_1N14 BAT54
.ENDS
*Definition For Project Bk1B133A_Temperature_Sensor_V1
.SUBCKT Bk1B133A_Temperature_Sensor_V1 AGND TEMP REF_3V
RR1 TEMP AGND {MC( 1MEGohms , 1000.000000M /100)} TC=100.000000U
RR2 REF_3V TEMP {MC( 220Kohms , 1000.000000M /100)} TC=100.000000U
XR3 TEMP AGND NTC100K
.ENDS
*Definition For Project BK1B111B_Solar_Panel_CubeSat_V1
.SUBCKT BK1B111B_Solar_Panel_CubeSat_V1 SOLAR_NEG SOLAR_POS
DD1 SOLAR_NEG POS DFLS220L
DD2 POS SOLAR_POS DFLS220L
XD3 SOLAR_POS POS CESI-TJ-CTJH-70x40
XD4 POS SOLAR_NEG CESI-TJ-CTJH-70x40
.ENDS
*Globals
.global AGND
.global 0
.include "..\..\sym\1N4148.mod"
.include "..\..\sym\8320A.mod"
.include "..\..\sym\BAT54.mod"
.include "..\..\sym\CAP1.mod"
.include "..\..\sym\CESI-TJ-CTJH-70x40.mod"
.include "..\..\sym\CPC.mod"
.include "..\..\sym\CZRU52C7V5.mod"
.include "..\..\sym\Connector_1PIN.mod"
.include "..\..\sym\DFLS220L.mod"
.include "..\..\sym\HMC1002.mod"
.include "..\..\sym\INA138.mod"
.include "..\..\sym\IRF7324.mod"
.include "..\..\sym\IRLML6402.mod"
.include "..\..\sym\LM4128_3V.mod"
.include "..\..\sym\LM4128_4V1.mod"
.include "..\..\sym\LM6142.mod"
.include "..\..\sym\MAX975HS.mod"
.include "..\..\sym\MMBF0201.mod"
.include "..\..\sym\MMBT3904LT1G.mod"
.include "..\..\sym\MMBT3906.mod"
.include "..\..\sym\NTA7002N.mod"
.include "..\..\sym\NTC100K.mod"
.include "..\..\sym\Q2S32768.mod"
.include "..\..\sym\RES1.mod"
.include "..\..\sym\RES_4WIRE.mod"
.include "..\..\sym\SI7112ADN.mod"
.include "..\..\sym\SMAZ10.mod"
.include "..\..\sym\WM7608CT.mod"
.include "..\..\sym\WM7612CT.mod"
.include "..\..\sym\X_4MEG.mod"
.include "..\..\sym\ad8226.mod"
.include "..\..\sym\irf7311.mod"
.include "..\..\sym\lt1761-3.3.mod"
.include "..\..\sym\op1177.mod"
```

Chapter 5
Electric Power Supply Management

5.1 Introduction:

1B8_CubePMT is one tile of Aramis-C1 that contains electric power supply and attitude and determination control system. Electric power supply helps to control the power generation while the ADCS controls the positioning and spinning of satellite across the earth. Electric power supply contain solar panel, boost converter, housekeeping sensors, load switches, linear and switching regulators while ADCS contain sun sensor, magnetometer, gyroscope, magnetic torque actuator and magnetorquer coil. 1B8_CubePMT has a main microcontroller MSP430F5438 that help to manage the power and data processing and maintain its operation.

In this chapter we will discuss the design, implementation and operation of all the subsystems of AraMiS-C1 EPS in detail. The aim of electric power supply (EPS) unit is to generate, distribute and convert power to different voltage levels. Nanosatellite dimensions and space environment constraints limit the design of an ideal EPS system. To accommodate such a large number of subsystems in a small space, require to reduce the dimension of all the subsystems. The main goal in the EPS design is to achieve higher efficiency and to reduce the size of all components used. Therefore COTS components were selected for EPS on the basis of power loss analysis and small dimensions. The desired functionalities guide the EPS design. The designed EPS use to produce sufficient energy to supply all the subsystems of the AraMiS-C1 satellite. The EPS provide several power outputs (3V, 3.3V, 5V etc.) with stabilized voltages. It also contains different sensors mounted at different point on the EPS.

5.2 EPS Subsystems for 1B8_CubePMT_3U:

EPS at tile level contains the following subsystems which we will simulate it later on,

- BK1B132 Current Sensors.
    - BK1B132A Input Current Sensor.
    - BK1B132D Output Current Sensor.
- BK1B131 Voltage Sensors.
    - BK1B131B Input Voltage Sensor.
    - BK1B131C Output Voltage Sensor.
- BK1B1122 PWM DC Converter.
- BK1B1121D Boost Converter.
- BK1B125 Linear Regulators.
    - BK1B1252A 3V Reference Regulator.
    - BK1B1254C 3.3V Linear Regulator.
- BK1B125 Switching Regulators.
    - BK1B1253B 5V Switching Regulator.
    - BK1B1254B 3.3V Switching Regulator.
- BK1B121 Load Switches.

- BK1B121C Low Voltage Load Switch.
- BK1B121D High Voltage Load Switch.
- BK1B121E Bidirectional Load Switch.

- BK1B133 Temperature Sensor.
  - BK1B133A Temperature Sensor.
  - BK1B133B Temperature Sensor.
- BK1B111 Solar Panel.
  - BK1B111A Solar Panel.
  - BK1B111B Solar Panel.
- BK1B235 Sun Sensor.
- BK1B115B Over Voltage Protection.

In 1B8_CubePMT_3U, it seems to be strange that Boost converter (step up to 14V) is still attached along with six solar cells that also give the same 13.2V output which is also equal to 14V PDB. It's because of the safety purpose that during mission in the space ,if one out of six solar cells damage then in this time boost converter helps to maintain the voltage level equal to 14V PDB. Maximum power point tracker (MPPT) operates solar cells at maximum power point. Over voltage protection circuit keeps the PDB voltage within the operation limits. Switching and linear regulators step down the PDB voltage to different voltage levels required for all the subsystem components. Load switches supply and cutoff power from the subsystems through enable signal from the tile processor. Housekeeping sensors such as voltage, current and temperature sensors are employed at different points of the EPS in order to monitor the operation and inform the tile processor in case of abnormalities. Block diagram of the 3U 1B8_CubePMT EPS subsystem is shown in figure 5.1.

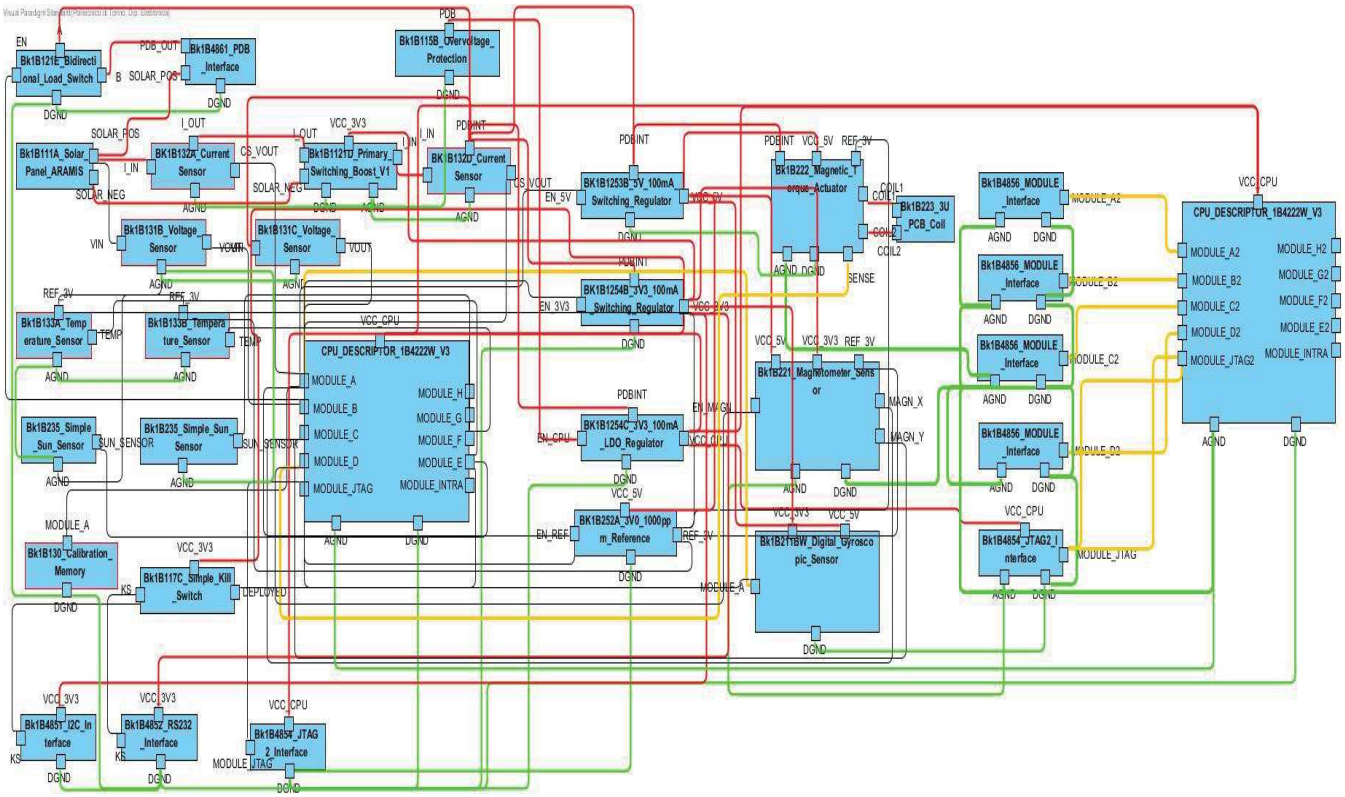


Figure 5.1: EPS Block diagram at tile level.

5.2.1 BK1B132A & BK1B132D Current Sensors:

In 1B8_CubePMT, there are two kinds of Current Sensors. One Sensor (BK1B132A) is to limit the current to maximum amount equal to 625mA while the other sensor (BK1B132D) is to limit the current to maximum amount equal to 152mA. The output of the Current Sensor CS_VOUT is connected to the ADC pin of the tile processor in order to instantly monitor the flow of current. Here we choose BK1B132A current sensor for finding the output and sampling frequency. Its formulas are given below:

$$Vo = \frac{(I_{sense} \times R_{sense} \times R_{out})}{5K\Omega}$$

$$f_{sampling} = 2 \times \frac{1}{2 \times \pi \times C_{OUT} \times R_{OUT}}$$

Where R_{SENSE} and R_{OUT} have the value when maximum range of input current flow through R_{SENSE}, Vo become equal to output range. Similarly, C_{OUT} and R_{OUT} sets the sampling frequency of the current sensor, as from below formula: The schematic diagrams of BK1B132A current sensor is given blow in figure 5.2.

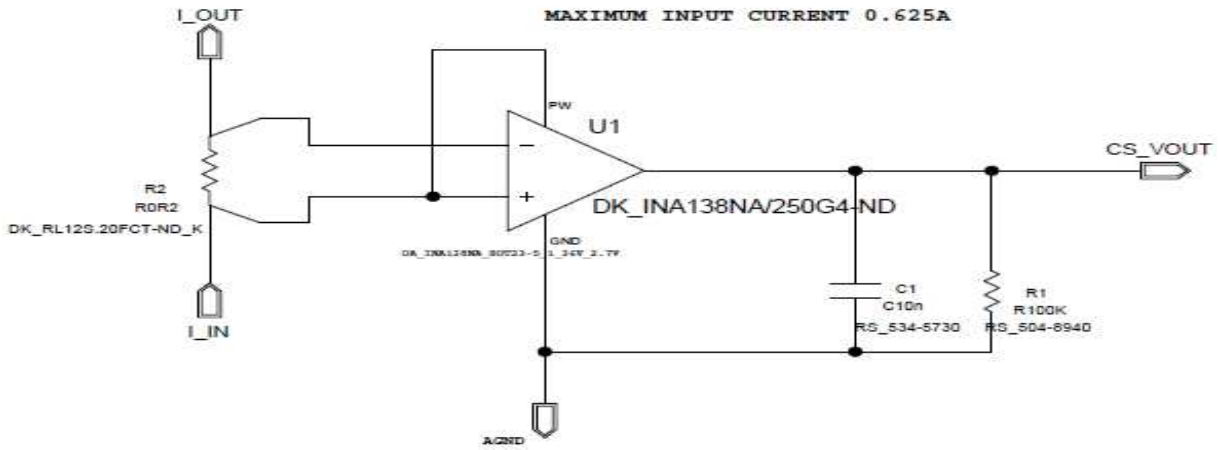


Figure 5.2: Schematic of BK1B132A Current Sensor

Here, the output voltage and sampling frequency obtain from this current sensor are calculated as

$$Vo = \frac{(I_{sense} \times R_{sense} \times R_{out})}{5K\Omega} = (0.625*0.2*100k)/5k=2.5V$$

$$f_{sampling} = 2 \times \frac{1}{2 \times \pi \times C_{OUT} \times R_{OUT}} = 2*\ 1\ /\ (2*3.14*10n*100k) = 318Hz$$

5.2.2 BK1B131B & BK1B131C Voltage Sensors:

In 1B8_CubePMT_3U, there are two kinds of Voltage Sensor. One Sensor (BK1B131B) is to limit the voltage to maximum amount equal to 10V while other sensor (BK1B131C) is to limit the voltage to maximum amount equal to 20V. The output of the Voltage Sensor Vout is connected to the ADC pin of the tile processor in order to instantly monitor the potential. Here we choose BK1B131B voltage sensor for finding the output. Its formula is given below:

$$V_{out} = V_{in} \times \frac{R_{17}}{R_{17} + R_{29}}$$

The schematic diagram of BK1B131B voltage sensors is given blow in figure5.3

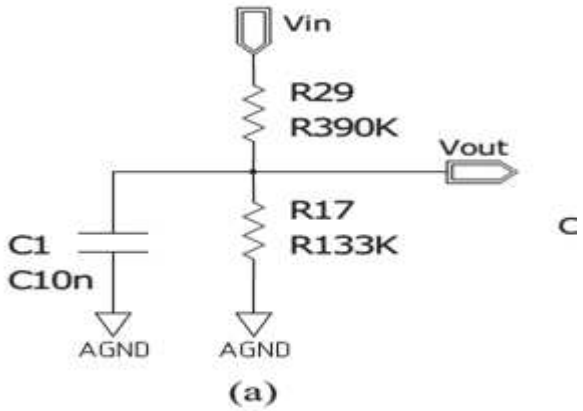


Figure 5.3: Schematic diagram of BK1B131B voltage sensor

When the Voltage Sensor is connected before the terminal of MSP430 processor, it looks like Low pass filter. The most important factor in filter designing is sampling. The sampling frequency ($f_{sampling}$) is set by the value of C1 and R_{eq} (R17//R29) of BK1B131B. In order to avoid aliasing, below criteria should be satisfied;

$$f_{sampling} \geq 2 \times \frac{1}{2\pi C_1 R_{eq}} \qquad \text{Where } R_{eq}=\frac{R_{17} \times R_{29}}{R_{17}+R_{29}}, C_1 = 10nF$$

From the above equations, it is calculated the sampling frequency should be almost 321Hz for BK1B131B for avoiding aliasing problem.

The schematic of voltage sensor with microprocessor is shown is below Figure 5.4.

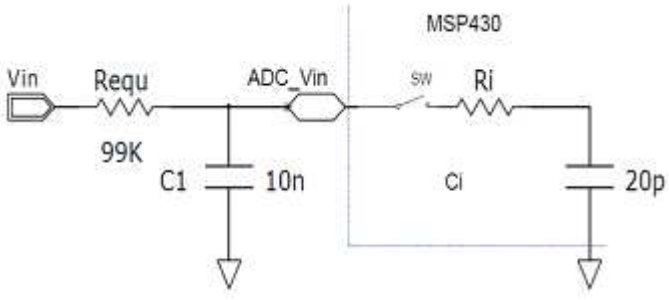


Figure 5.4: Equivalent circuit of 10V voltage sensor attached on MSP430 ADC pin.

The internal circuit diagram of Analog to Digital converter of MSP430 contains an internal resistor (R_i) and a capacitor (C_i). The value of resistor R_i=10Ω is normally neglected because of its small value while C_i=20pF is attached in parallel to C1=10nF that cause an error. The error is that it can change the point of sampling frequency and provide aliasing problem in the system. So, changing the value of capacitor C1 is the only solution to avoid the problem of Aliasing.

When the switch is open, capacitor C_i has no charge. The charge distribution across C1 and C_i is calculated as given below.

$$Q_i = C_i V_i = C_i \times 0 = 0$$

$$Q_1 = C1V_1 = Q_t$$

When switch is close, C_i charge instantly. In transient state, both the capacitors have same potential that are shown below.

$$Q_i = C_i V_x = \Delta Q$$

$$Q_1 = Q_t - \Delta Q = C_1 V_x$$

Where V_x is the voltage across C1 when switch is closed that are shown below.

$$V_x = V_1 \frac{C1}{C1 + C_i}$$

The relative error introduce by C_i is calculated by dividing the difference between (V1-Vx) with V_1 that is given below.

$$e_{V_1} = \frac{\Delta V}{V_1} = \frac{V_1 - V_x}{V_1} = \frac{C_i}{C1 + C_i}$$

5.2.3 BK1B1122 PWM DC Converter:

For the inverting input voltage of a comparator U7 that is part of Boost Converter, a PWM-DC-converter block is used in order to give a constant voltage at the inverting terminal of U7. These converters usually give the constant output voltage that plays a major role in Boost Converter. In our case, it gives 2.83 V at the output terminal (DC_OUT) for the input voltage is 3.6 V. The Schematics of PWM DC converter is shown in below Figure 5.5.

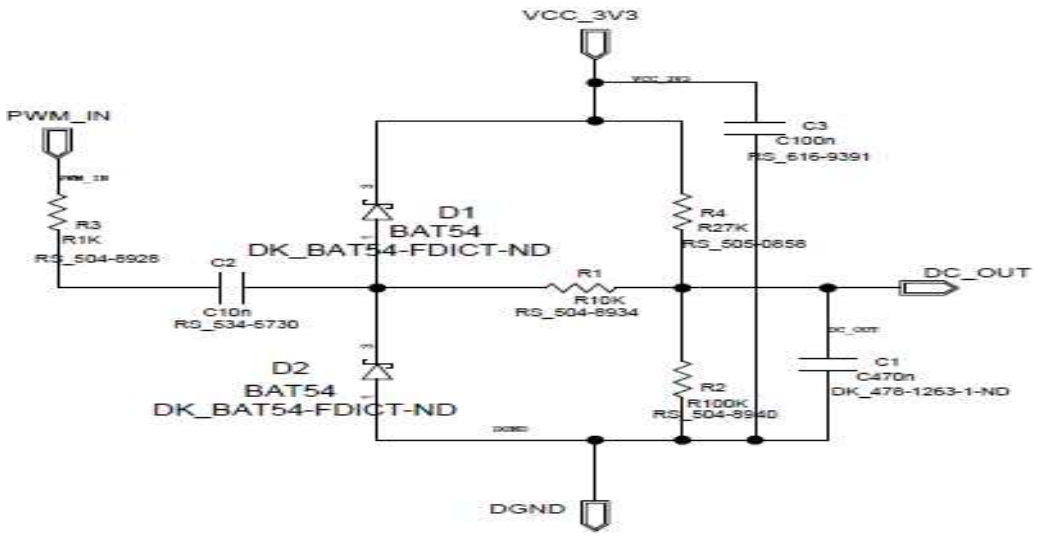


Figure 5.5: Schematic of PWM DC Converter.

5.2.4 BK1B1121D Boost Converter:

Boost converter consists of a MOSFET, an inductor, a schottky diode (preferred because of low forward voltage drop) and two ceramic capacitors (preferred because of low ESR). Two series connected solar cells generate a constant voltage of 4.2V. Boost converter step up this generated 4.2V to PDB voltage level that is 14V.

Capacitor C32 plays an important role that is controlled by resistive divider network (R30 & R32).This divider divides the input voltage (SOLAR_POS) and gives it to the non-inverting terminal of comparator U7. For the inverting terminal, PWM DC converter gives a constant voltage that is almost 2.9V. When the capacitor C32 charge up to 4.165V, it means positive terminal of U7 becomes greater than the inverting terminal. The outputs of U7 switch high and short the MOSFET (Q9). At this time, capacitor C32 draws the voltage from 4.16 up to 3.835V. When the capacitor reach at 3.835V,positive terminal of the U7 become less than negative terminal that correspond to switch low at the output of U7.At this time, capacitor C32 again start charging up to 4.165 and the process repeats again. Maximum and Minimum voltage of U7 at two different levels VH = 4.165V and VL =3.83V is called hysteresis window that is only possible with the help of resistive divider network (R30 & R32). This hysteresis window prevents the circuit from oscillation due to the presence of noise. It also helps in making the time interval for charge and discharge of capacitor C32. The designed values of resistor divider network are R31=26.7KΩ, R30=2.2kΩ. The schematic of the Boost Converter is shown in below Figure 5.6.

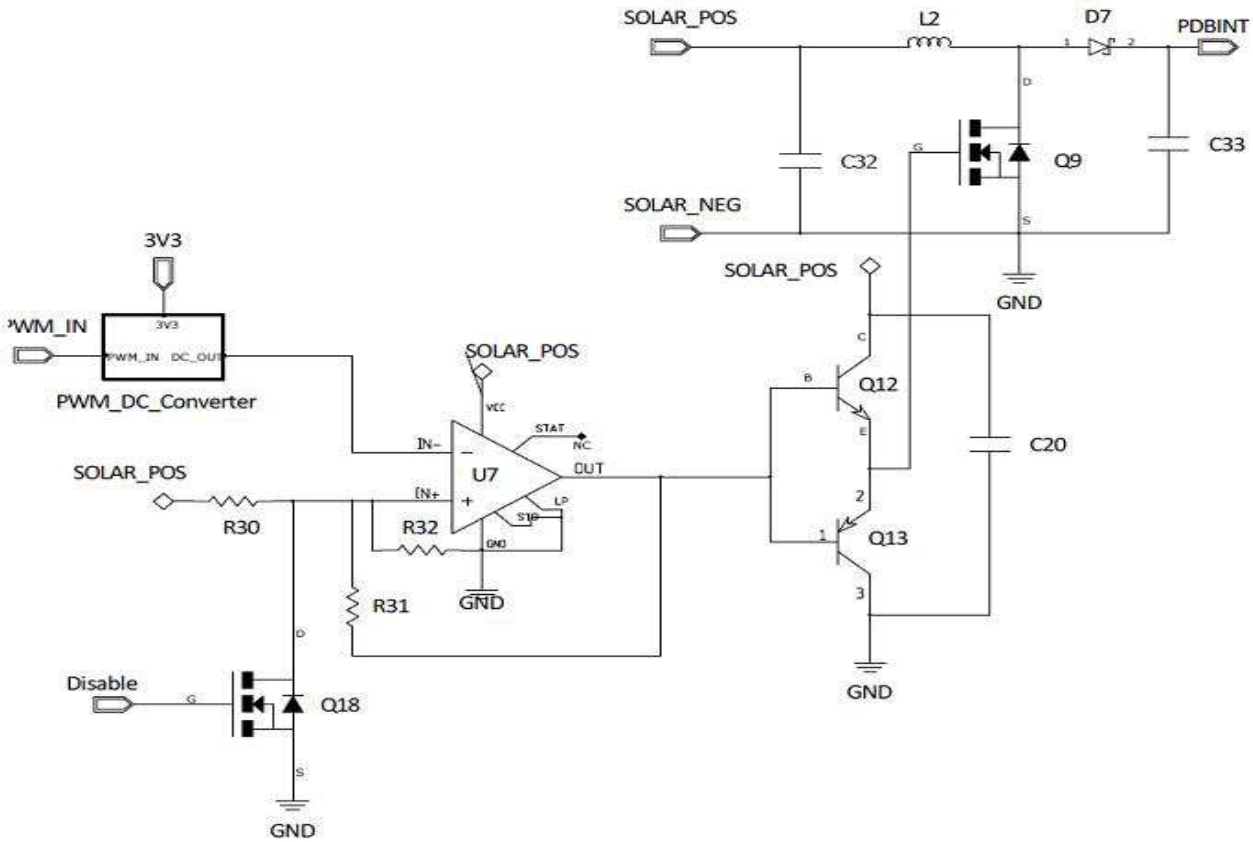


Figure 5.6: Schematic of Boost Converter.

5.2.5 BK1B1252A 3V Reference Regulator:

This regulator gives 3V reference voltage. It works only when it is enabled from the Tile processor. It actually steps down from 5V input to 3V output in order to give this reference voltage for the magnetometer and magnetic torque actuator. Their input and Output voltage difference are very less that's corresponds to low power consumption. The schematic of the 3V reference Regulator is shown in below Figure 5.7.

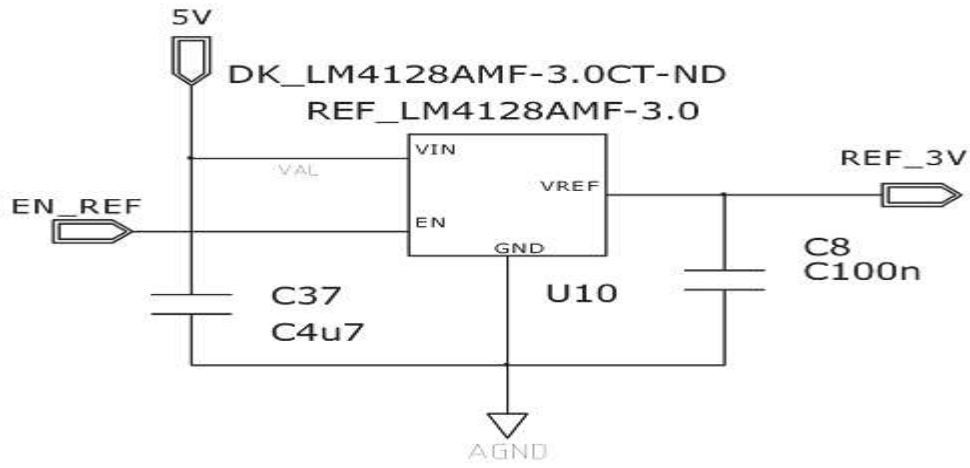


Figure 5.7: Schematic of the 3V reference voltage supply.

5.2.6 BK1B1254C 3.3V Linear Regulator (Low dropout Voltage):

This regulator converts PDB voltage (~14V input) to 3.3V at the output. The purpose of this LDO is to continuously give power to Tile processor whenever the processor want and also make it independent from other sub circuit. It is enabled from the Tile processor. The voltage difference between input and output of this linear regulator is very high that's why it has high power consumption. The schematic of the 3.3V LDO is shown in below Figure 5.8.

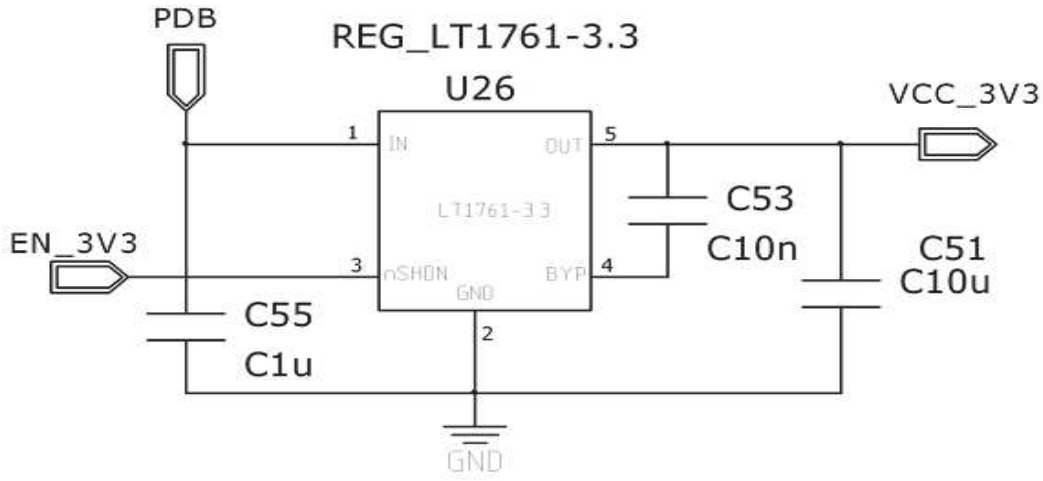


Figure 5.8: Schematic of the 3.3V voltage supply.

5.2.7 BK1B1254B 3.3V Switching Regulator:

This regulator converts PDB voltage (~14V input) to a 3.3V that give power to all the subsystem of 1B8_CubePMT instead of processor. So there is no any involvement of this regulator with the processor. It draws high current from the power supply so that's why it consumes more power and contains a lot of noise problem. The schematic of the 3.3V Switching Regulator is shown in below Figure 5.9.

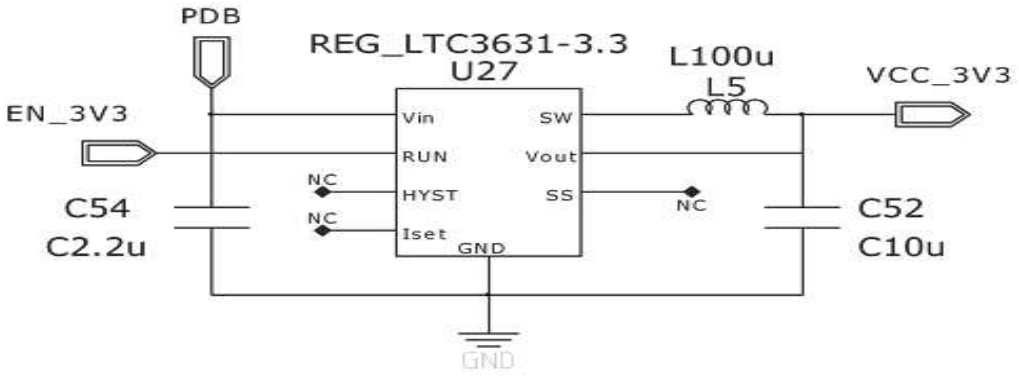


Figure 5.9: Schematic of the 3.3V Switching Regulator.

5.2.8 BK1B1253B 5V Switching Regulator:

This regulator gives 5V to all the subsystem of 1B8_CubePMT. It also draws high current from the power supply so that's why it consumes more power and contains a lot of noise problem. It is enabled from the Tile processor. The schematic of the 5V Switching Regulator is shown in below Figure 5.10.

Figure 3.13: Schematic of the 5V voltage supply

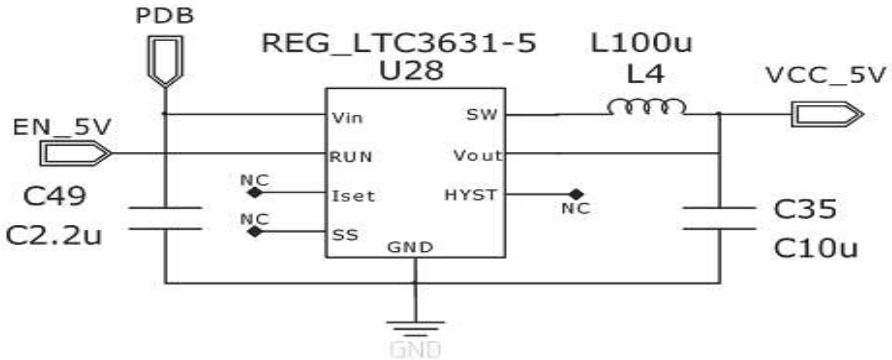


Figure 5.10: Schematic of the 5V Switching Regulator.

5.2.9 BK1B133A & BK1B133B Temperature Sensors:

Temperature sensor is the sensor that can sense the temperature with the help of NTC thermistor and give the output in the form of voltage. In 1B8_CubePMT_3U, there are two kinds of temperature sensor. One Temperature sensor (BK1B133A) measures the temperature within the range from -30˚C to 70˚C while the other temperature sensor (BK1B133B) measures the temperature range within the range from 0˚C to 120˚C .Between these temperature ranges, the

resistance value is varied between 2.2kΩ ~100kΩ and accordingly we will get the specified range of Output voltage (0 to 2.5V) by utilizing 3V of reference regulator.

In NTC thermistor, Temperature and output voltage are inversely proportional to each other. Lower the temperature is, the higher the value of voltage equal to 2.5V (within the dynamics of the A / D converter) and the increase of this value tends to decrease as temperature, more or less linearly. Tolerance level of Temperature sensors are almost 1% that corresponds to high accuracy. Here we choose BK1B133A temperature sensor for finding the output voltage. Its formula is given below:

$$\text{TEMP} = 3\text{V} * \frac{11\_R1 \,//\, 11\_R3}{11\_R1 \,//\, 11\_R3 + 11\_R2}$$

Where 11_R3=$R_{25}e^{\beta 25(\frac{1}{T}-\frac{1}{T25})}$,T_{25} =298.15K (Temperature at 25℃), R_{25}=100kΩ (resistance of sensor at 25℃) , β= 4100K. The schematic diagram of temperature sensor BK1B133A is shown in below figure 5.11.

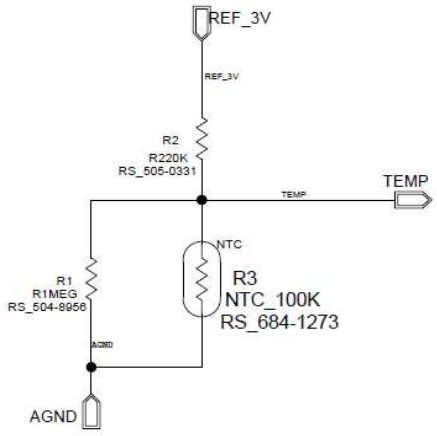


Figure 5.11: Schematic of Temperature sensors (a) -30˚C -70˚C temperature range (BK1B133A)

5.2.10 BK1B121 Load Switches:

Load switch provide cutoff power to the subsystem with the help of enable signal from the tile processor. It is usually placed at the input of each subsystem. With the help of this, we can better monitor the power dissipation of each subsystem. In 1B8Cube_PMT, there are two sorts of load switches. One is used for high voltage level especially for power distribution bus while the other is used for low voltage levels including 5V, 3.3V and 3V. Another important sort of load switch is 'Bidirectional load switch' that also play a major role in our project. These load switches will describe in step by step.

Before describing the working of different sorts of Load switches, it needs to know the selection of P-channel Mosfet instead of N-channel Mosfet. The reason is that it is simple to control the switching (on or off) block. Secondly, N-channel load switch need an extra voltage rail in order to control the gate but this is not required for P-channel load switch.

Moreover, Power transistor which is known as a Pass transistor has a diode in parallel to its channel. This creates an undesirable flow of current between two potential differences even when

the system is disconnected. In order to clear it, another bi-directional NMOS is required. So when the NMOS conduct the anode potential becomes less than cathode that fully disconnects the path of pass transistor. It leads to dissipate less power.

5.2.10.1 BK1B121C Low Voltage Load Switch:

BK1B121C Load switch is used for Low voltage level. In Attitude control system, low voltage (5V/3.3V/3V) load switch is used to give cutoff power to magnetorquer coil driver by enabling it from the tile processor.

Usually, Pass transistor (P-Channel) on and off are controlled by a small signal NMOS transistor. When enable signal is at low, NMOS transistor is switched off and the voltage on the gate reaches up to IN terminal. It means that no current will flow across the pass transistor and the voltage across gate and source assume to be the same. On the other hand, when enable signal is high, NMOS transistor turns on and the gate voltage of pass transistor switched to ground. In this way the pass transistor is switched on. As long as the voltage on IN terminal is higher than the threshold voltage of the P-channel transistor, it remains on and once the enable is low, it will again turn off.

As we increase the time between closing and opening of the PMOS, it will reduce the inrush current coming from the capacitor C32 of the boost converter. It will also prevent the external battery from power surge. The schematic of Low Voltage Load Switch is shown in below Figure 5.12.

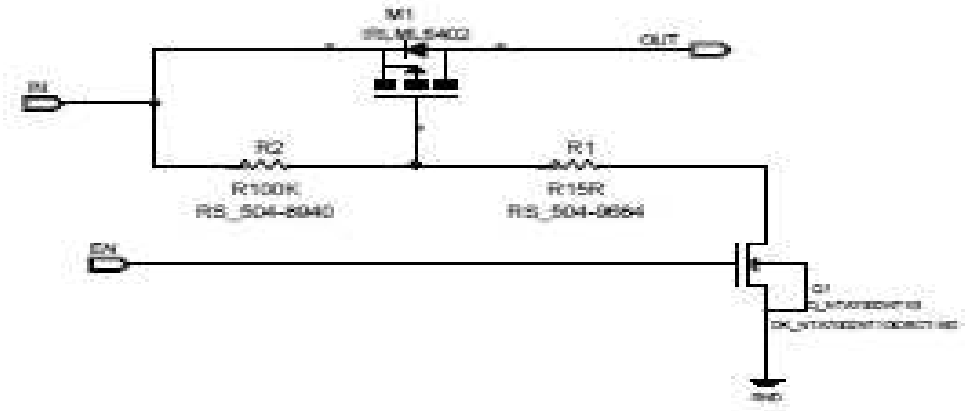


Figure 5.12: Schematic of Load Switch (a) Low Voltage.

5.2.10.2 BK1B121D High Voltage Load Switch:

BK1B121D Load switch is used for high voltage level. In Attitude control system, high voltage (PDB) load switch is also used to give cutoff power to magnetorquer coil driver by enabling it from the tile processor. Its schematic diagram is same as the previous load switch. Only the difference here is the values of the resistors R1 and R2. These values of resistors correspond to the rate of on/off switching of pass transistor that must be specified according to the requirement. The schematic of High Voltage Load Switch is shown in below Figure 5.13.

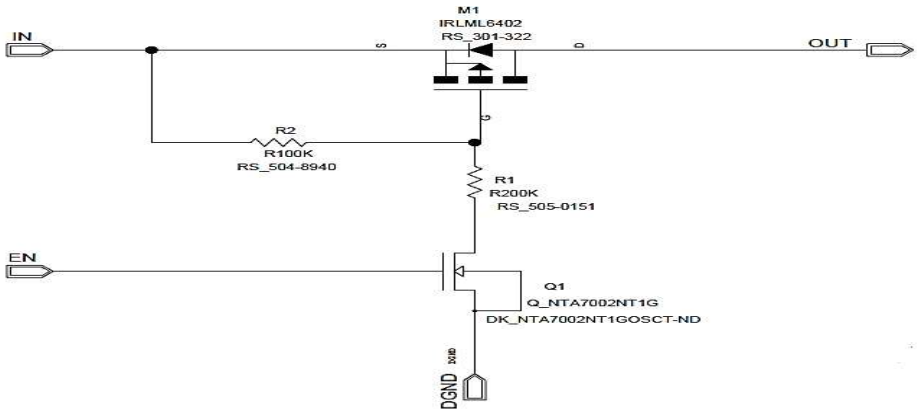


Figure 5.13: Schematic of Load Switch (b) High Voltage.

5.2.10.3 BK1B121E Bi-directional Load Switch:

Bidirectional load switch as the name tells is one of the important load switches in Aramis-C1.It is placed between power distribution bus and battery. This load switch helps in charging the battery from the power distribution bus in the presence of sunlight. On the other hand, the battery provides power to power distribution bus in the absence of sunlight. It is enabled from the tile processor. The schematic of Bidirectional Load Switch is shown in below Figure 5.14.

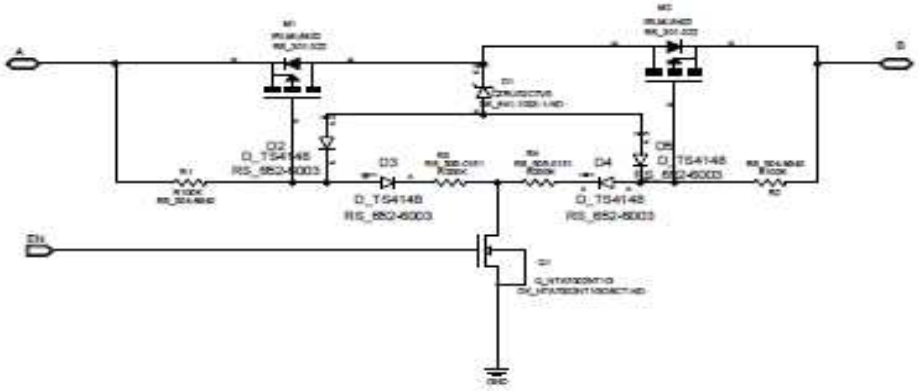


Figure 5.14: Schematic of Bidirectional Load Switch.

5.2.11 BK1B115B over Voltage Protection:

Over voltage protection circuit limits the PDB voltage for specified operation. It contains only two Zener diodes that are connected in back to back. One terminal is connected with positive terminal while the other is connected with ground. It keeps the voltage level equal to 20V. Its because the breakdown of each diode is 10V. The schematic of Over Voltage Protection is shown in below Figure 5.15.

Figure 5.15: Schematic of Over Voltage Protection circuit.

5.2.12 BK1B111B Solar Panel

This Solar Panel have two solar cells which are made from GaAs material whose efficiency is almost 26%.These are connected in series in order to generate 4.4V from both of them. We added a simple schottky diode across each solar cell that can help in generating 2.2V from single cell when the other cell becomes damaged. The schematic of Solar Panel is shown in below Figure 5.16.

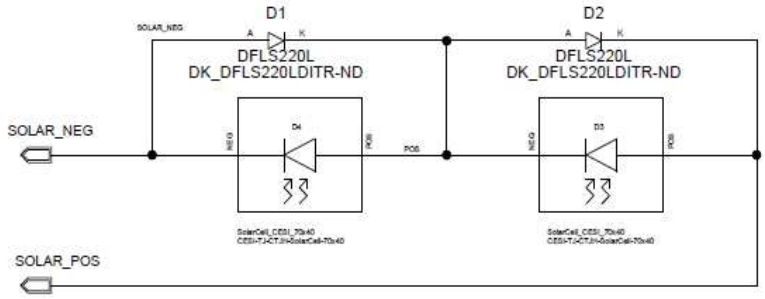


Figure 5.16: Schematic of series connected 2 Solar Cells.

5.2.13 BK1B111A Solar Panel

This Solar Panel has six solar cells which are made from GaAs material whose efficiency is almost 26%.These are connected in series in order to generate 13.2V from all of them. We added a simple schottky diode across each solar cell that can help in generating 2.2V from single cell when the other cell becomes damaged. The schematic of Solar Panel is shown in below Figure 5.17.

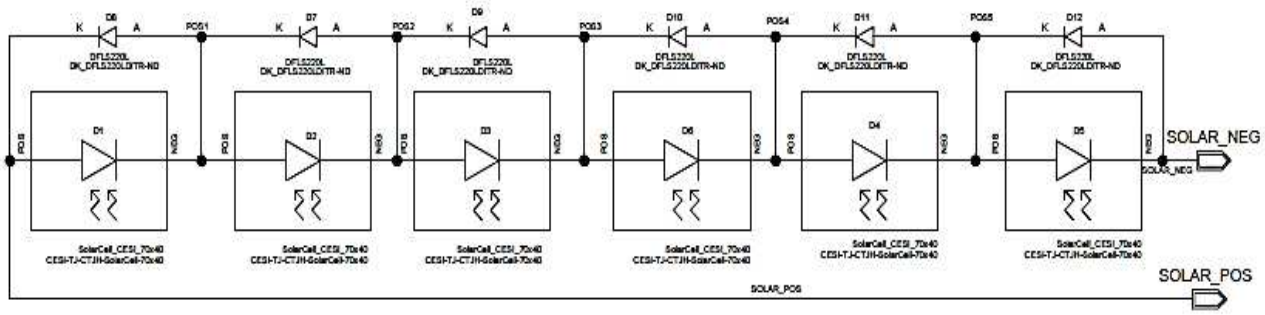


Figure 5.17: Schematic of series connected 6 Solar Cells.

Chapter 6
Attitude Determination and Control System

6.1 Introduction:

Attitude Determination and Control System (ADCS) on a 1B8_CubePMT provide an extra feature in the field of nanosatellite. Attitude determination sensor on each tile measures the satellite orientation in the orbit and gives this information to on board processor. On board computer compare this information with already defined values in the processor. This compared value is then processed by the attitude control system which indicates the desired direction of the satellite. ADCS block diagram is shown in below Figure 6.1.

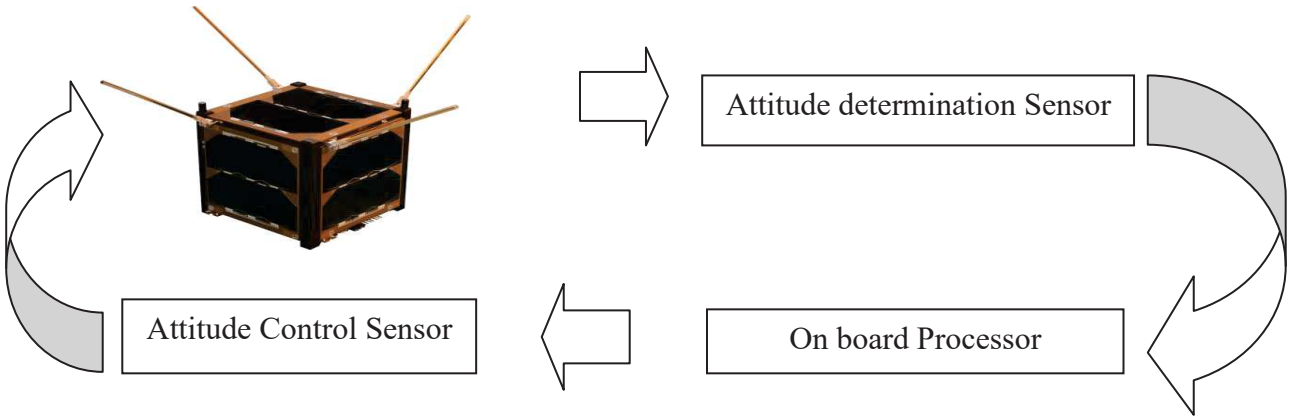


Figure 6.1: ADCS block diagram

The above picture shows the major difference between ADS and ACS is that ADS tells only orientation of the satellite while ACS manage the orientation of satellite. The ACS also tells the satellite face in front of sun or it points in the direction of earth. For this we choose permanent magnet because of its light in weight, economical and consume less power.

Another special feature of ADCS is generating torque to maintain the motion of satellite in desired position. For this, we use magnetorquer coil that does not need an extra place but just to embed it inside the PCB layers of 1B8_CubePMT. These coils are attached with each other through different type of straps. The magnetic field from this coil interacts with earth magnetic field that generates magnetic moment and cause torque for the stabilization.

6.2 Attitude Determination System:

Attitude Determination System is divided into three parts which are given below:

- Sun Sensor.
- Magnetometer.
- Gyroscope.

Different number of attitude sensors in each axis of satellite is shown in below Table 6.1:

Types of Attitude Determination Sensor	Number of attitude sensor in each axis		
	X-axis	Y-axis	Z-axis
Sun Sensor	2	2	1
Magnetometer	2	2	4
Gyroscope	2	2	0

Table 6.1: Number of attitude sensors in each axis

6.2.1 BK1B235 Sun Sensor:

A sensor that works in the presence of sunlight in order to determine the attitude parameter of satellite is known as sun sensor. It is composed of monolithic photovoltaic solar cell CPC1822 which give the output voltage when light fall on it. This generated voltage is enough to operate the tile processor (0V to 2.5V). The tile processor then computes it when no load at the output is equal to 4.75V or 75uA when it is short circuit. The theoretical formula of measuring output voltage is given below.

$$V_o = V_{max}\cos(\theta)$$

Where θ is the incident angle of light on the sun sensor and

$$V_{max} = 1.65 \pm 20\%$$

Schematic diagram of sun sensor is shown in below Figure 6.2.

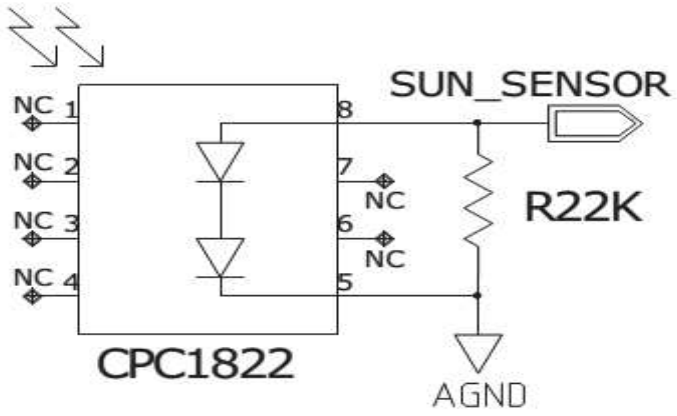


Figure 6.2: Schematic of sun sensor.

6.2.2 BK1B221 Magnetometer:

A sensor that measures the earth magnetic field for the determination of attitude parameter is known as Magnetometer. A Set/Reset circuit is used in order to refresh the magnetometer. It actually reduces interference effect due to magnetic element. HMC1002 magnetometer based on AMR technology is chosen because of its cheap price and easily available COTS in the market. It measure the low magnetic field (from -2 to 2 G) along 2-axis with high sensitivity and reliability.

When earth magnetic field (-0.625 to 0.625 G) is incident on this sensor, it give the output (0 to 2.5V) to the tile processor. It is because of two Wheatstone bridge A and B that convert this incident magnetic field to two differential output voltage VA and VB. Here we are considering one bridge for the calculation of expected output voltage VA that is given below.

$$V_A = K_M . B_x + V_{off}$$

Where sensitivity in mV/G is K_M , V_{off} is offset Voltage and B_x is magnetic field in G.

Two operational amplifiers OP1177 and AD8226 are used before giving the output voltage.OP1177 act as a buffer which will give the output toward the reference terminal of AD8226. The output of the OP1177 is calculated by using voltage divider rule which we shown below.

$$\frac{R8}{R8 + R6} \times REF\_3V = \frac{1K}{1K + 1K} \times 3V = 1.5V$$

Each connected output amplifier have gain=15.96 and V_{off}=1.5V. Both R1 and R2 can change the gain of amplifier which can be design like given below:

$$A_D = 1 + \frac{49.4K\Omega}{R_G}$$

$$R_4 = R_5 = \frac{49.4K\Omega}{A_D - 1} = 3.302K\Omega$$

By putting the value of resistors in above equation of gain, the obtained value is equal to 15.96. Similarly R8 and R9 are responsible to affect the offset voltage but we can neglect this effect due to its low value. At the end of this circuit, schottky diodes are used after these amplifiers that can limit the maximum output voltage equal to 3.3V.

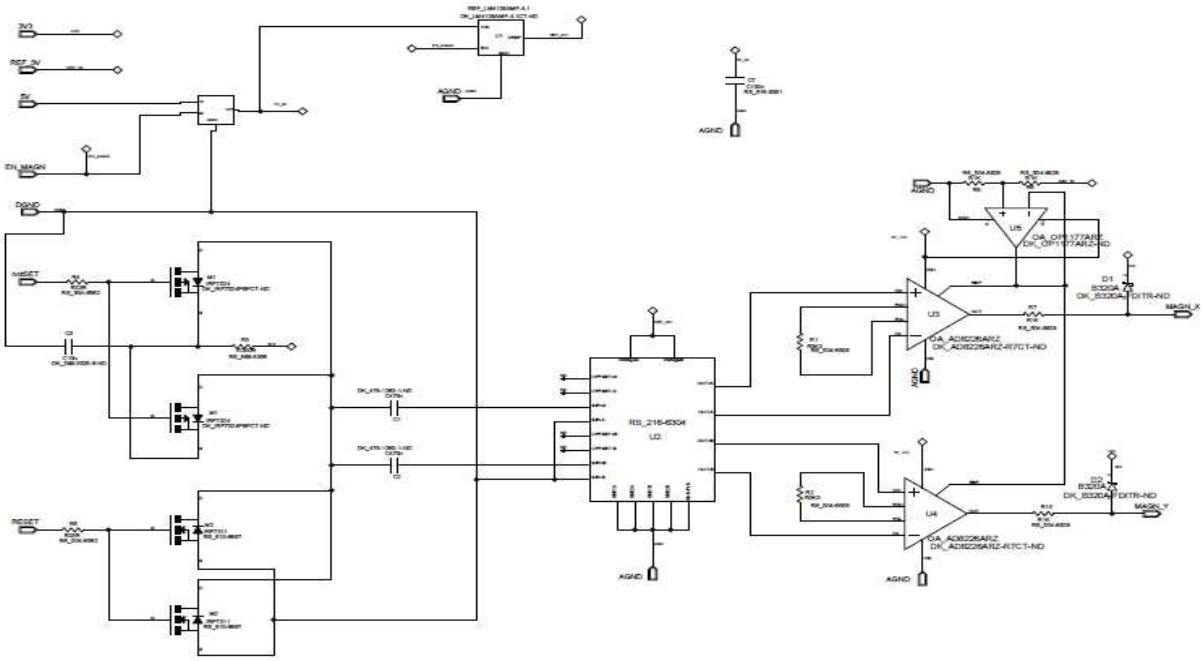


Figure 6.3: Schematic of the magnetometer subsystem.

6.2.3 BK1B211B Gyroscope:

A device used for measuring angular velocity is known as Gyroscope. It is a digital sensor ADIS16080 on 1B8_CubePMT whose dynamic range is $\pm 80\,°/\text{sec}$. Digital values on serial peripheral interface mean that gyroscope is revolving with suitable angle. These digital values will give to the tile processor through SPI port that compute it in the range of $\pm$ 2rpm. Noise density effect on tile processor has the frequency range from 0.1Hz to 40Hz. When we apply 1Hz filter through software, the remaining noise become 0.0025rpm which is so small that once can easily predict attitude stabilized value. So in this way we get the more accurate result of attitude determination sensor.

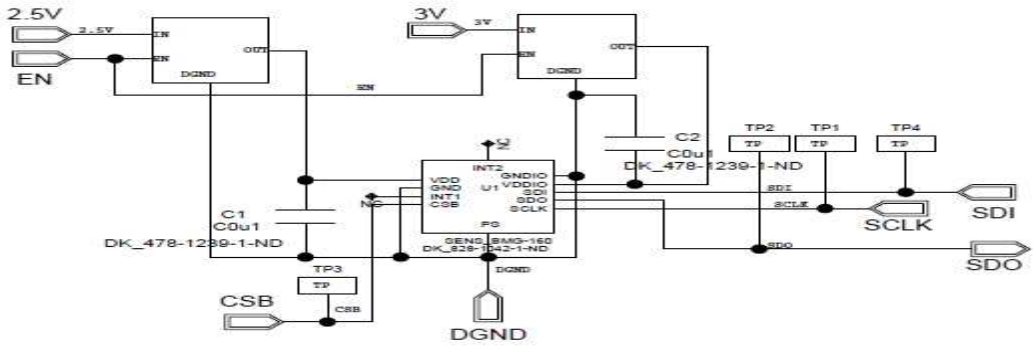


Figure 6.4: Gyroscope block diagram.

6.3 Magnetorquer System:

Magnetorquer system is divided into two parts:

- Magnetorquer Coil Driver
- Magnetorquer Coil

6.3.1 1B222 Magnetic Torque Actuator:

Magnetic torque actuator consists of magnetorquer coil driver, load switch and differential voltage sensor. High and Low Load switches provide cut-off power to magnetorquer coil driver when they are enabled from the tile processor. Magnetorquer coil driver has a pulse width modulation motor driver IC that controls the direction of current flow. Two output pins OUT1 and OUT2 are connected with magnetorquer coil while the input pins attached with tile processor that includes not BRAKE, not ENABLE, PHASE and MODE. These pins are helpful in order to perform the coil in different configuration including the current in forward, reverse, stop or the standby. Differential voltage sensor maintains the maximum current flow between coil and its driver. Its schematic diagram is shown in below Figure 6.5.

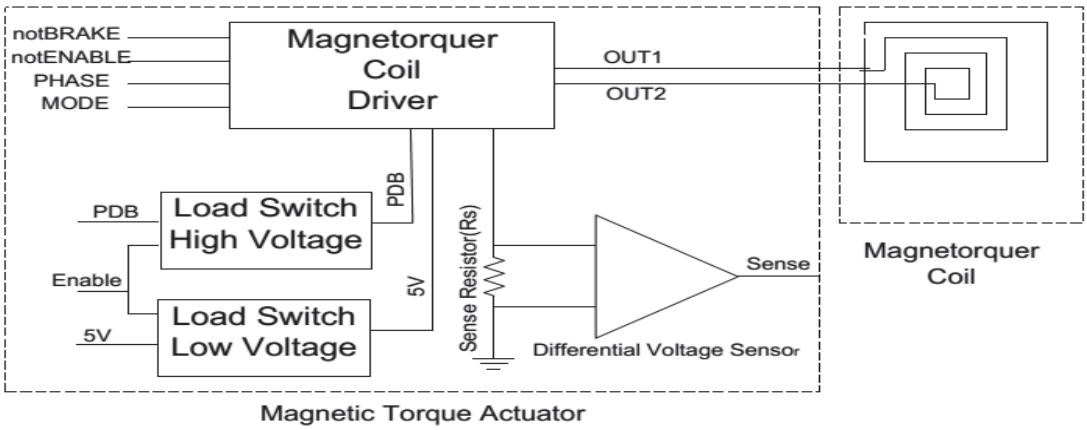


Figure 6.5: Magnetorquer subsystem block diagram.

If we go further inside the magnetorquer coil driver, it is seen that a two directional current is flowing through the magnetorquer coil driver. In one time, transistor Q1 and Q3 are switched on that cause the direction of current flow from left to right. During this time, transistor Q2 and Q4 remain open. Similarly, when transistor Q2 and Q4 are switch on that cause the direction of current flow from right to left. During this time, transistor Q1 and Q3 remain open. These directions of current are shown by green dashed lines in two different columns. The four diodes D1, D2, D3 and D4 in front of each transistor are used to protect the circuit for de-energizing the coil. The internal circuitry of this IC is shown in below Figure 6.6.

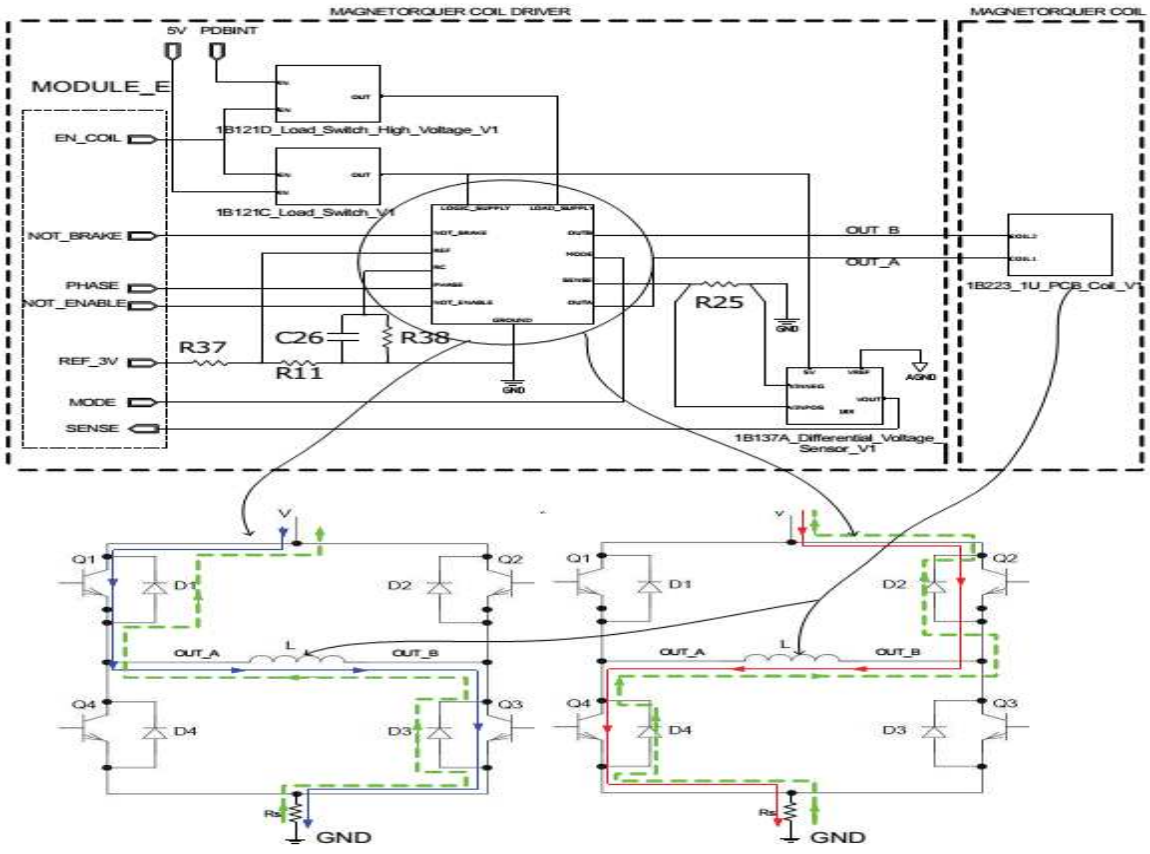


Figure 6.6: Magnetic Torque Actuator and its internal circuitry.

6.3.2 1B223 Magnetorquer Coil:

Magnetorquer coil generates magnetic field when current flow through it that interacts with the earth magnetic field and the resulting torque is used to orient the satellite in any desired direction. The meaning of desired direction means that whether the direction of Solar Panel is directed toward the Sun or the direction of Antenna is directed toward the Ground Station. Magnetorquer coil is embedded inside the four layer (fourth, fifth, sixth and seventh) of 1B8_CubePMT in order to maintain the flow of current for attitude control system. Each coil has turns equal to 50, so the total number of turns in the PCB become 200. It does not require any extra space in the schematic diagram. This coil must be energized in order to maintain the orientation of satellite.

- **Working Principle:**

From the theoretical point of view, when current flow through a solenoid, a magnetic moment $\vec{D}$ is generated which is shown below:

$$D = N.S.I$$

Where N is the number of turns of the coil, S is the area of the single turn and I is the current through the coil. By right hand rule, one can easily find the direction of clockwise current through coil represented by curly fingers while the thumb indicates the direction of magnetic moment$\vec{D}$.

Its actual diagram is shown in below Figure 6.7.

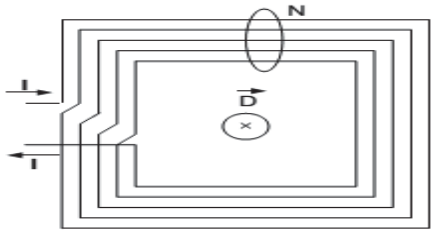


Figure 6.7: Direction of current flow in a current carrying coil

When current flows through coil, magnetic field $\vec{B}$ is generated that produce the torque τ.It is shown in below equation:

$$\vec{\tau} = \vec{D} \times \vec{B} = \vec{D}\,\vec{B}\sin\theta\,\hat{n}$$

Where θ is the angle between $\vec{D}$ and $\vec{B}$ and $\hat{n}$ is unit vector normal to the plane containing $\vec{D}$ and$\vec{B}$. It is actually a cross product between $\vec{D}$ and $\vec{B}$ that has maximum torque when $\vec{D}$ and $\vec{B}$ are perpendicular to each other while it is minimum when $\vec{D}$ and $\vec{B}$ are in the same plane.

Their actual diagrams along with its parameters are shown in below Figure 6.8.

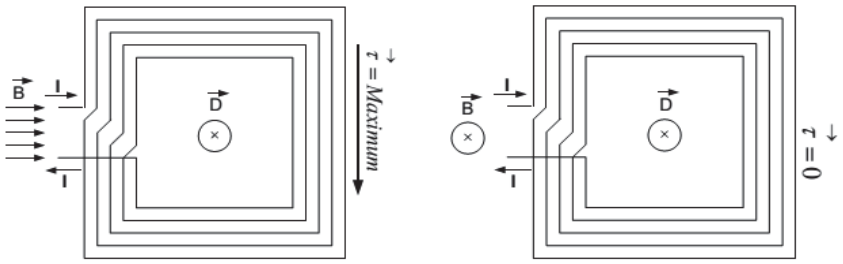


Figure 6.8: Magnetic field $\vec{B}$, magnetic moment $\vec{D}$ and resultant torque τ

6.3.2.2 Magnetorquer Coil Design:

In order to design the complex coil for 3U version, we need to be careful about the length of coil in zigzag form. This zigzag form the coil is because of the fact that we need to use additional holes due to support of this lengthy PCB.

The length of the Magnetorquer coil is proportional to its resistance which corresponds to the magnetic moment, power consumption and heat generation. 1B8_CubePMT_1U required 50 numbers of turns in each layer, while its 3U version contains only 30 numbers of turns. We also wanted the same number of turns in each layer as far as the concern of more magnetic moment thus more torque is produced but the problem occurs was that when we increased three times the size of PCB then it cover a large amount of area which restrict the generation of magnetic moment. Strictly speaking we don't want to increase the number of turns of the coil without increasing the magnetic moment. So we are restricted to 30 numbers of turns in each layer as we get the maximum peak of magnetic moment with acceptable power. In this way we used 120 numbers of turns in all the four layers. Their results are shown in below figures 4.9 and 4.10.

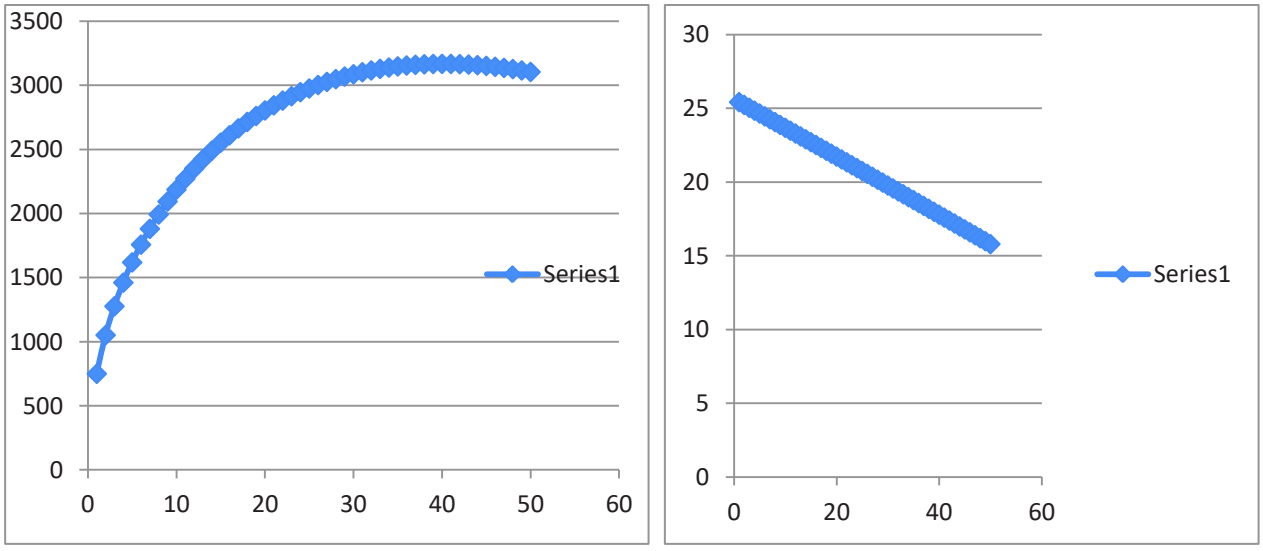


Figure 6.9: Magnetic Moment VS 50 turns of Coil and Magnetic Moment/Power Consumption

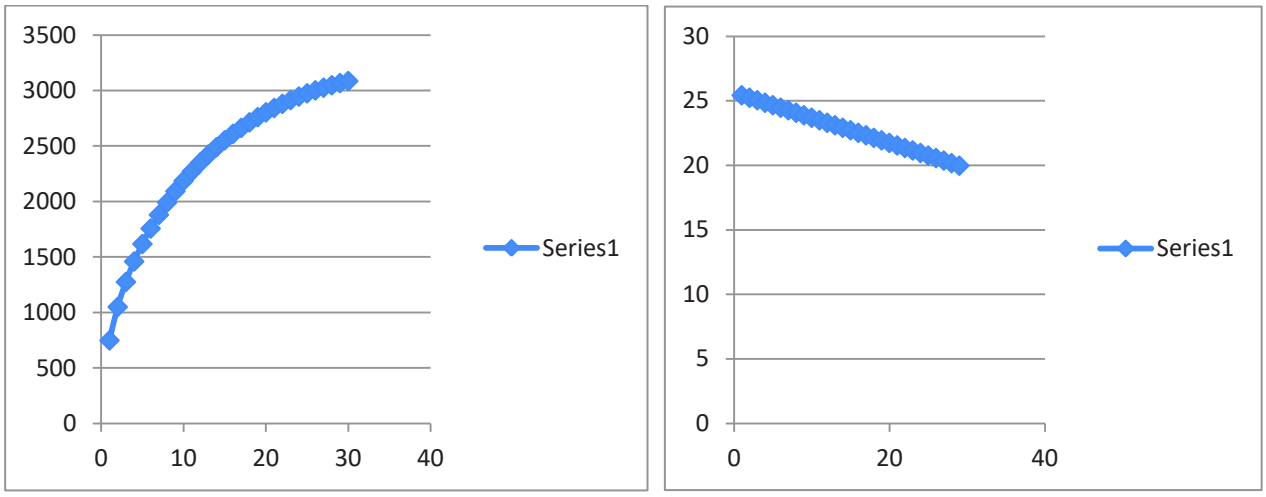


Figure 6.10: Magnetic Moment VS 30 turns of Coil and Magnetic Moment/Power Consumption

Each coil trace has a width of 0.3mm and a thickness of 18µm. Space between adjacent traces is 0.2mm. We can say that the distance between the centers of two trace is 0.5 mm. All these parameters are discussed in the coming sections. A cross sectional view of the 1B8_CubePMT_3U version is shown in below figure 6.11.

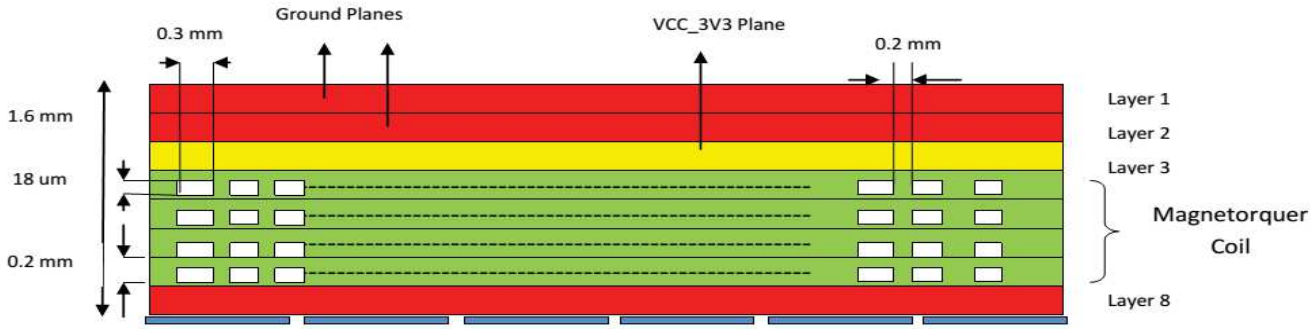


Figure 6.11: Magnetorquer Coil traces inside the 1B8_CubePMT_3U version

The following diagram shows the cell of Magnetorquer coil in which I mentioned the vertical and horizontal lengths of the square shape and also for the separation area between two squares.

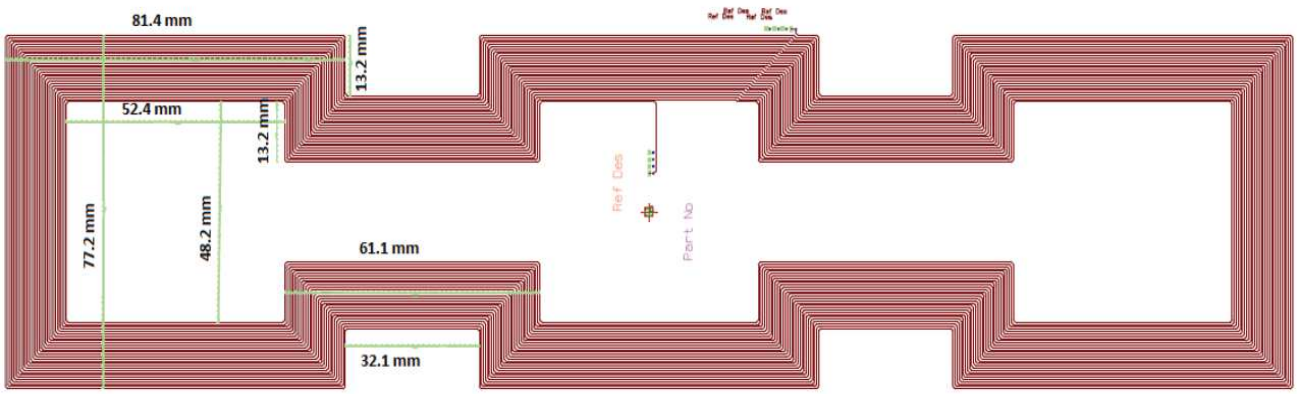


Figure 6.12: Dimensions of Single Coil Magnetorquer Coil 3U

Parameters	Values for 3U
Single turn average length; lavg	818.8 mm
Total length of single coil; Lt	24.379 m
Trace cross sectional Area; A=w×t	0.3mm×18 μm
Total area occupied by single coil	0.36 m^2
Distance between two adjacent traces	0.2 mm
Bundle width (30 traces)	15 mm
Copper resistivity (from manufacturer),	3×10^{-8} Ωm
Single coil resistance, Ro	135.4 Ω

Table 6.2: Dimension parameters of the magnetorquer coil

6.4 Magnetic Moment versus Power Dissipated:

Magnetic Moment and Power Dissipation are the important terms in designing the magnetic torque coil. Magnetorquer coil generates magnetic moment when current pass through it. As a result of this magnetic moment, the coil dissipates power respectively. Magnetic moment across the coil is calculated as given below.

$$\vec{D} = M \cdot \overrightarrow{D_o}$$

Where M is the number of Coil connected in any fashion (Series, Parallel or Hybrid). Secondly, the power consumed by single turn is calculated as given below

$$P_o = {I_o}^2 R_o \quad \text{Where } R_o = \rho \frac{L_t}{A}$$

Where Io is the current flow in a single coil, Ro is the resistance of the single coil and Po is the power consumed by single coil. So, the Power consumed by M turns of coils connected in any possible fashion is given by

$$P = M \cdot P_o \qquad \therefore I = m\, I_O$$

$$\therefore V = n\, V_o$$

$$\therefore M = m \times n$$

The ratio of magnetic moment and power consumed is calculated as given below.

$$\frac{D_o}{P_o} = \frac{N.S.I_O}{R_O.{I_o}^2} = (\frac{N.S}{R_o})\frac{1}{I_o}$$

$${D_o}^2 = \frac{(N.S)^2}{R_o} . P_o$$

$D^2 = n.m.\frac{(N.S)^2}{R_o} . P = K.P$ (Where k is a constant of proportionality that change its value by changing the number of coils in series, parallel or hybrid fashion)

6.4.1 Effect of Torque:

When the Earth magnetic field and magnetic moment of the coil during the current flow in the coil interact with each other in the sense that it produce an external force that help in the motion of the satellite in desired direction. This external force is known as Torque. Torque generation is actually depends on the amount of current flow through different combination of coils .This torque is calculated as given below.

$$\tau = B.D.\sin\theta = B .\sin\theta . N.S.I$$

Where B is the magnetic field of the earth and D is the magnetic moment of the coil that should always perpendicular to each other in order to generate torque in third axis. It is better to explain in the following diagram.

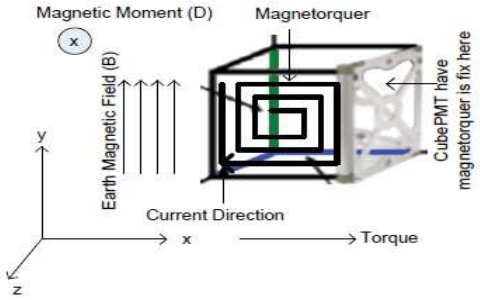


Figure 6.13: Interaction of Coil and Earth Magnetic Field

Chapter 7
Development of Components in Dx-Designer

7.1 Introduction:

This chapter is related to how to use the Dx-Designer Mentor Graphics. In Aramis_Mentor_Lib library, there are seven main features that are interlinked with each other. Here I am going to mention it.

- Parts
- Cells
- Symbols
- Padstacks
- Reusable Blocks
- Models
- Model Mappings

In order to explain it step by step, I would like to start it from the Padstack.

7.1.1 Development of Padstacks:

In order to make a new padstack inside the padstack editor, first of all I have to right click on any folder (e.g. All) and make a new padstack by giving a new name for this padstacks. Inside the padstack editor, I have to remove bug which are already present from the list and then I have to select Pads from the Pad tab. Inside the Pad tab there are many types of Pad especially Round, Oblong, Square, Rectangle, Octagon, Elongated Octagon, Radius Corner Rectangle, Chamfered Rectangle, Round Finger, 4 Web Round Thermal, 4 Web Round Thermal-45, 2 Web Round Thermal, 2 Web Round Thermal-45, 4 Web Oblong Thermal, 4 Web Oblong Thermal-45, 4 Web Square Thermal, 4 Web Square Thermal-45, 4 Web Rectangle Thermal, 4 Web Rectangle Thermal-45, Round Donut and Square Donut. I have to choose any of them and then I have to give the parameters for example for Round Pad I have to give the diameter of the circle and give the X and Y offset equal to 0 so that it would place in proper position inside the padstack. Once I make the pad then go to Padstacks tab and select the type of Padstacks. I have to choose one type from all padstack type including Pin-SMD, Pin-Through, Mounting Hole, Tooling Hole, Shearing Hole, Via, Fudicial, Pin-Die and Bondpad and then put the new pad which I created before inside the default list. The parameters of pad for top and bottom mount should always be little less then top and bottom mount of solder mask and solder paste. The reason for this is that in practically, the size of hole across solder mask is always less than our expectation and sometime it would be displaced from the exact position. The list of all padstacks inside the library is shown in below figure 6.1.

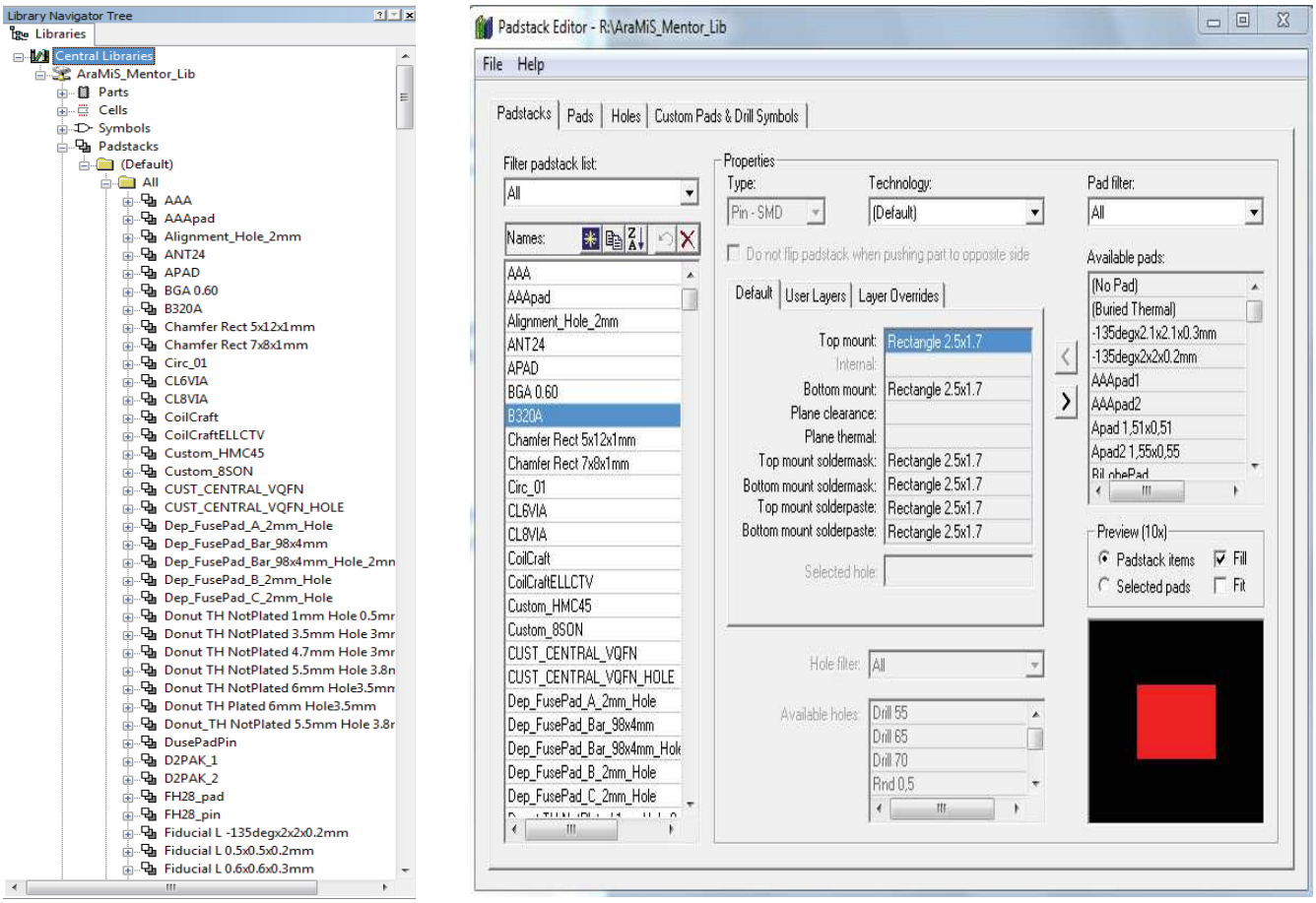


Figure 7.1: Creation of Padstack in Padstacks Editor

7.1.2 Development of Cells:

In order to make a new cell inside the cell editor, first of all I have to right click on any folder (e.g. Anwar) inside the cell and make a new package cell by giving a new name for this cell. Inside this block, I have to mention the total number of pins need for this new cell, layers while editing cell, package group and mount type technique. Inside the cell editor, there are three operational modes in side of it which I mentioned below.

- Place
- Route
- Draw

These operations will be explained in the next chapter but for the time being, it's better to explain on how to place the pins for making the cell. Once I open the place pins from the toolbar then it is shown in the place parameters tab that I have to make pin sequence by selecting the pin pattern whether to fill from left to right or from right to left and so on. Above of this pattern I have to define the number of column and rows along with its spacing between two pins. In the pattern placement I have to select to select the type of pattern especially in my project, I used the pattern of SOIC for making new cell and I rotated some padstack according to make exact cell as it was mentioned in the datasheet. On the left side of the dialog box, I have to make new pins by select and adding the padstack from the list. These Padstacks are already present inside the library as this is the

most important step before creating new cell. I have to add all the pins which I defined before and place it accordingly on the main screen of cell editor. Once I place all the Padstacks on the main screen then I have to add place placement outline, place assembly outline and place silkscreen outline accordingly. Lastly I have to add the conductive shape at the corner of the silkscreen outline for making proper dimension of the component on the printed circuit board. I have mentioned the final form of cell inside the Cell editor in below figure 6.2.

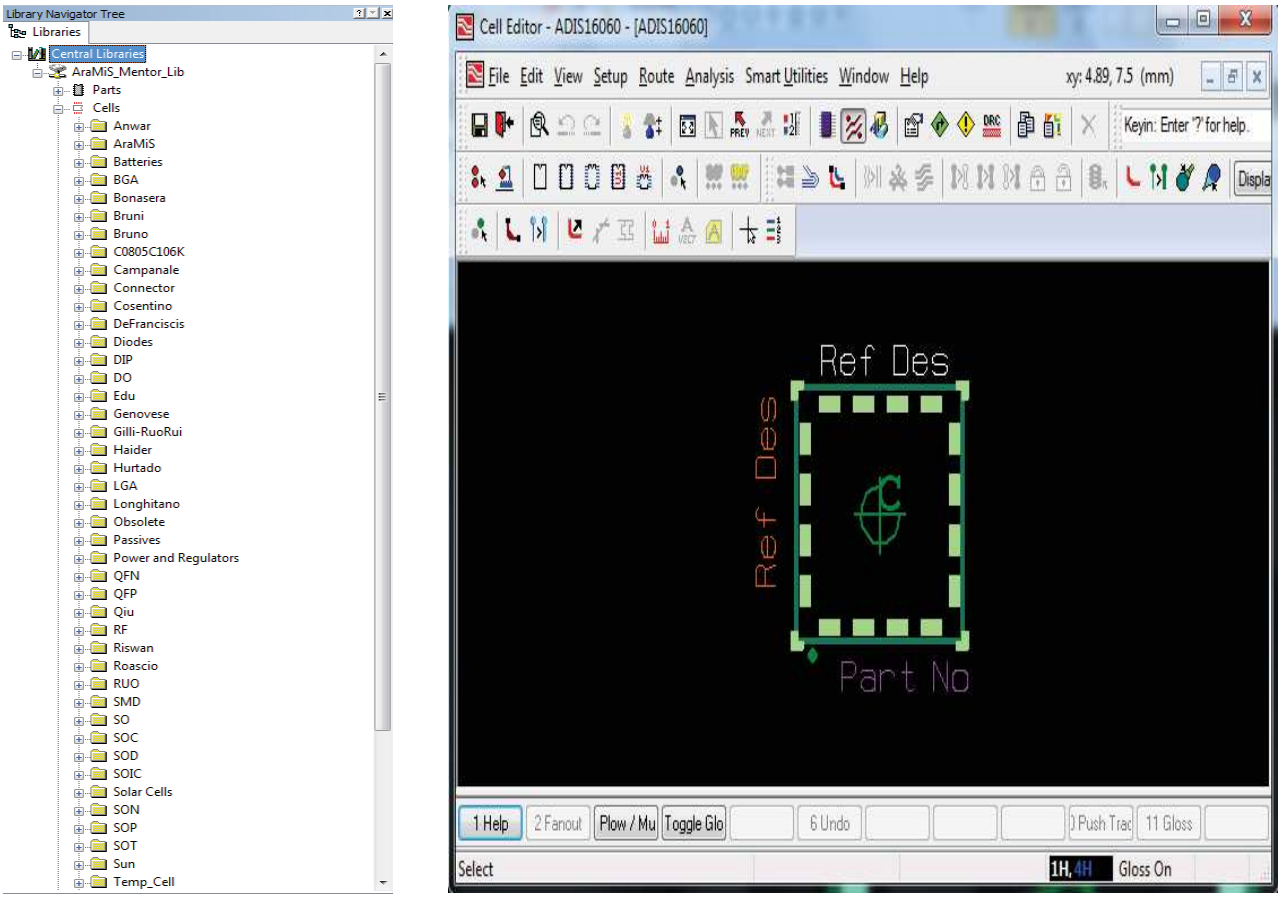


Figure 7.2: Creation of Cell in Cell Editor

7.1.3 Development of Symbols:

In order to make a new symbol inside the symbol editor, first of all I have to right click on any folder (e.g. Anwar) inside the symbol and make a new symbol by giving a new name for this symbol. Inside the symbol editor, there are four operational windows use for it. First of all make the block in the symbol window with the help of some drawing tools. These drawing tools are available inside the toolbar especially square, circle, arc etc. After that choose the pins from the tool bar and attach it with chosen block according to the desired position for making new pins of the integrated IC. After that it is possible to edit all the pins inside the pin window. This edit can help to rename the pin along with to change the type of pin. The types of pins mean some pins are usually for the input signal and some are for the output signal. I have to edit these pins types accordingly. Property window help to add or remove the property of the symbols. These properties are related with printed circuit board or if the component has some spice model then I have to add X for mentioning

the model property. Lastly, the console window helps to type the script command. This window shows all the error and warning automatically while doing wrong step for the symbol.

Once the symbol has been created then surround the symbol with bounding box so that it defines the area in the schematic. The origin of the symbol should always be placed at the bottom left border of the symbol outline otherwise it will give a wrong adjustment of symbol inside the schematic. I have mentioned the final form of symbol inside the symbol editor in below figure 6.3.

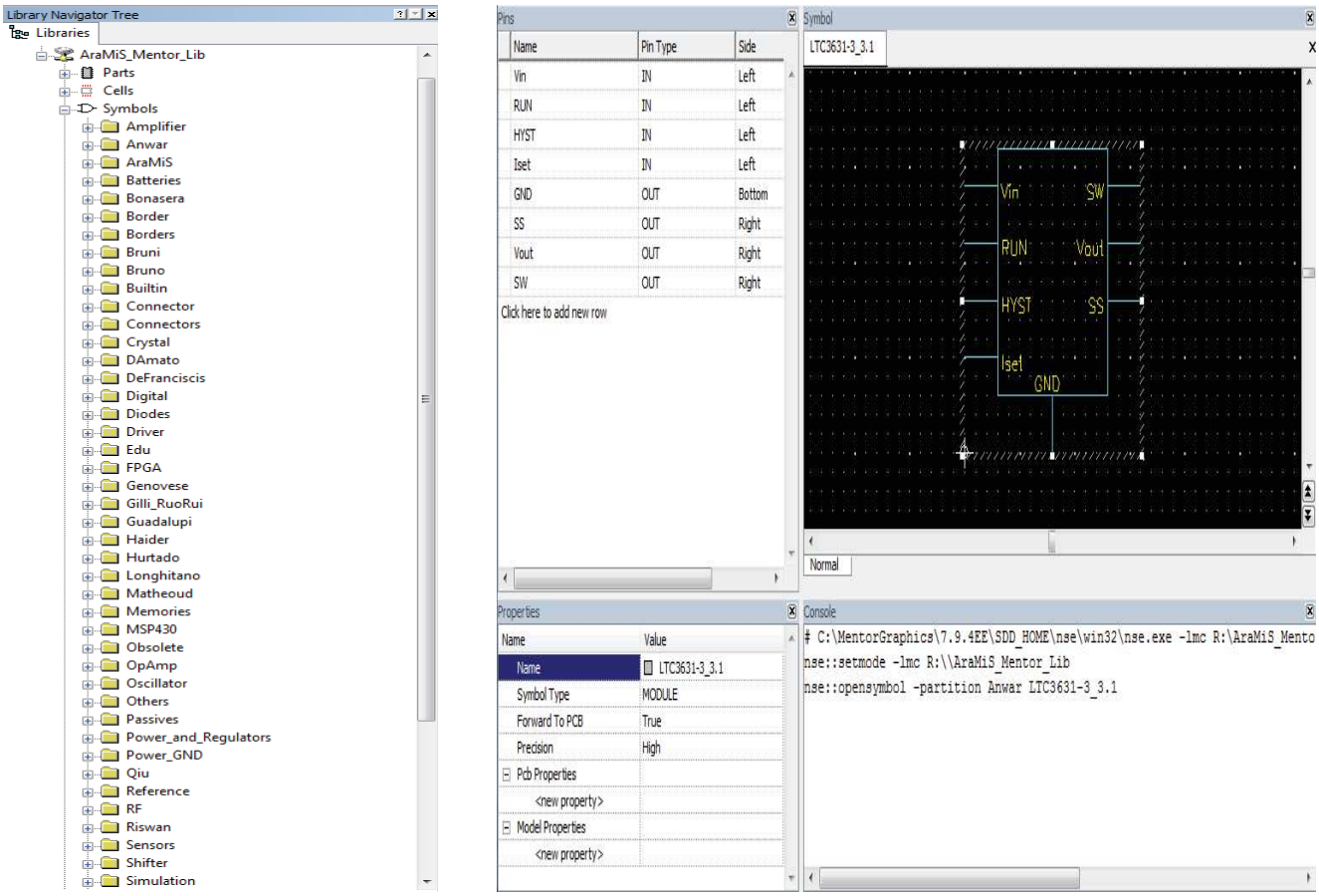


Figure 7.3: Creation of Symbol in Symbol Editor

7.1.4 Development of Parts:

In order to make a new part inside the part editor, first of all I have to right click across on the All folder and make a new padstack. Inside the padstack editor

In order to make a new part inside the part editor, there are two options for it.

- Create a new part by clicking on the new icon. Then choose the partition and a row inside the part editor. Once it come inside the part editor, then write the correct part number, part name and part label of the component according to the datasheet. After that always choose distinct part number from the datasheet like Supplier number. Edit the part name according to the information related to package and it is always

small as it does not require the distinct name. Lastly, additional information known as Part label is not necessary but it's important as it contains the information related to electrical parameters.

- Create a new part by choosing any part from the list then copy this part by clicking on the copy icon. This will appear a new part just below the original part. This part editor need to change this new part number otherwise both the part name will be same and software will not allow do it. For the part name and part label, it would be the same as it is mentioned above.

Once the correct part is added inside the part editor table then below there is a component properties box where I can add the proper values of some parameters especially Power dissipation, Tech, Class and Model. Near to this property box, there is a reference designator prefix for example for Integrated circuit its prefix is U and for Resistor its prefix is R. I have mentioned the final form of symbol inside the symbol editor in below figure 6.4.

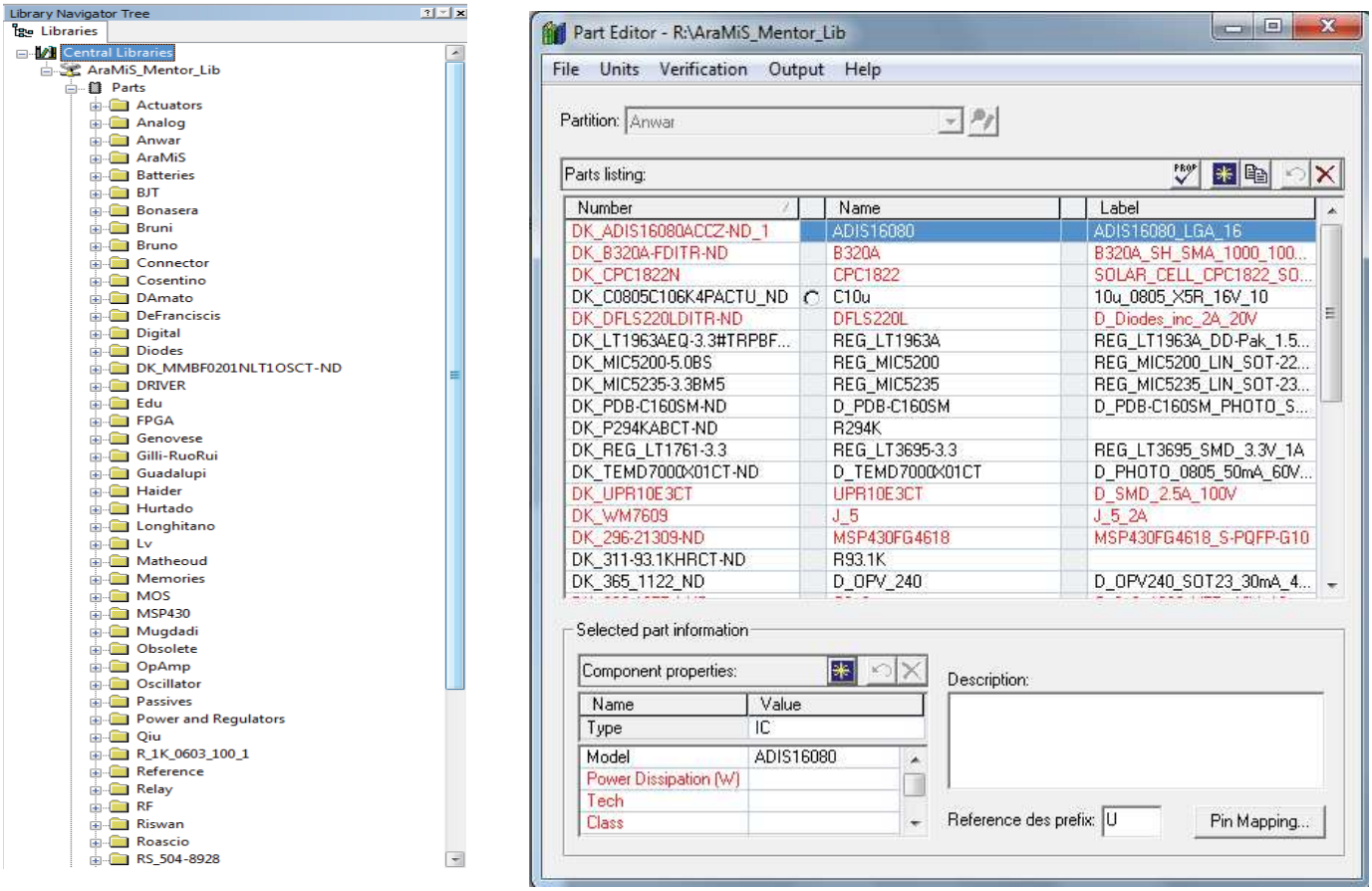


Figure 7.4: Creation of Part in Part Editor

The next step is assigning the correct symbol and package cell to this part. This action will be possible after clicking the dialog box of Pin mapping. Inside the pin mapping, there is an icon for importing the already available symbol from the library and near to this; there is another icon available for creating the new symbol on the left side. On the right side, there is an icon for

importing the already available cell from the library and near to this; there is another icon available for creating the new cell.

When I want to import the symbol, then I have to choose the right symbol from the list. This can be assured once I see the symbolic view of this symbol below this dialog box. After that I have to choose select to create new gate information, enter the number of slots, Include pin property and pin property mapping. Similarly, when I want to import the cell, then I have to choose the right cell from the list. There is a library partition along with number of pins and package group. This is very useful to find correct cell from the library very fast and this can be assured once I see the symbolic view of this cell below this dialog box. The last option is to choose the option for putting the cell on the top of the layer, bottom of the layer or alternate. This alternate option is to place the component either by surface mount technique or through hole technique.

After importing the cell and symbol in order to make the part, I have to assign the physical pins of the components as it defines inside the datasheet. For example in below figure, I take the pin # 1 from the logical pins and then move it toward anode A inside slot # 1. Similarly for pin #2 I move it logical pins toward cathode K inside slot # 1.

Once I imported the symbols and cells then I have to select Apply on these changes and then OK. The imported cell and symbol and their pin mapping is shown in below figure 6.5.

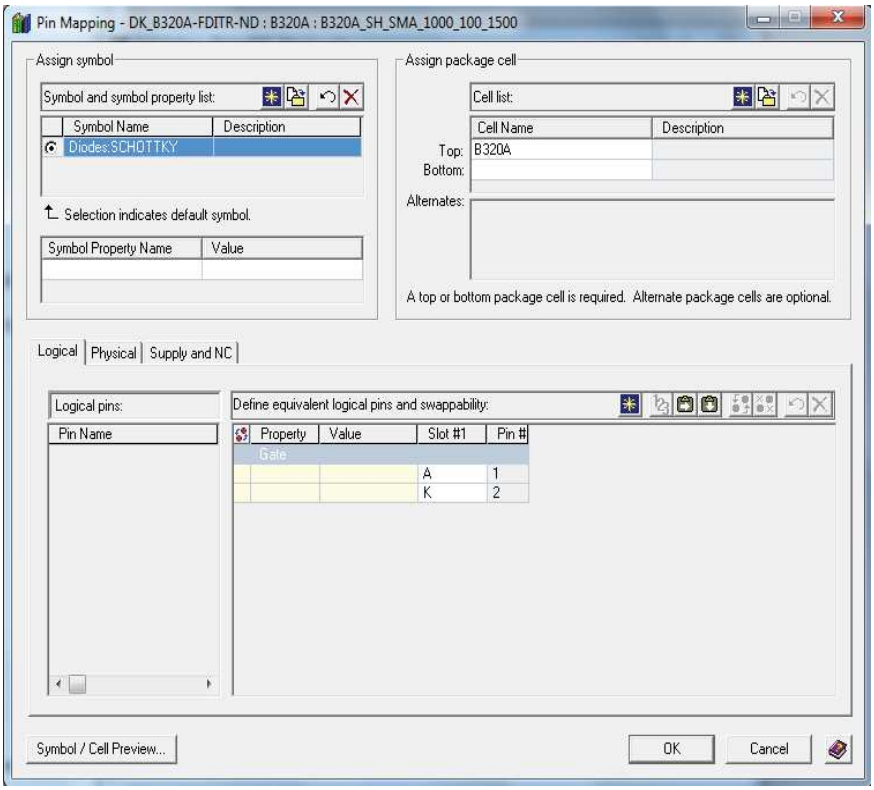


Figure 7.5: Import Cell, Symbol and their Pin Mapping

7.1.5 Development of Reusable block:

In this library, there is special type of blocks whose name is ‘Reusable Blocks’. It contain logical, physical and both logical and physical block that are used in our project. Logical block mean it

contains only the circuit diagram, physical block mean it is composed of only the layout of the circuit diagram. It is helpful for the production of printed circuit board and both Physical and Logical block contain the components of the circuit from the layout to its application level. Additionally, these reusable blocks are helpful in order to improve the electronic components by removing all the errors inside of it. This improvement is possible by editing the affected block directly on the schematic. This way can save the time and energy.

In order to make a new reusable block inside the library, first of all I have to copy and paste my main project and then open this 1B8_CubePMT-Copy project on Dx-Designer and then I have to remove all the blocks of this copied project except one of them which I want to make it reusable. After that create the board of this block and close the project. Then I have to open the Library manager then go to the section of Reusable block. Then right click on the Logical-Only folder and then choose the option of 'New Logical-only Reusable Block' and give the new name to this reusable block and then it will show this reusable block inside the Logical-Only folder.

In order to package and Net list of this reusable block, I have to verify this block and then open it. If I open this reusable block without verifying then it will go in Read only mode and then I will not be able to modify any components. After removing all the errors, I have to package all the components of this reusable block and then Net list it in order to generate spi file. At the end I have to verify this reusable block and use it in any schematic as a reusable block. I have mentioned the final form of reusable block inside the library in below figure 6.6.

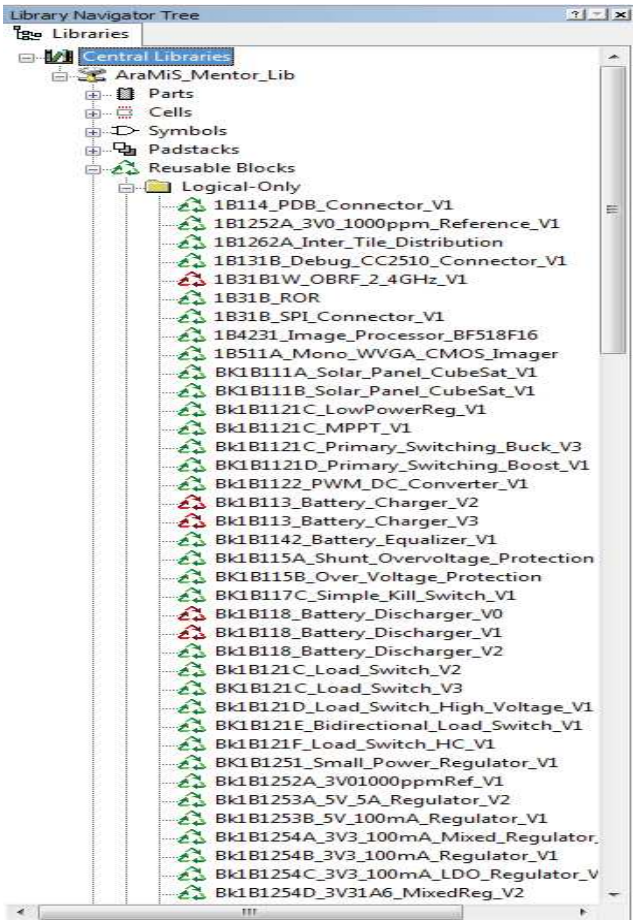


Figure 7.6: Creation of Reusable block in Library Manager

7.1.6 Development of Models:

In order to make a spice model for any component of the project, I can import a model or make a new one. For importing the existing model, I have to import it by right clicking on the passive folder and import the spice model from another folder.

For making a new model, there are two options for it. One is to find the spice model of specific part number of component on the internet. Usually there are free spice models are available on the internet, just download the text format of this model and save as the .mod format and save this mod file in the specific directory which I am going to mention it below.

R:\AraMiS_Mentor_Lib\Models\Spice\Passives

If the spice model is not available on the internet then I have to create the spice model myself. For this I have to open the datasheet of specific component and then understand the characteristic of that component by seeing its output/input graphs. Usually for passive components, it would be easy to make the spice model but for active components like transistor or some regulator, it would be quite difficult in order to make the new spice model on the text document and once I created the spice model then I have to save it in .mod form inside the above directory. I have mentioned the final form of Spice model inside the library in below figure 6.7.

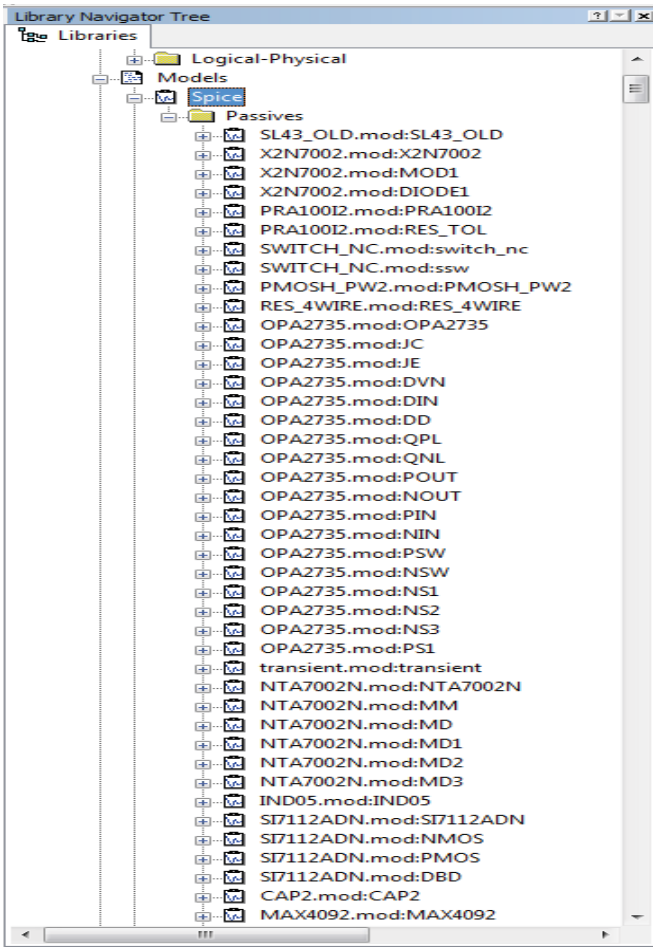


Figure 7.7: Creation of Spice Model in Library Manager

7.1.7 Development of Model Mapping:

Model Mapping is the last feature of the Mentor Library Manager. With the help of this model mapping, I can see the how the physical and logical layer s of the part is related with each other and the association with the model layer with the part. All these information show in one place make the environment user friendly. In order to make the proper mapping of model, I have to add spice model in correct path. If there is some spice model missing of the specific part then there will show nothing inside the spice model. So from there I have to make sure that in order to use this part in my schematic, I have to add the spice model in the required directory so that I can make the proper Net list and use this part easily for the simulation point of view. I have mentioned the final form of Model Mapping inside the library in below figure 6.8.

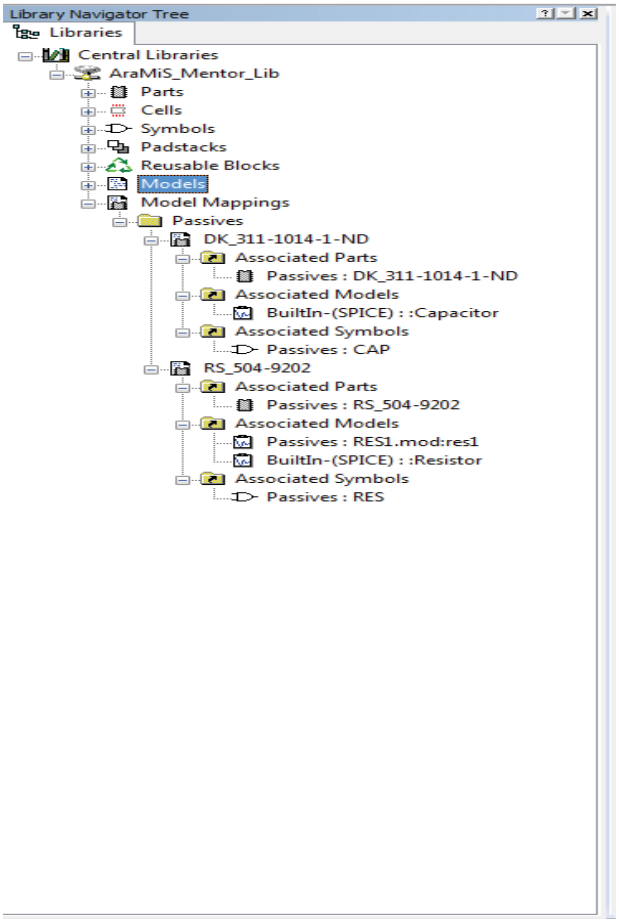


Figure 7.8: Creation of Model Mapping in Library Manager

Chapter 8

Realization of PCB for 1B8_CubePMT_3U and Mechanical Analysis of the Board

8.1 Introduction:

The PCB for 1B8_CubePMT was realized using the software Expedition PCB. The PCB developed is mounted on the AraMiS structure for the functioning of the system and also to provide mechanical structure to the satellite.

8.2 PCB Dimensions:

The dimensions are 324.9mm x 82.5mm, these dimensions of the PCB are designed considering the standards of AraMiS. Some constraints posed on the size of the board are:

- From the figure below, it can be observed that this 1B8_CubePMT_3U is almost three times bigger than 1B8_CubePMT_1U.
- Since 1B8_CubePMT_3U has larger size than the previous board, so I have plenty of place to put its own components and also to put others component for controlling other tiles (e.g.1B423_On Board Computer).

The eight holes of 5.5mm are placed at the border and some additional 16 holes are placed at the middle of the tiles. These are used to affix the board to satellite with the suitable screws. The height of the components and various devices are considered during analysis to ensure that we have the necessary space to implant suitable characteristic payload mission.

8.3 Positioning Of Components:

Once the schematic is designed using the Design Capture .The Schematic is packaged by using the command (Tools →Package), which then maps the symbols in the schematic to the cells in the Expedition PCB. This allows us to place the corresponding components used in the schematic in the design space of Expedition PCB. Whenever there is a change made in the schematic, the schematic needs to be packaged to forward these changes to the Expedition PCB. Forward annotation in the Expedition helps in keeping updated with the schematic. Backward annotation is also present to map the changes from the Expedition PCB to the Schematic. The board designed is made up of eight layers. The layers are defined as shown in the below figure 8.1:

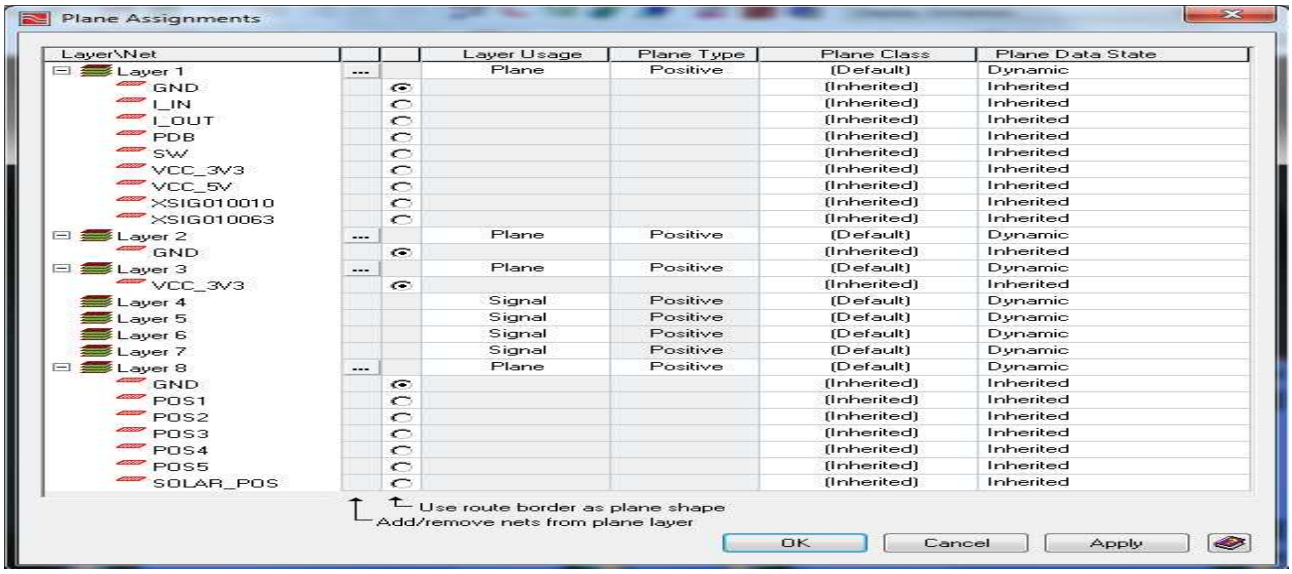


Figure 8.1: Plane assignments

These layers are defined in the following way step by step.

Layer 1:

It is a positive plane assigned to GND and most of the components are placed in this layer for Power Management, Attitude determination and control system. I placed all the components related to its Power Management, its Attitude determination and control system. I also placed another processor and its connectors for connecting other systems (e.g. on board computer) on this layer. In this way it maintains high power consumption.

Secondly, in this layer I added some extra nets from plane layer including I_IN, I_OUT, PDB, SW, VCC_3V3, VCC_5V, XSIG010010 and XSIG010063. These net added because of making the high power nets for switching regulator and also for the Boost converter as it is available inside the datasheet. The reason to make these nets was that these required for the switching regulator as followed the instructions of these regulators according to its datasheet.

Layer 2:

It is also positive plane assigned to GND. The reason to make it ground was that this layer help to protect all the components on first layer from magnetic field generated from the layer (fourth to seventh layer). Even for large number of nets in the first layer it's possible to make the appropriate connection by making Vias manually (passing from second or third layer and then come to its first layer).

Layer 3:

It is a positive plane and it assigned to VCC_3V3. The reason to make it 3.3V was that most of the components of the first layer require 3.3V to operate. Even for large number of nets in the first layer it's possible to make the appropriate connection by making Vias manually (passing from second or third layer and then come to its first layer).

Layer 4 to 7:

From fourth to seventh layer is a positive signal. Inside this, I placed the thirty turns of the coil across each layer. These 120 turns of coil in this printed circuit board is enough to generate the magnetic field according to acceptable values of Magnetic Moment/Power Consumption.

Layer 8:

It is a positive plane assigned to ground. I placed the remaining components especially Sun Sensor, Solar Panel and Schottky diode. Secondly, in this layer I added some nets including GND, POS1, POS2, POS3, POS4, POS5, and SOLAR_POS from plane layer. The reason to make these nets was that these nets linked with thicker lines of solar panels that allow higher current to pass through it.

The positioning of components are done by considering the main components especially Processor, Switching Regulators and the Coil of the Boost and then followed by Resistors, Capacitors which are assigned to the control signals then subsequently the bypass capacitors are placed. Once these components are placed, the connectors such as PDB, JTAG, I2C, RS232, and Module Interface for connected another processor.

At first, the processor is placed on the top layer, in the centre portion of the board considering that it connects with the most of the components in the board and also directly with other modules. But once I add another processor then I adjusted the place at the corner side of the printed Circuit Board. JTAG is always connected near to the processor for the programming purpose. I have shown the placement of all the components of first layer in below figure 8.2.

Figure 8.2: Placements of components in 1B8_CubePMT_3U

In processor MSP430F5438IPZR, the power supply line VCC_CPU has 5 pin distributed among the components and there are some bypass capacitors of different type to have greater frequency range. These bypass capacitors are placed near to the processor as it can be observed from the figure below.

For the HMC1002 with the power supply line 5V_int, it has three input pins distributed among the components and it has one bypass capacitor of values 100nf that are placed near the Magnetometer as shown in the datasheet.

In case of Magnetorquer coil Actuator, DRV_A3953 has two supply lines (5V_int and PDBINT_EN) for two pins and capacitors of 100nf are used as a bypass capacitor. This driver has five input pins distributed among the components. This bypass capacitor is always connected between their relative voltages and ground signal.

The layout of switching regulator has to be considered seriously as the EMI must be minimized and to assure proper operation. The problems are eliminated by having high level of integration and it is difficult to have efficient operation with a poor layout. These certain rules are to be followed for avoiding grounding and also problems related to heat sink.

- The Cin is placed as close to VIN and GND of LTC3631-5V.
- The Cout capacitor is also intended to be placed as close as possible between the Vout and the GND of the LTC3631-5V.
- The capacitors Cin and Cout are placed in such a way that the current flows adjacent to the LTC3631-5V.
- The nets to connect two terminal of Inductor L1 should be passed between Cin and Cout connected at the terminal 2 and 6 of LTC3631-5V.
- There are many Vias placed in the GND plane so that it acts as a heat pipes to other layers of the PCB.

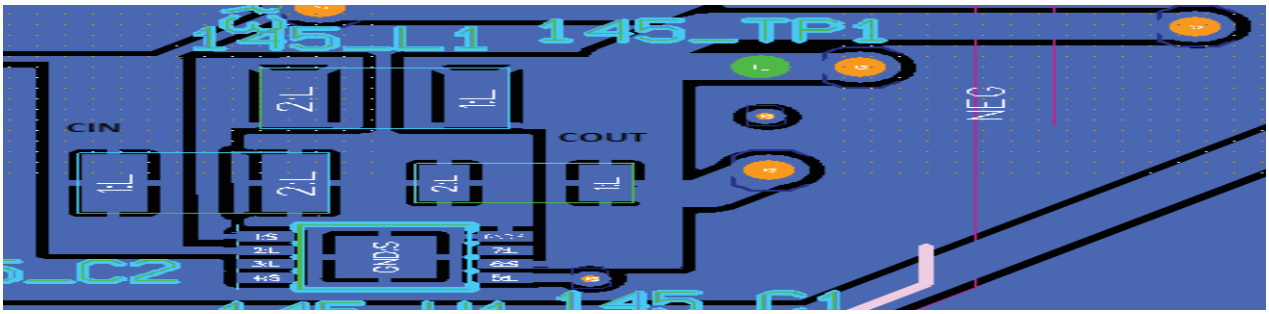


Figure 8.3: PCB Layout of Switching Regulator.

Finally, the connectors are placed after these components are placed. The JTAG connector is intended to be placed as close to the processor, due to the other components occupying the space and having reduced space, it couldn't be placed as near to the processor as expected. The BK1B4856_Module_Interface has been attached as the system gives the supply voltages 1B8_CubePMT to the 1B4231 onboard computer and Image Processor for the functioning of the system. Finally, the test points are placed at necessary positions to verify the functioning of the hardware after the realization of the PCB and for further testing of hardware.

8.4 Routing:

The CES (Constraint Editor System) helps in the control of the routing (size, Net classes) in the PCB. The trace widths associated to each net class and the clearances should be clearly defined. The minimum distance between the trace and the pads, between the pads and traces, between the traces and Vias, between the two pads can be edited in the Constraint editor system. In the editor control we can check that the appropriate layers are assigned and used for routing.

SOLAR		...	(default)	☑	10	50
COIL		...	(default)	☑	10	50
PDB		...	(default)	☑	10	50
POWER_5		...	(default)	☑	10	50
POWER_3V3		...	(default)	☑	10	20

Figure 8.4: Net classes defined in CES

Initially, we begin with Auto route which is been controlled by rules specified by the user and the routing algorithms. Subsequently, the other traces were routed manually .The width of the traces carrying the power signal is made relatively higher than the traces carrying the other signals.

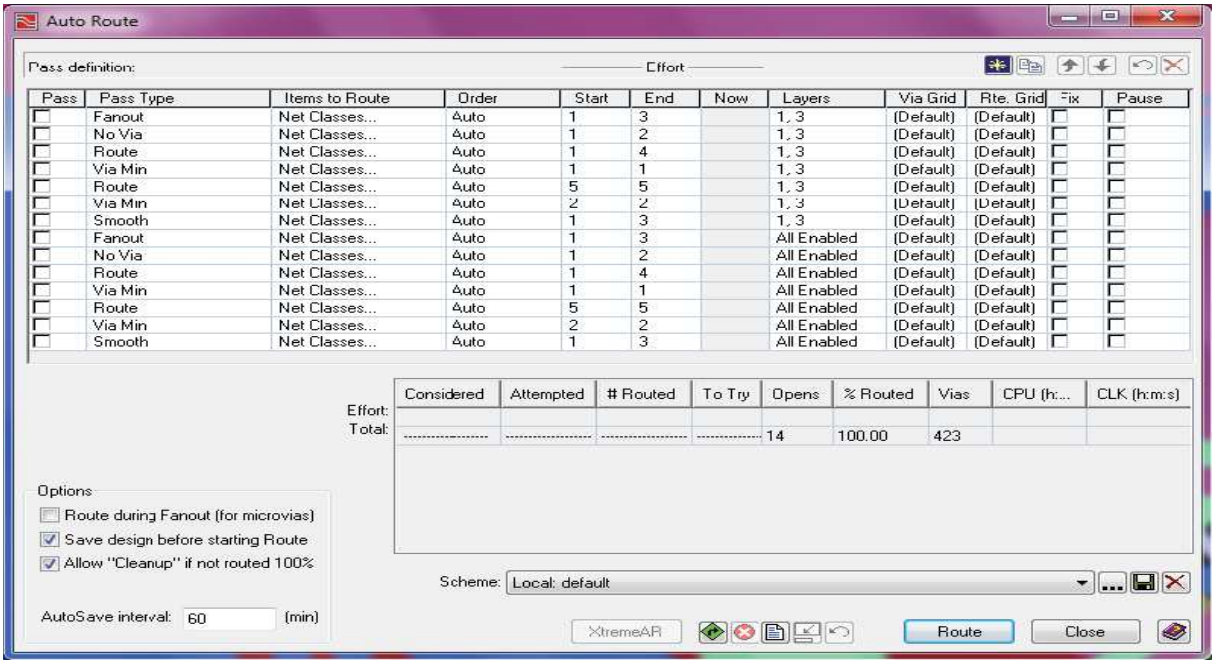


Figure 8.5: Auto route controlled by the user

The Auto route pass types are defined below:

- The Fan out helps to provide connections to the components in all the enabled layers.
- No Via allows us in routing the vertical and also horizontal signals without adding any Vias.
- Route establishes connection that was not completed over the past passes. This pass can be used also for routing the buses without bus path.
- Via min, it helps in increasing the space of the board by reducing the Vias through adding meanders. In boards where space is a major constraint we can increase the effort to allow meanders.
- Smooth helps in rerouting the Vias and pins.
- Remove hangers allows us to remove the pins that are not terminated and also for the Vias.

The printed circuit board designed previously is visualized on eight layers, which constitutes the PCB.

Layer 1

In Layer 1, the most of the components are placed and routed; the Connectors are placed on the bottom of the board, as we can see from the figure below 8.6.

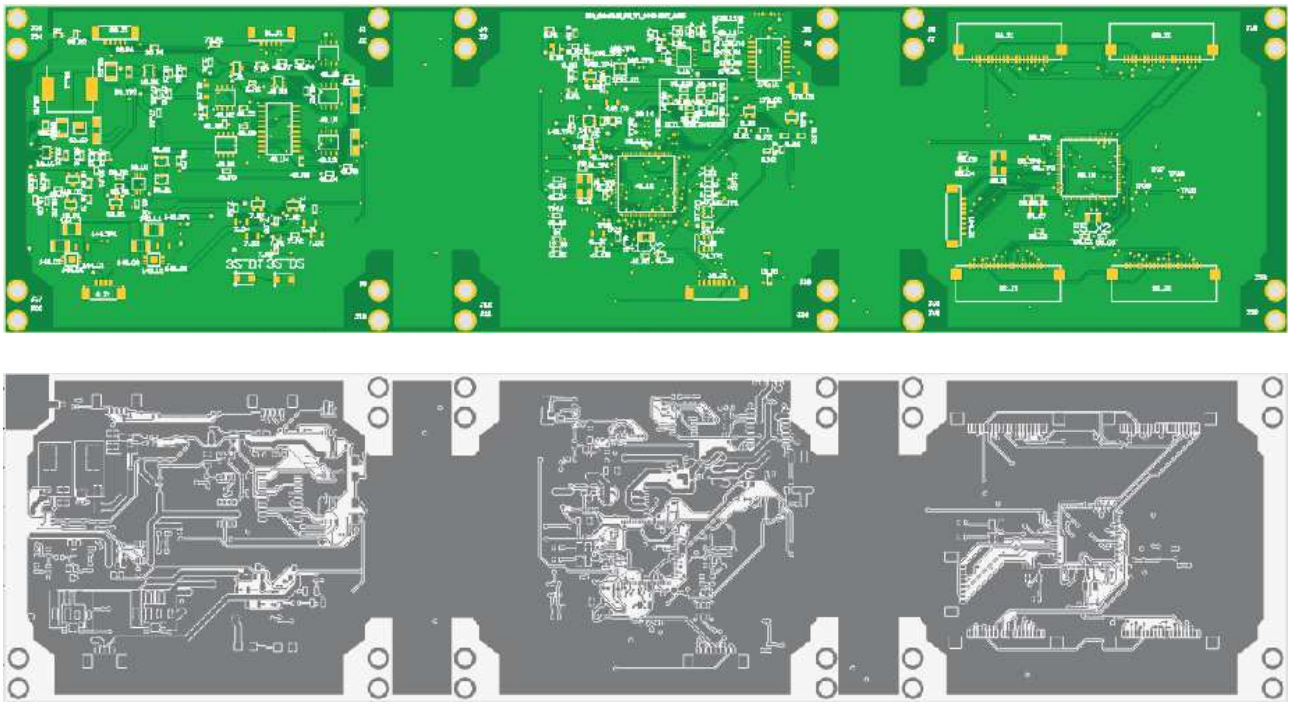


Figure 8.6: View of Top Layer and its Copper

Layer 2

In Layer 2, the ground plane is used and there is no routing of the traces and it is shown in the figure below 7.8.

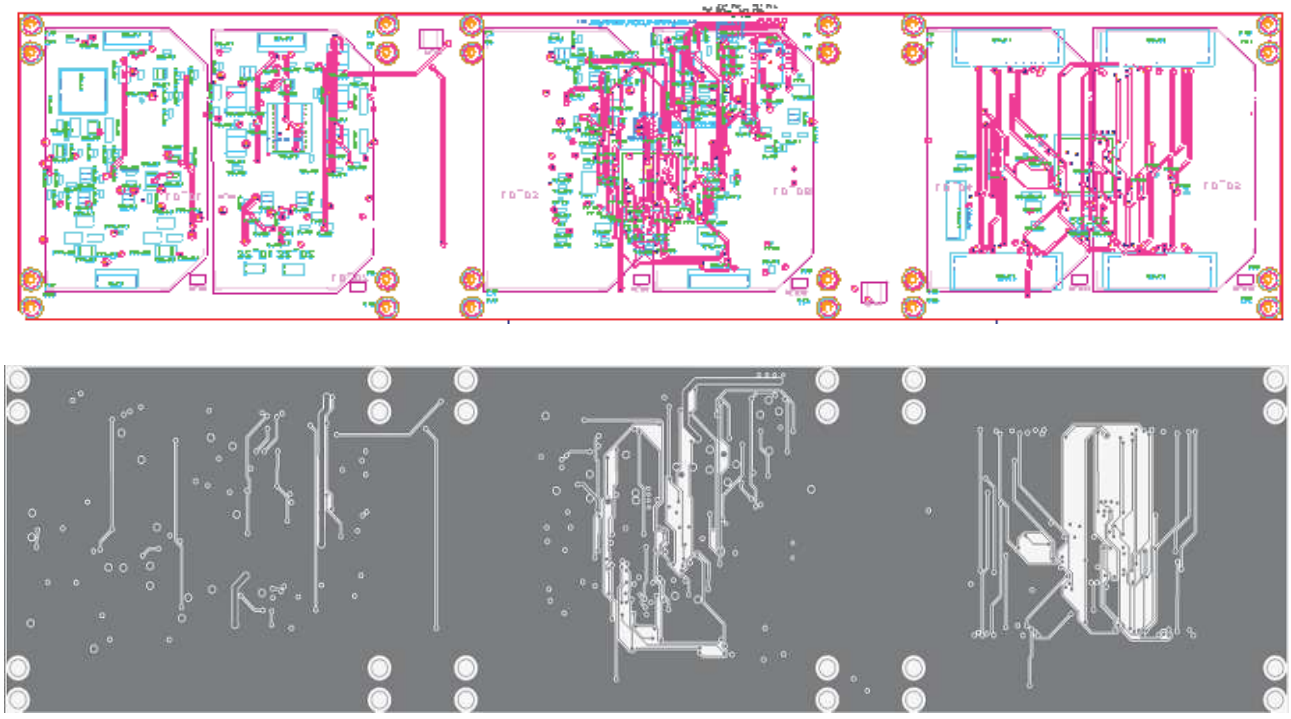


Figure 8.7: View of Layer 2 and its Copper

Layer 3

The layer 3 carries the most used power signal 3.3 V of the system. The trace width is wider due to low heat dissipation in the printed circuit board. It is shown in the figure below 7.9.

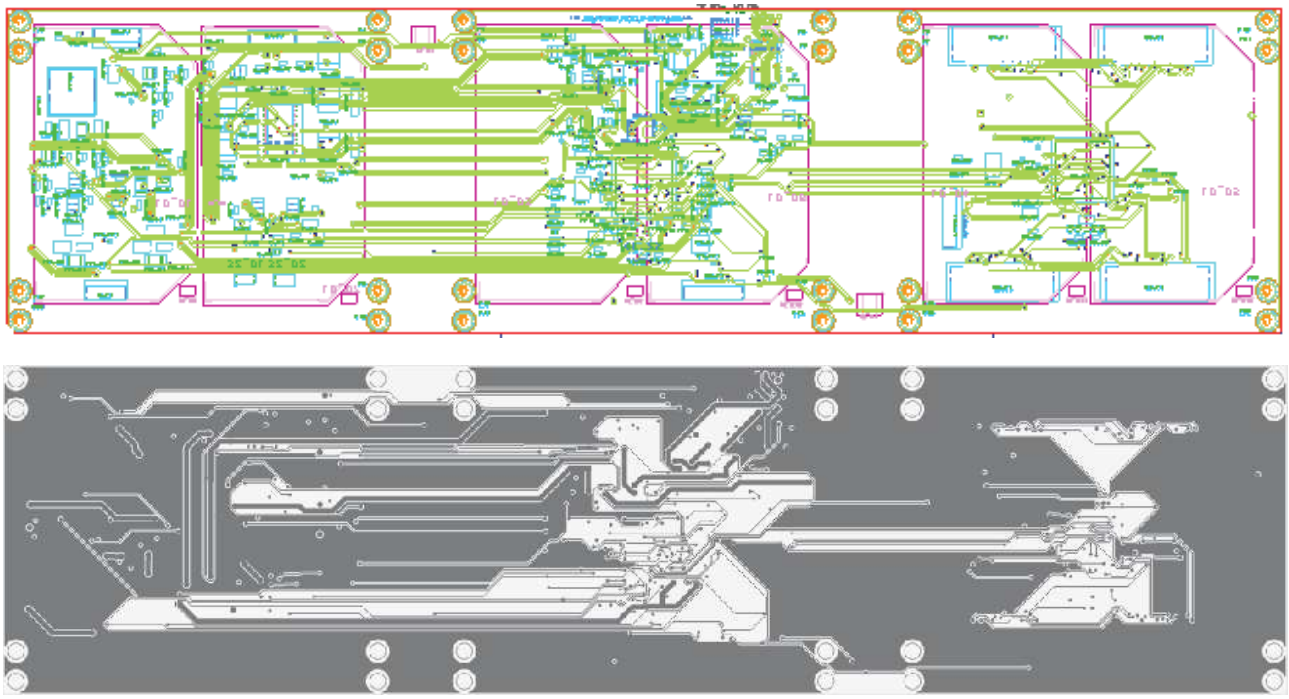


Figure 8.8: View of Layer 3 and its Copper

Layer 4 to 7

The layer 3 carries the most used power signal 3.3 V of the system. The trace width is wider due to low heat dissipation in the printed circuit board. It is shown in the figure below 8.9.

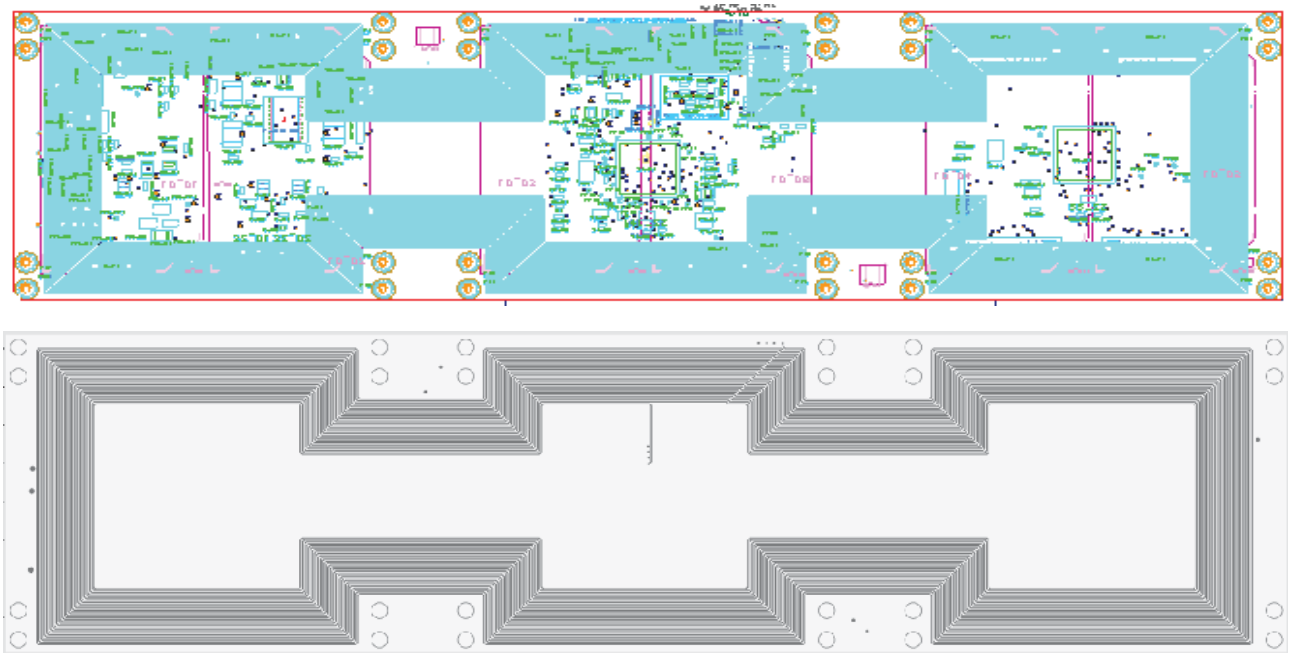


Figure 8.9: View of Layer 4 to 7 and its Copper

Layer 8

The bottom layer consists of the image sensor and the bypass capacitors placed near the exposed pads of the processor and this is shown in the figure below 8.10.

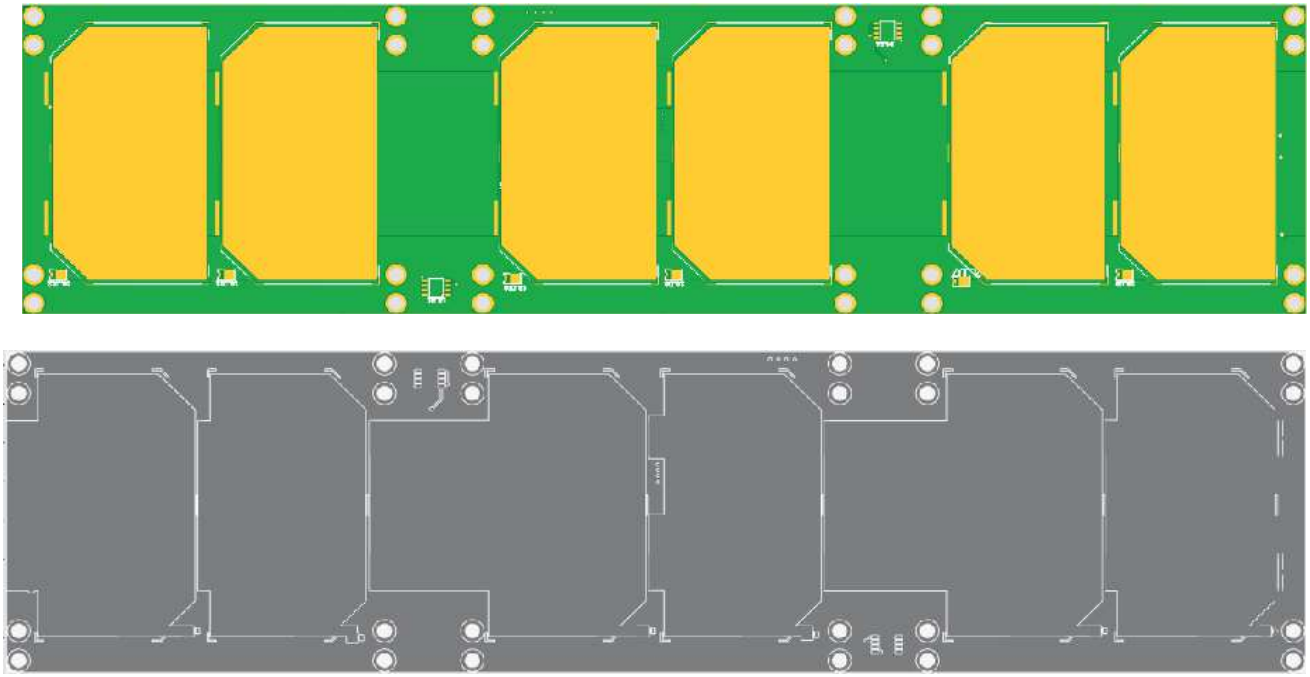


Figure 8.10: View of Layer 8 and its Copper

8.5 Analysis and Optimization:

The analysis is done by running the Batch DRC to support the verification clearance inside the rule areas. The rule areas used for the net class verification clearance are: Plane to Plane, Plane to Part, Part to Plane, Plane to via pad, via pad to via pad, Via Pad to Pad and Part Pad to Part Pad. The executed controls are:

- Proximity Control: verifies that all the clearance specified are respected as specified in the route parameters.
- Connectivity Control: Checks the tracks and connect to the pins avoiding floating tracks.
- Special rules ensures to meet the special manufacturing rules

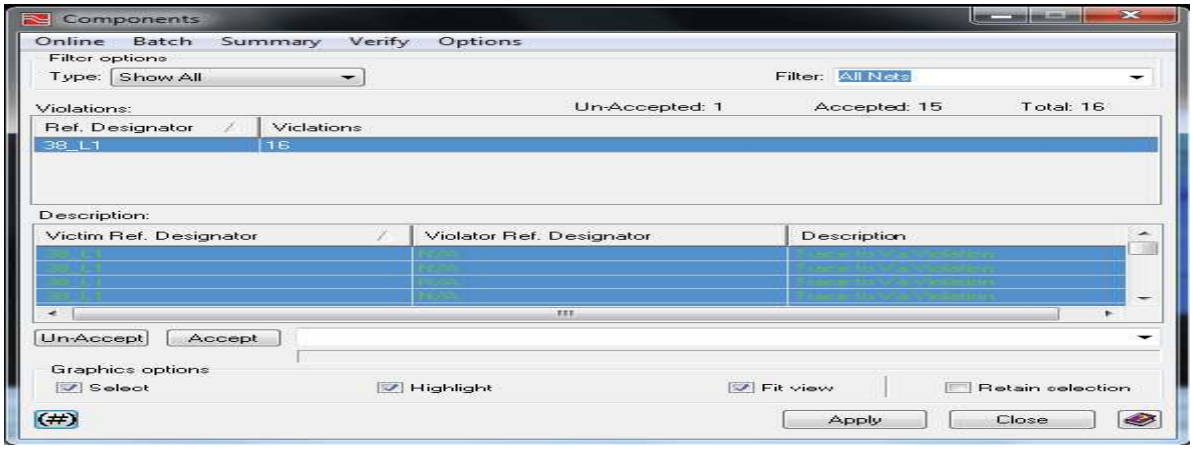


Figure 8.11: Batch DRC and Review Hazards

Once you run the Batch DRC and after you run the Online DRC, it is possible to check the violations as warnings. At first, as shown in the figure Review Hazards dialog box appears and then we must click Update Hazard Count (#) present in the bottom left corner. Then, Show All hazards in the menus and it also provides the option to view the hazards in the violation list and the description of the hazard.

8.6 Mechanical Analysis of PCB of Satellite:

Once the PCB is designed for 1B8_CubePMT_3U, the placement in the board is analyzed and adjusted to optimum position according to the mechanical environment.

In order to analyze the geometry of the printed circuit board, we used the software Solid works. The 3D model can be exported from the Expedition PCB through Export→IDF and can be used in Solid works. It can also use the Gerber and NCDrill files to generate the three dimensional view and this not only from electrical point of view and also to verify that the design fits well to the structure of the satellite.

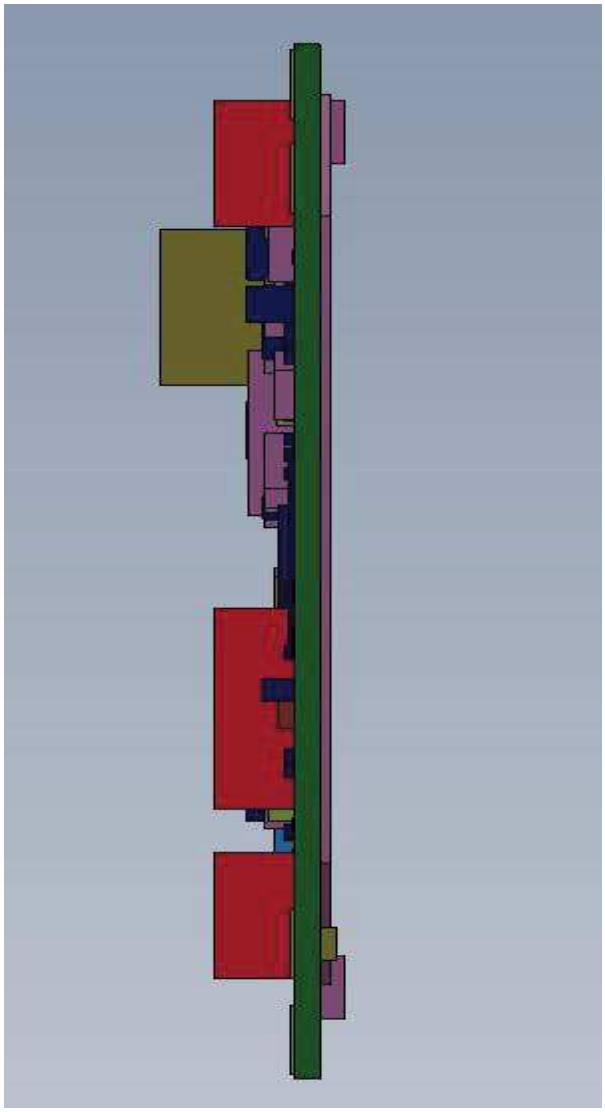


Figure 8.12: 3D representation of PCB designed

Once the Printed Circuit Board is inserted in the appropriate manner, the placements of the components are analyzed from the point of view space used. Then, the heights of the components are also verified so that we can sufficient space to insert the payload of our choice with respect to the mission. It also helped in determining the epicenter of the board to place the Image sensor.

- **VIEW TOP LAYER**

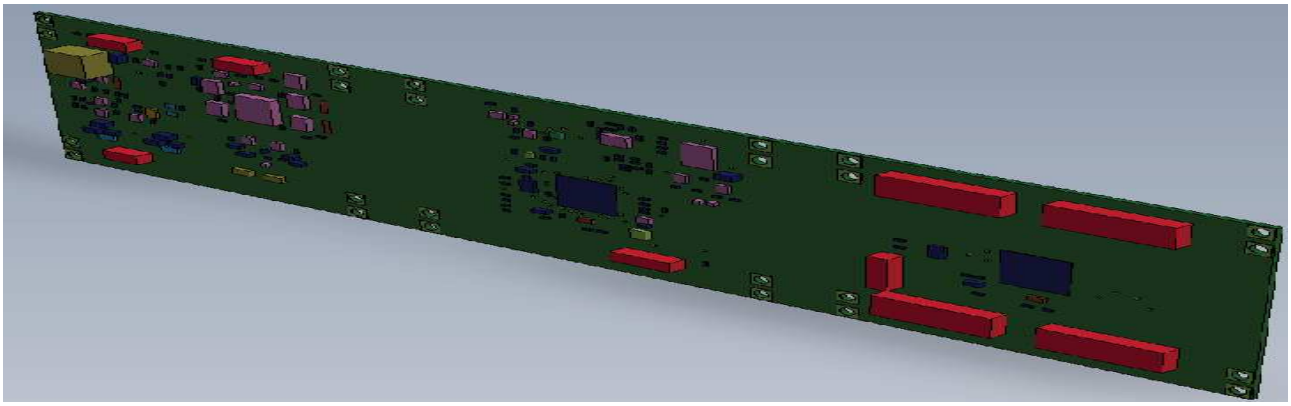


Figure 8.13: 3D representation of PCB designed

From the figure above, you can visualize the presence of the bulky devices on both the outer layers, both with respect to occupied area, and the height occupied inside the satellite and these components are Processor in the first layer and the Image sensor in the last layer and the connectors placed in the bottom part of the layer1.

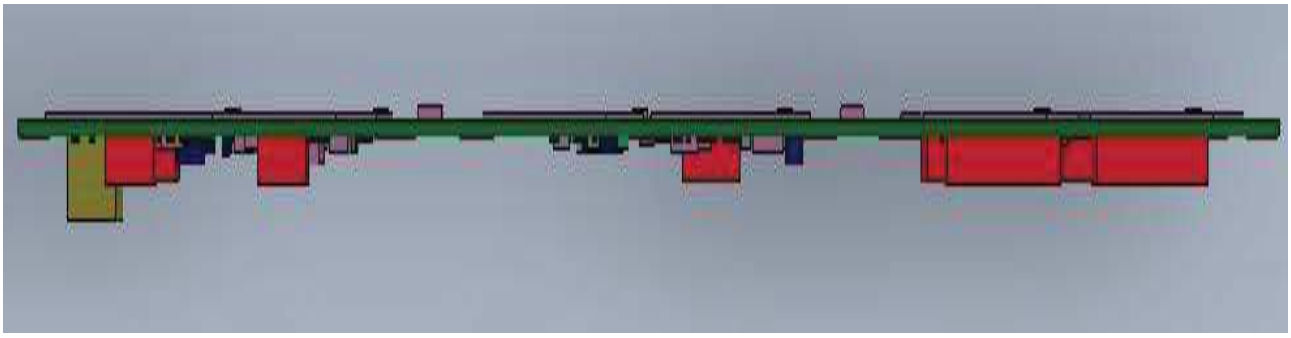


Figure 8.14: 3D front view of the Tile

- **Bottom Layer**

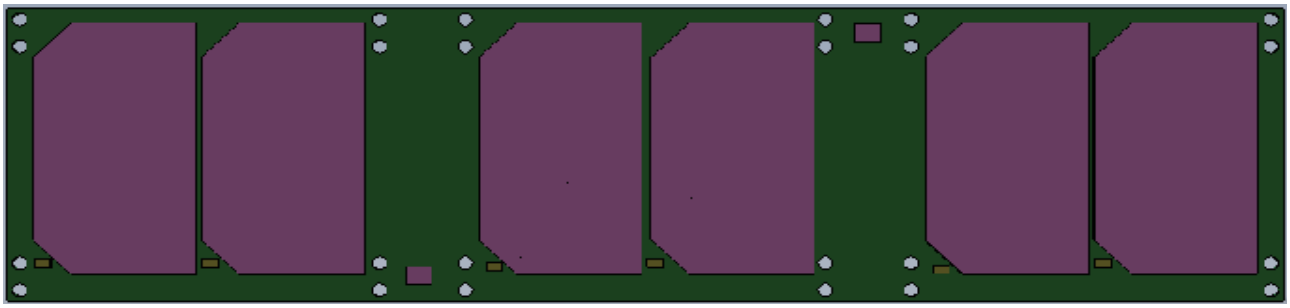


Figure 8.15: 3D Bottom view of the board with components

In this side, we can observe from the figure that components placed on this side are reduced including their height.

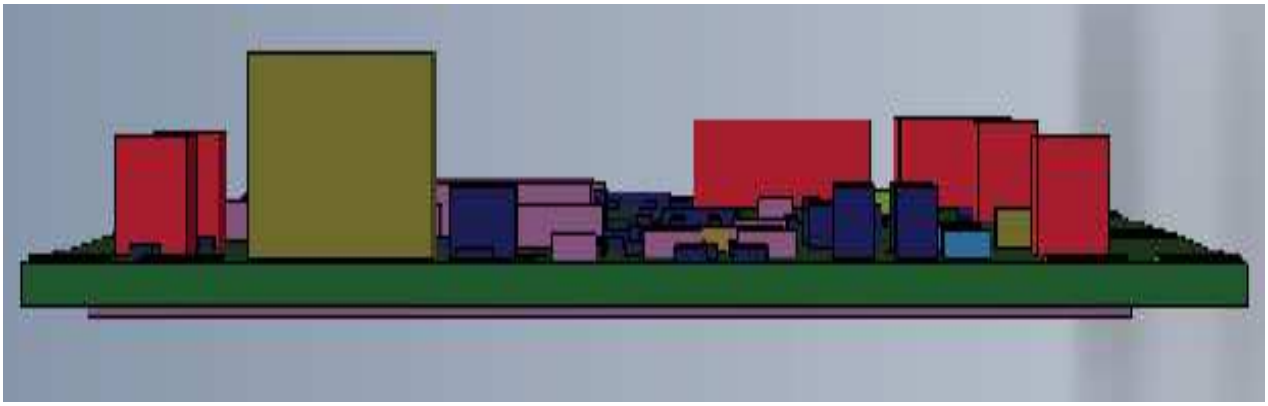
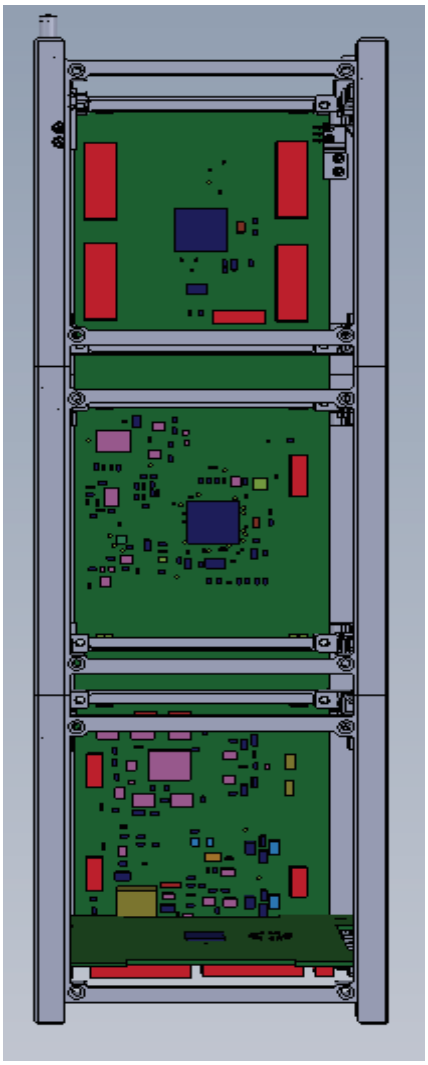
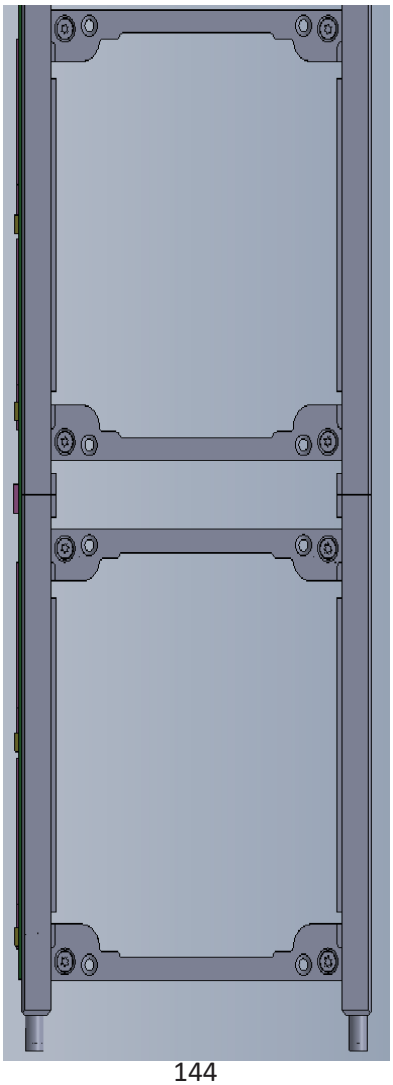


Figure 8.16: Side view of the board with components

At the end, the full structure of the satellite with the insertion of the full board inside the cubic structure of the satellite to verify the interference produced between geometry of the device and the satellite structure.





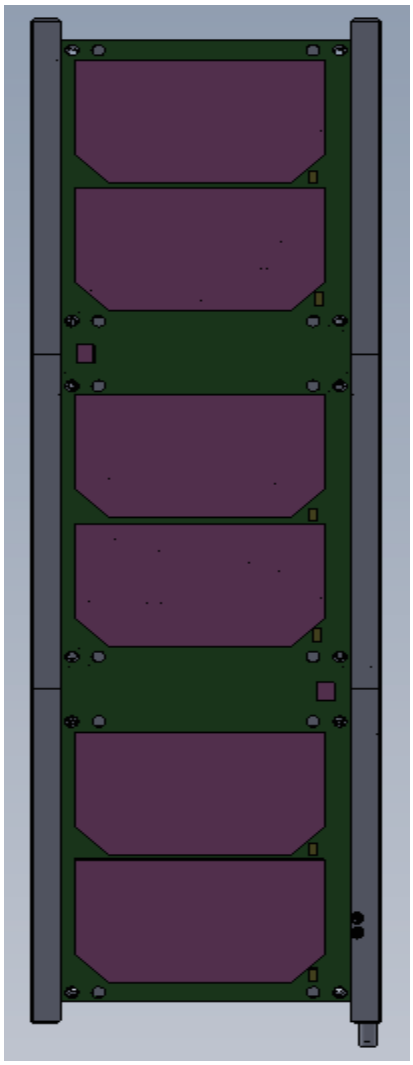


Figure 8.17: View of several structures inside AraMiS

Using Solid Works, the appropriate analysis are made to verify the mechanical interference and the results there is no presence of mechanical interference.

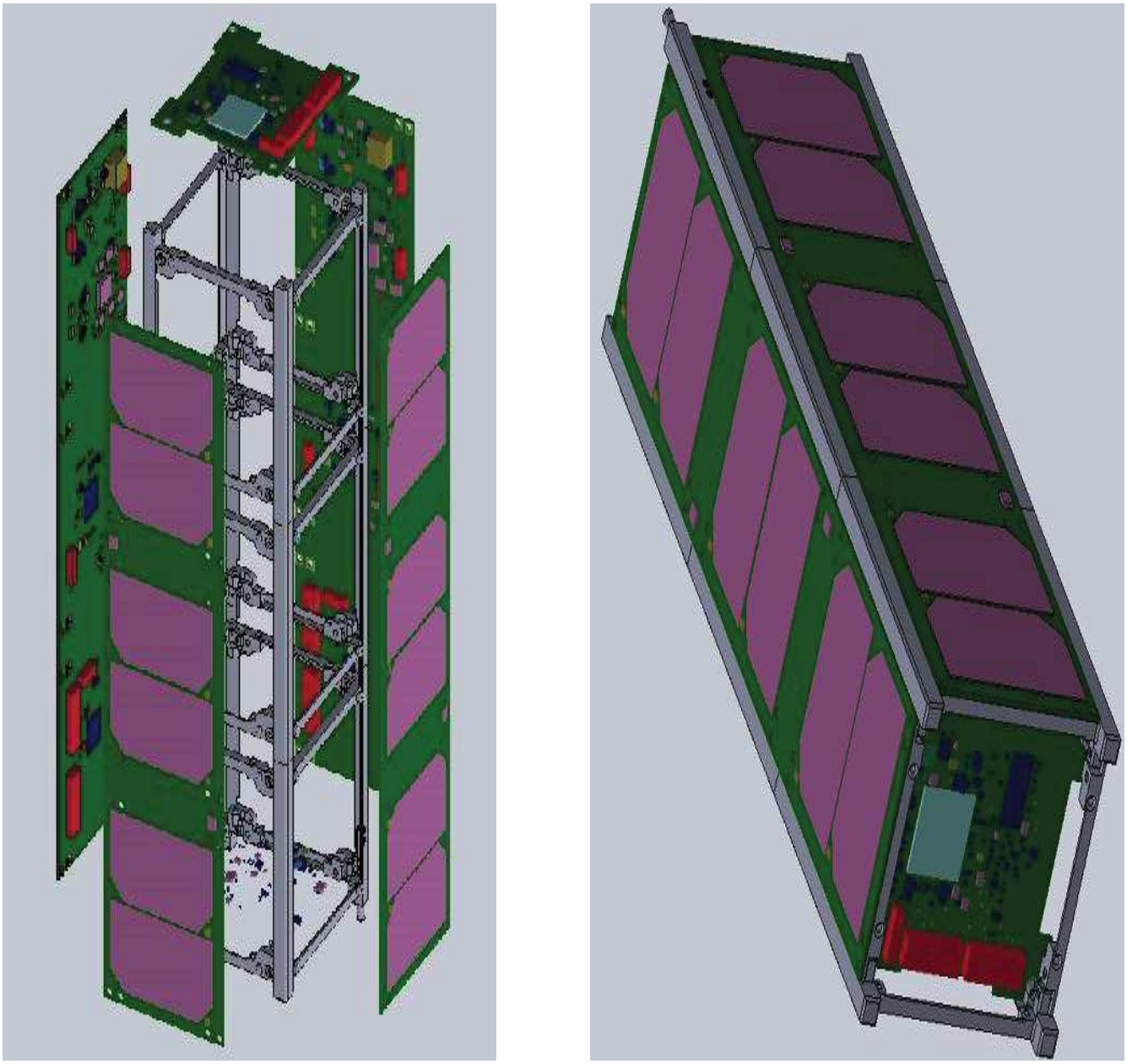


Figure 8.18: Both Burst and United form of 3D presentation of the board 1B8_CubePMT_3U

At the end, these three steps are performed to manufacture the PCB:

- Generating the file for drilling the rig, that it will carry the hole on the PCB called as NCDrill.
- Generate silkscreen through Silkscreen generator, the upper side is printed with Ref des associated with the components

- Gerber files generated to manufacturer of PCBs, track physically the PCB, using the Gerber output of Gerber Tool, which also lets you perform a final check of the PCB.

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